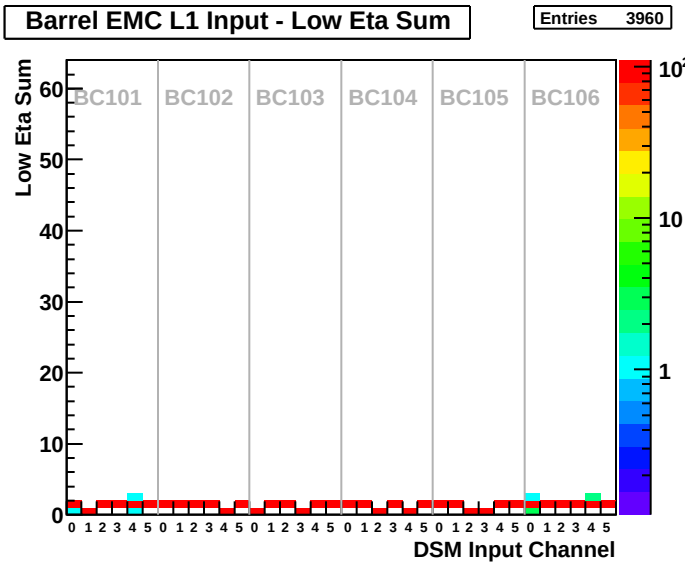
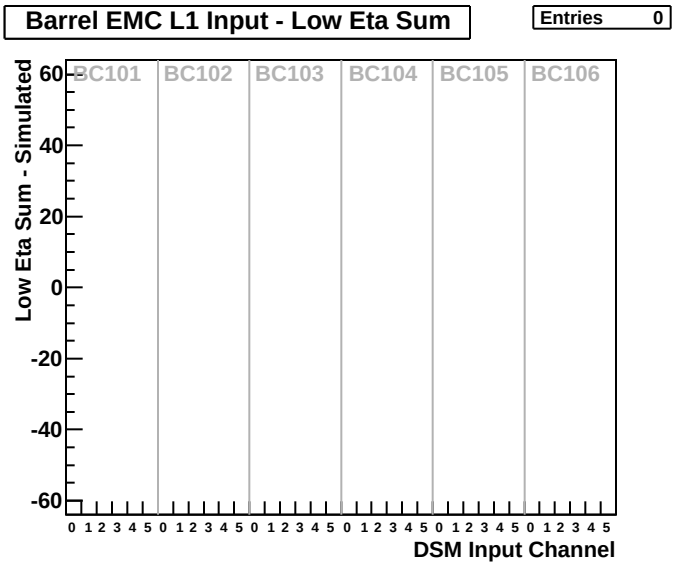
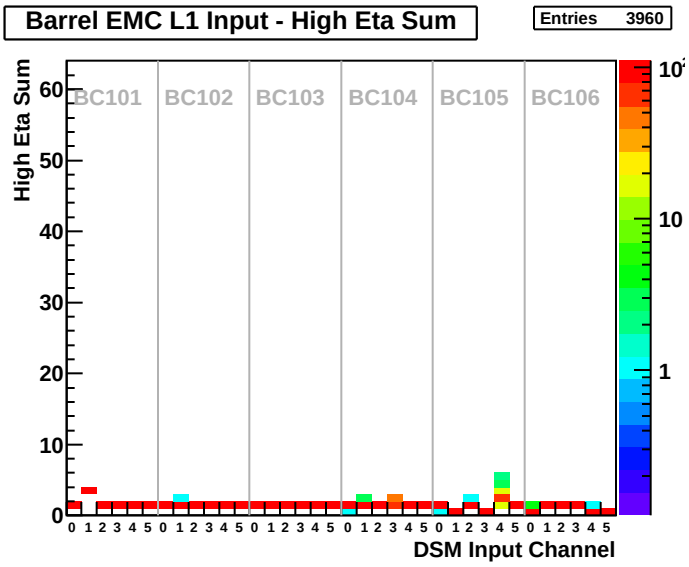
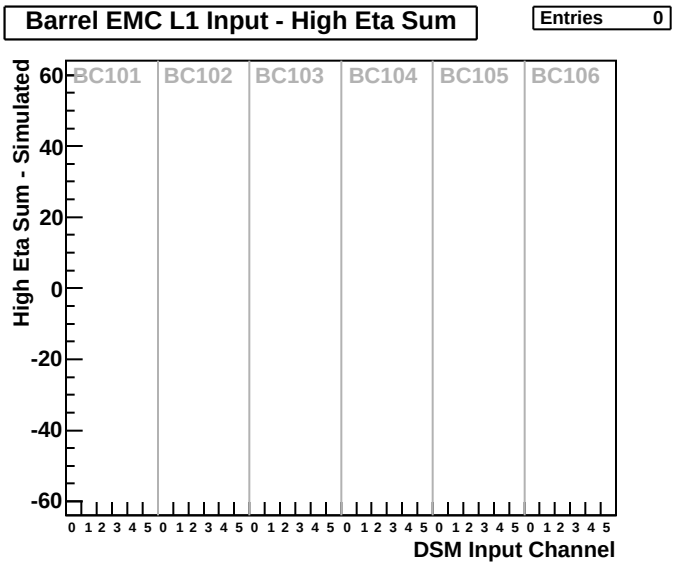
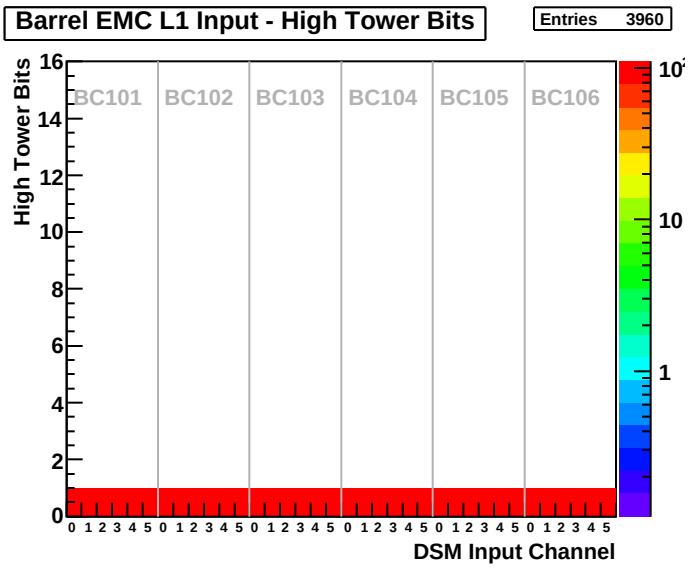
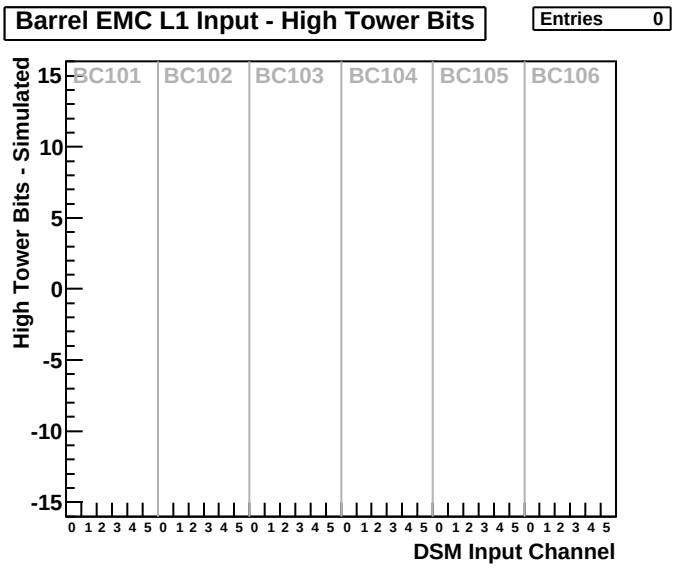

Barrel EMC L1 Input - Low Eta Sum
Entries 3960
Low Eta Sum
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

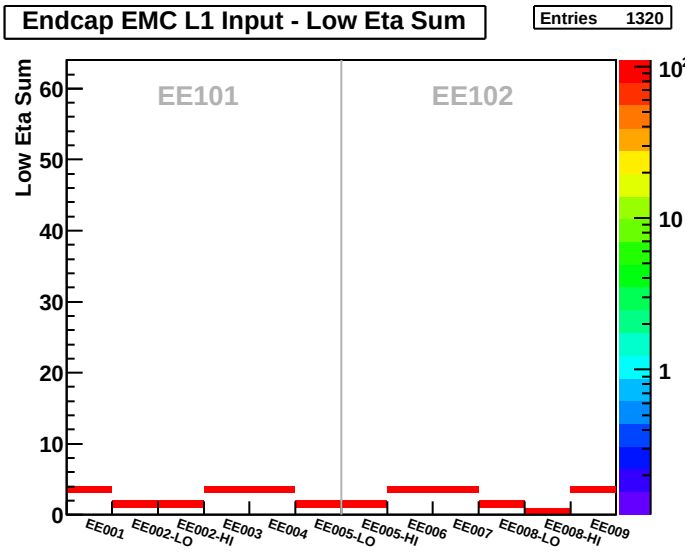

Barrel EMC L1 Input - Low Eta Sum
Entries 0
Low Eta Sum - Simulated
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

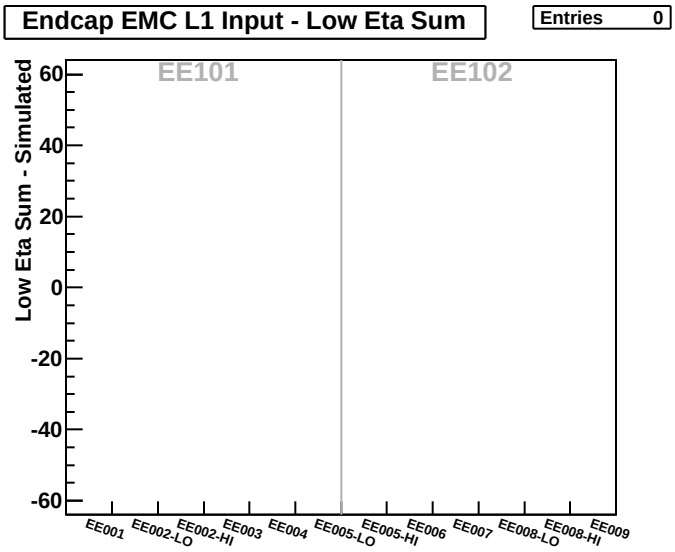

Barrel EMC L1 Input - High Eta Sum
Entries 3960
High Eta Sum
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

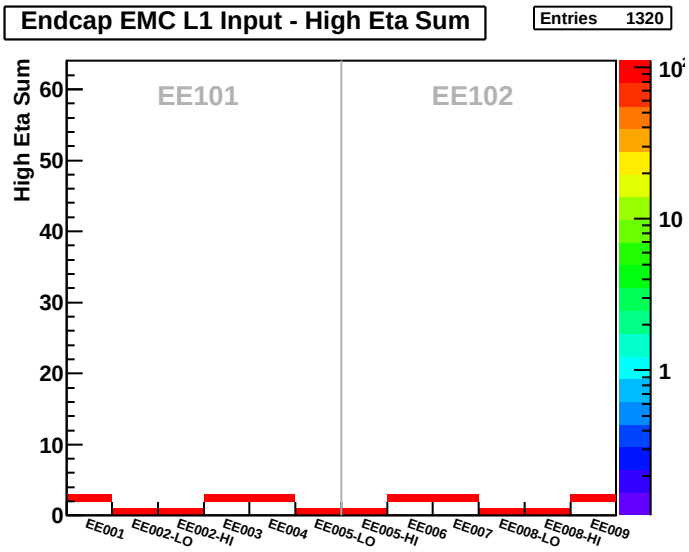

Barrel EMC L1 Input - High Eta Sum
Entries 0
High Eta Sum - Simulated
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

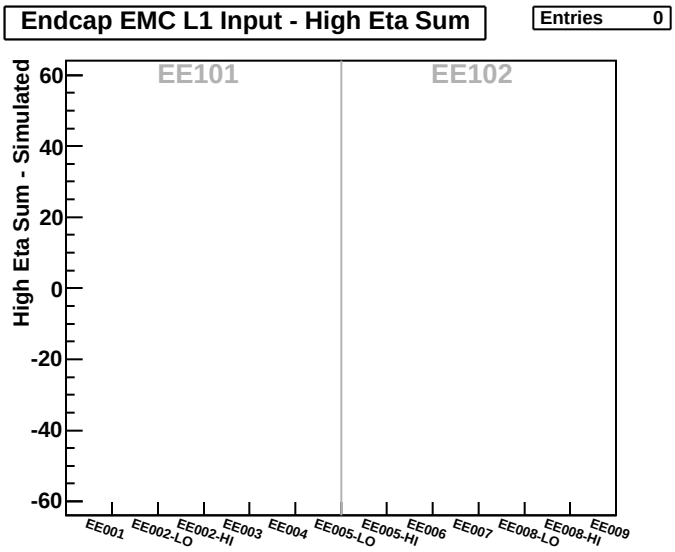

Barrel EMC L1 Input - High Tower Bits
Entries 3960
High Tower Bits
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

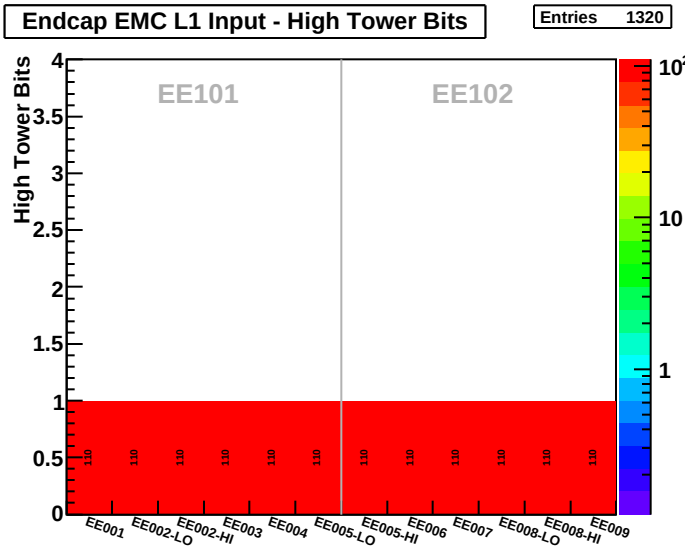

Barrel EMC L1 Input - High Tower Bits
Entries 0
High Tower Bits - Simulated
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

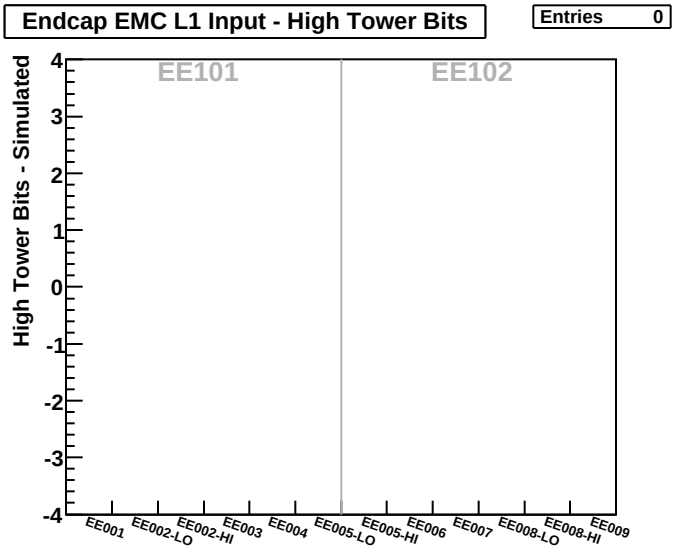

Endcap EMC L1 Input - Low Eta Sum
Entries 1320
Low Eta Sum
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

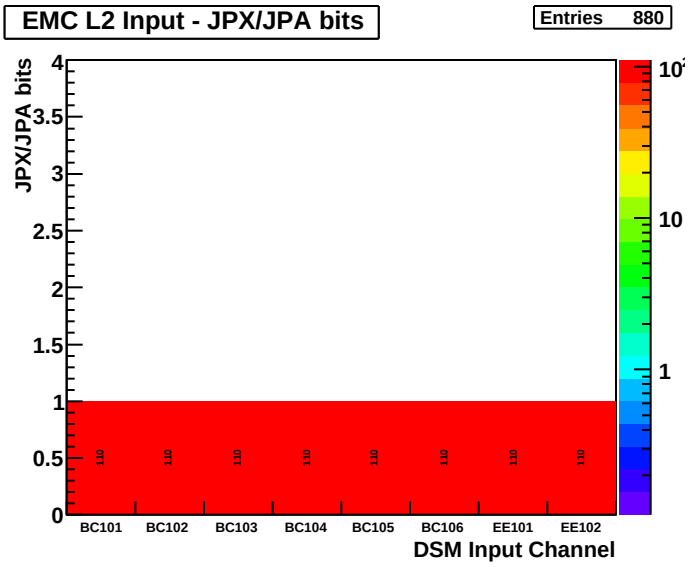

Endcap EMC L1 Input - Low Eta Sum
Entries 0
Low Eta Sum - Simulated
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

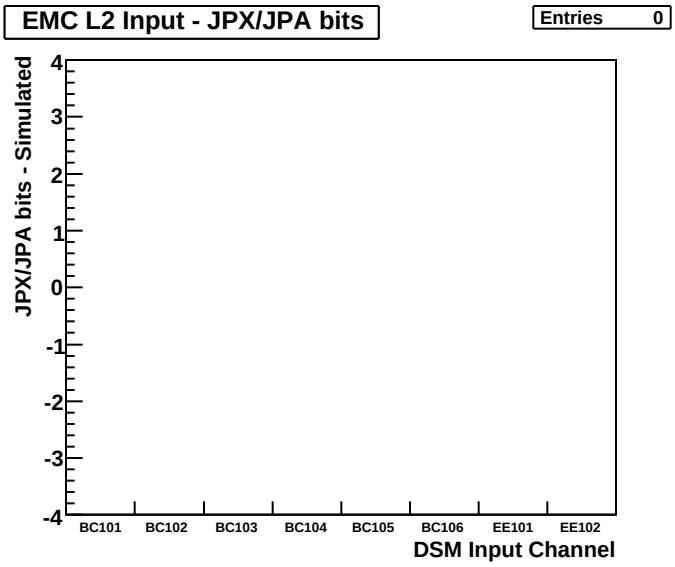

Endcap EMC L1 Input - High Eta Sum
Entries 1320
High Eta Sum
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

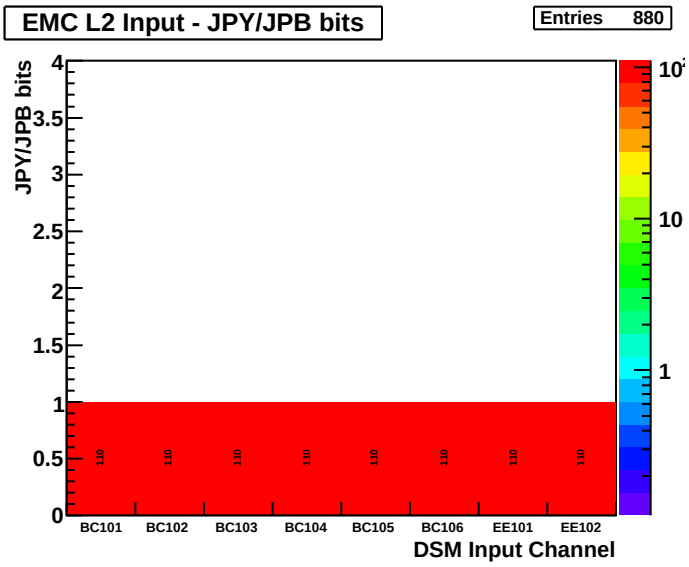

Endcap EMC L1 Input - High Eta Sum
Entries 0
High Eta Sum - Simulated
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

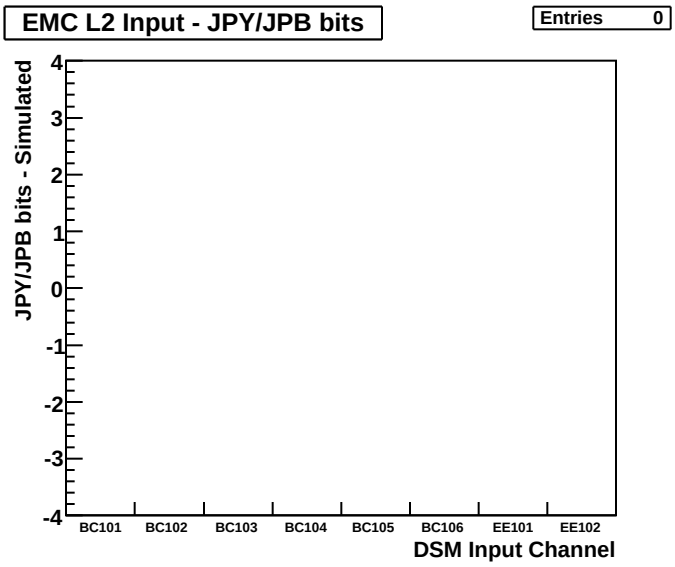

Endcap EMC L1 Input - High Tower Bits
Entries 1320
High Tower Bits
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

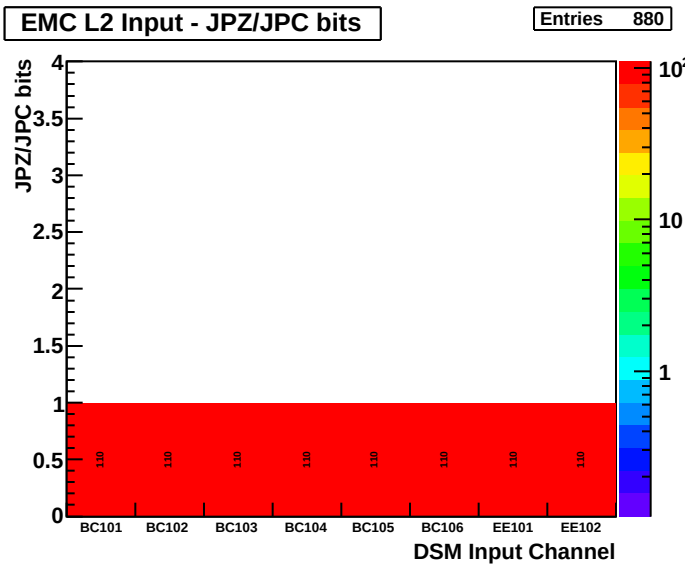

Endcap EMC L1 Input - High Tower Bits
Entries 0
High Tower Bits - Simulated
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

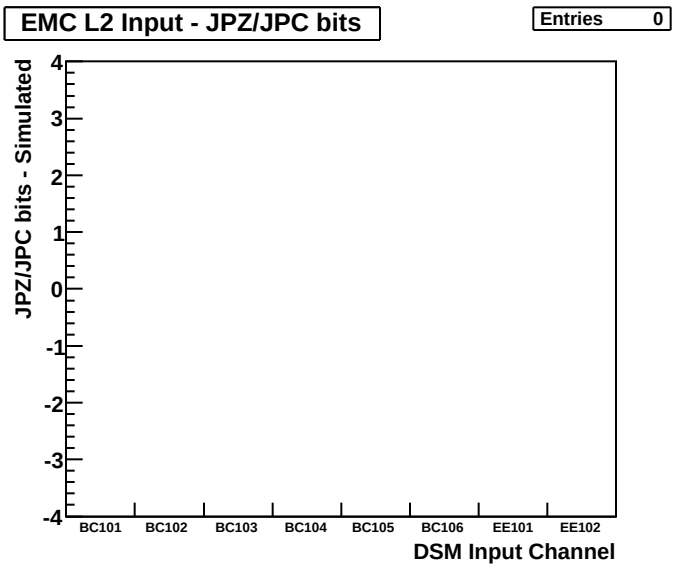

EMC L2 Input - JPX/JPA bits
Entries 880
JPX/JPA bits
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

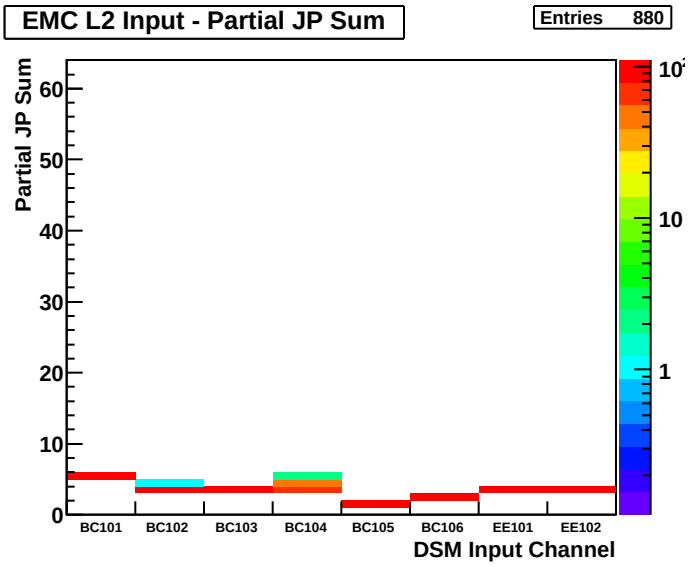

EMC L2 Input - JPX/JPA bits
Entries 0
JPX/JPA bits - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

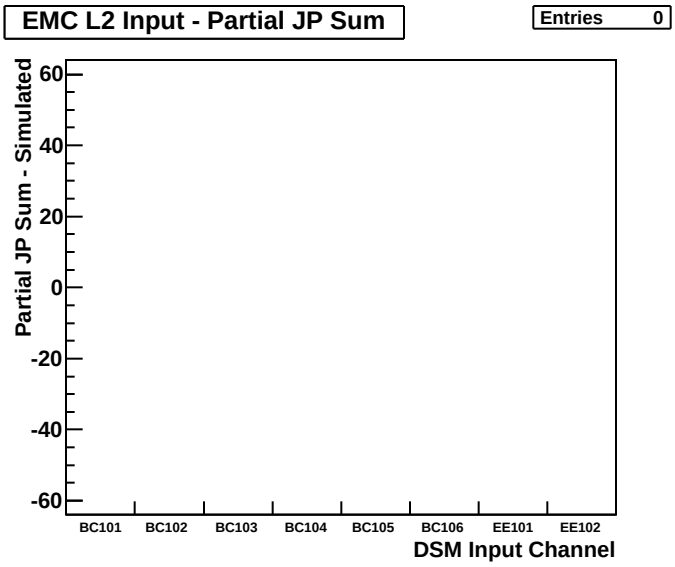

EMC L2 Input - JPY/JPB bits
Entries 880
JPY/JPB bits
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

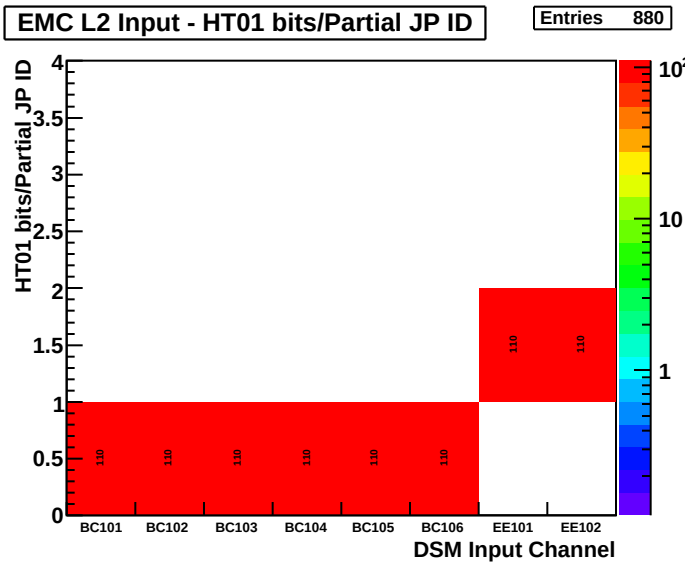

EMC L2 Input - JPY/JPB bits
Entries 0
JPY/JPB bits - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

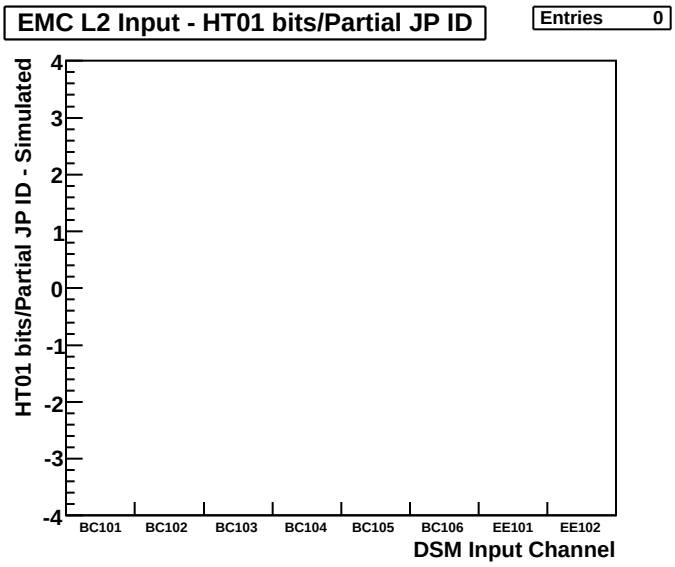

EMC L2 Input - JPZ/JPC bits
Entries 880
JPZ/JPC bits
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

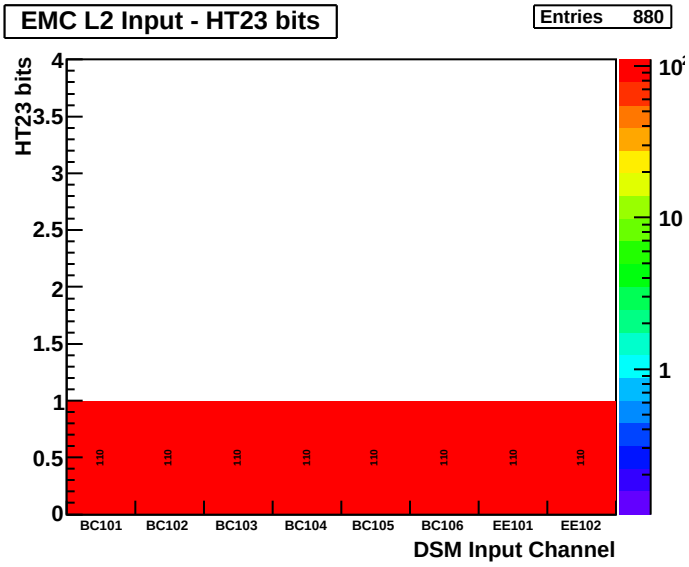

EMC L2 Input - JPZ/JPC bits
Entries 0
JPZ/JPC bits - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

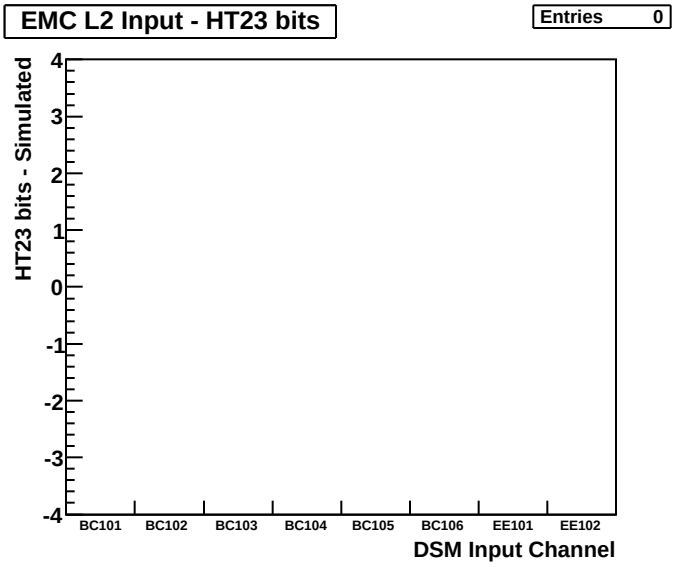

EMC L2 Input - Partial JP Sum
Entries 880
Partial JP Sum
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

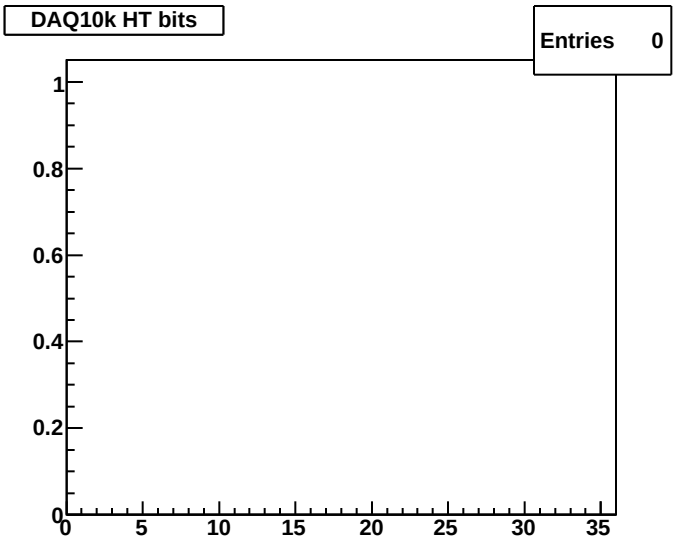

EMC L2 Input - Partial JP Sum
Entries 0
Partial JP Sum - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

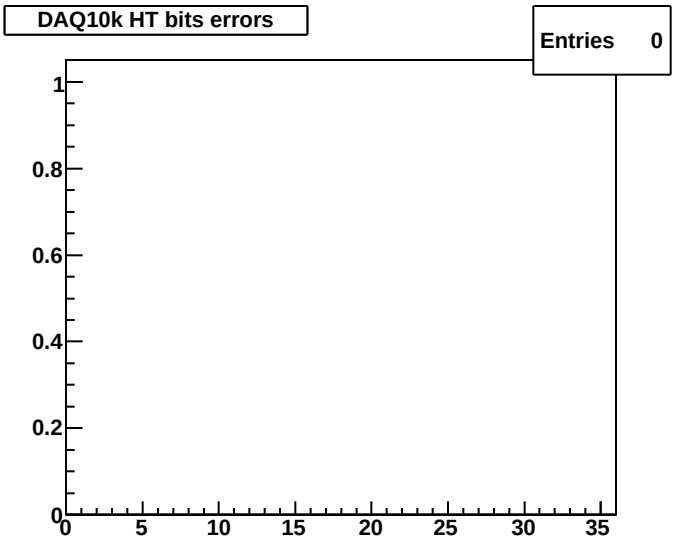

EMC L2 Input - HT01 bits/Partial JP ID
Entries 880
HT01 bits/Partial JP ID
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

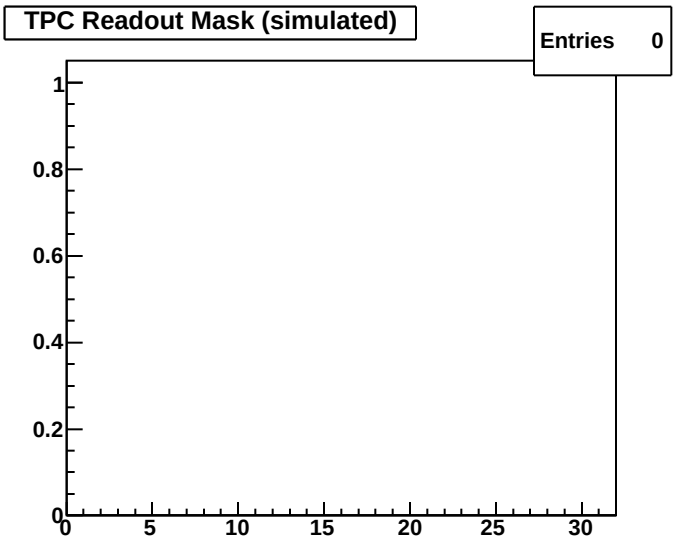

EMC L2 Input - HT01 bits/Partial JP ID
Entries 0
HT01 bits/Partial JP ID - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

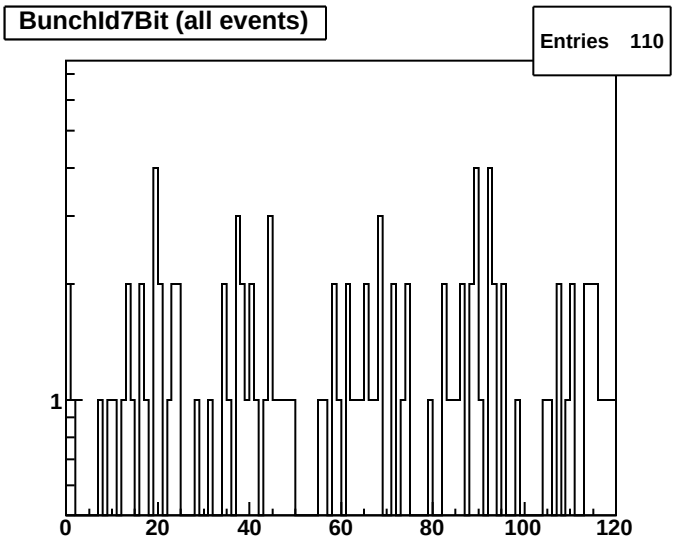

EMC L2 Input - HT23 bits
Entries 880
HT23 bits
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

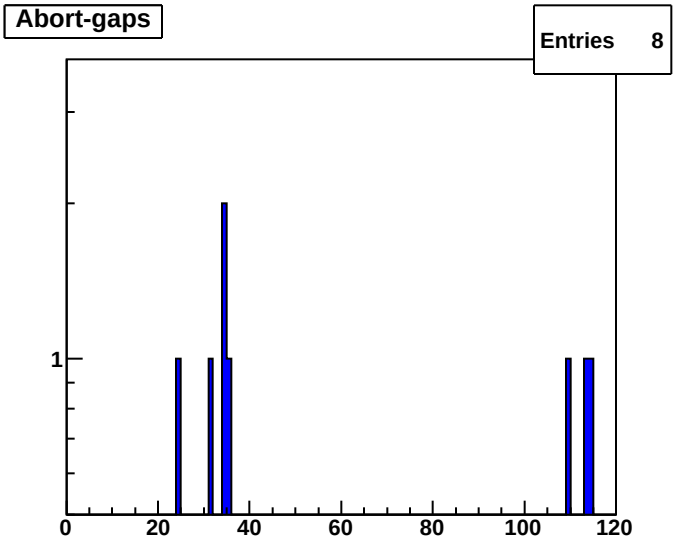

EMC L2 Input - HT23 bits
Entries 0
HT23 bits - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

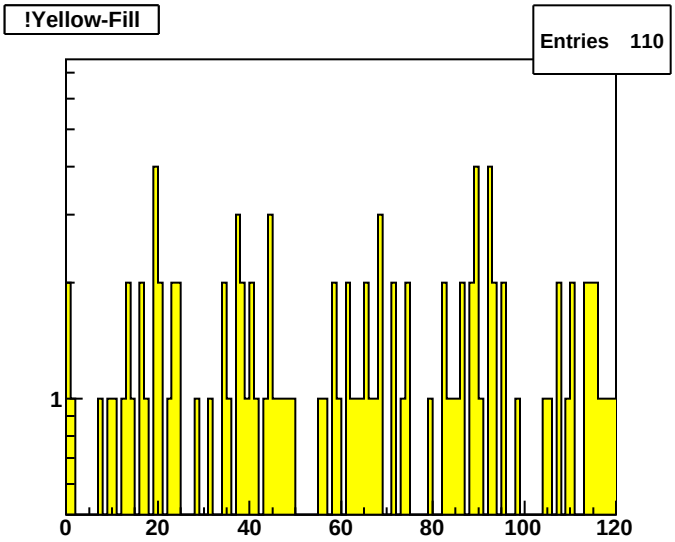

DAQ10k HT bits
Entries 0
1
0.8
0.6
0.4
0.2
0
0 5 10 15 20 25 30 35

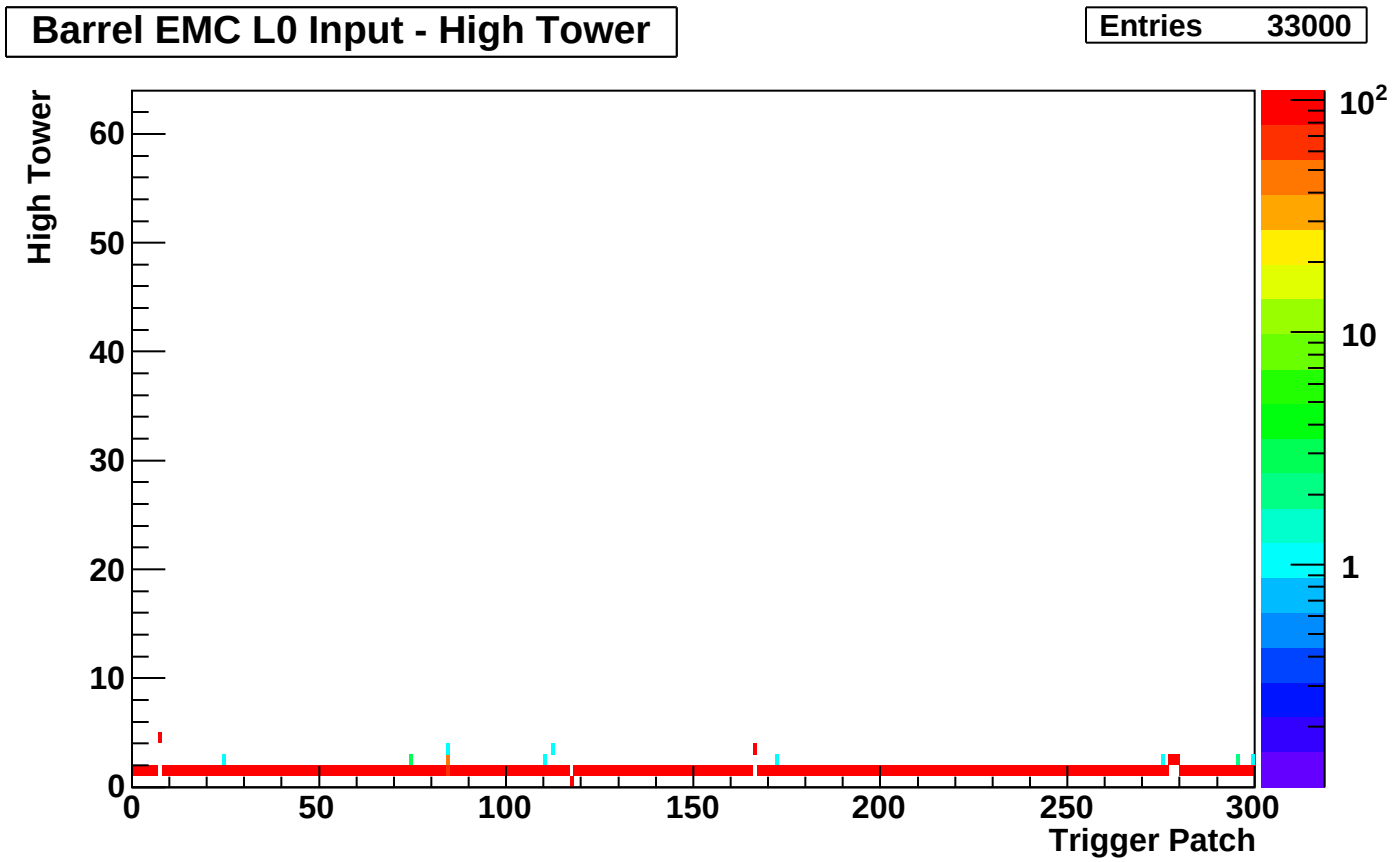

DAQ10k HT bits errors
Entries 0
1
0.8
0.6
0.4
0.2
0
0 5 10 15 20 25 30 35

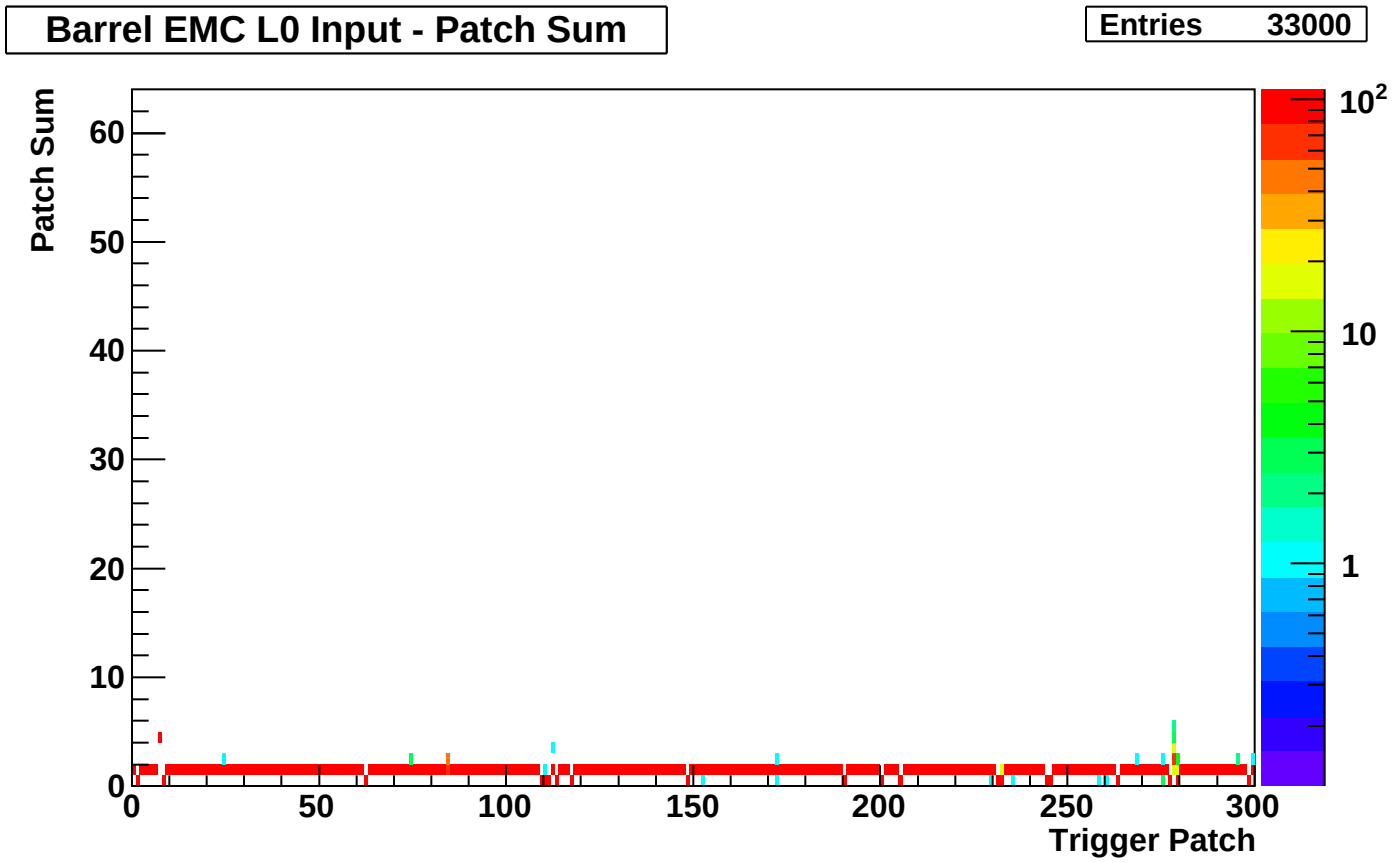

TPC Readout Mask (simulated)
Entries 0
1
0.8
0.6
0.4
0.2
0
0 5 10 15 20 25 30

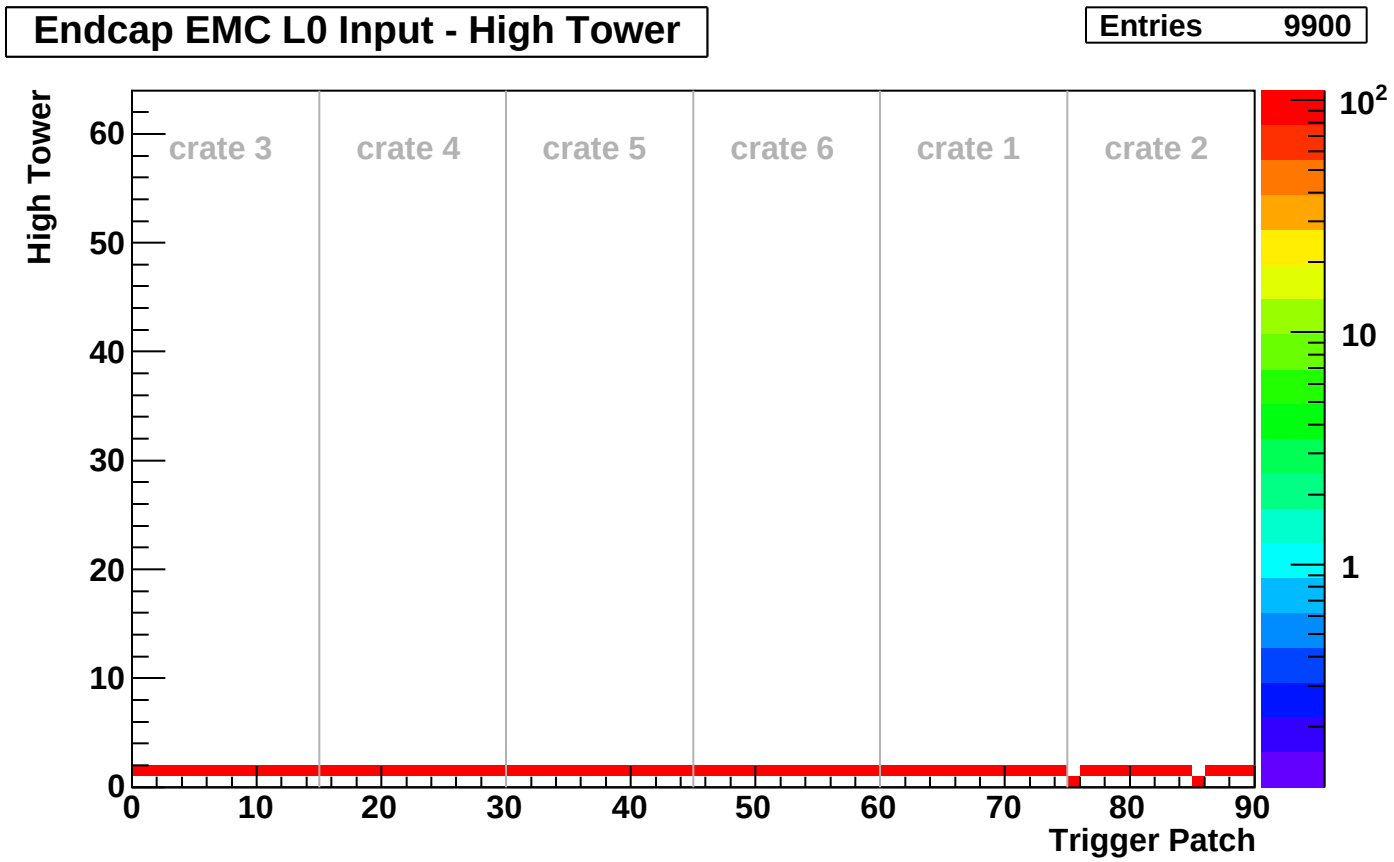

BunchId7Bit (all events)
Entries 110
1
0 20 40 60 80 100 120

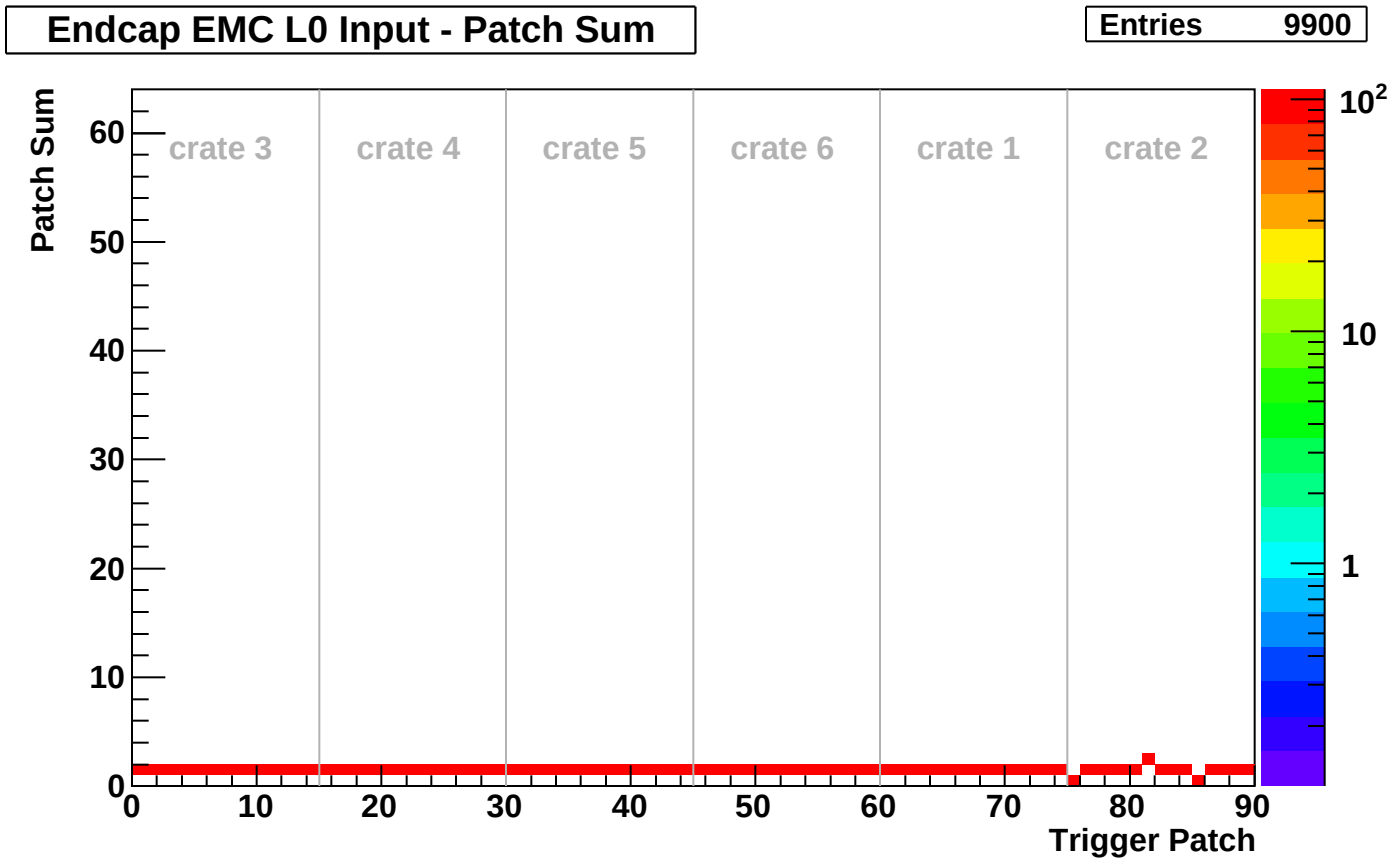

Abort-gaps
Entries 8
1
0 20 40 60 80 100 120

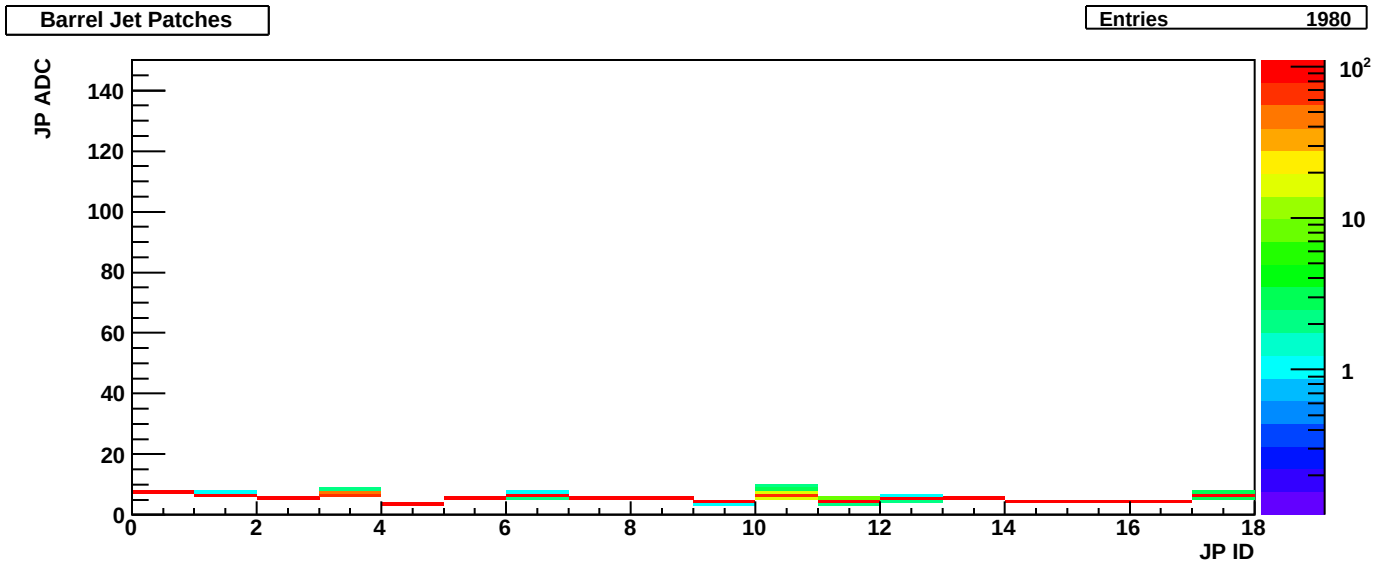

!Yellow-Fill
Entries 110
1
0 20 40 60 80 100 120

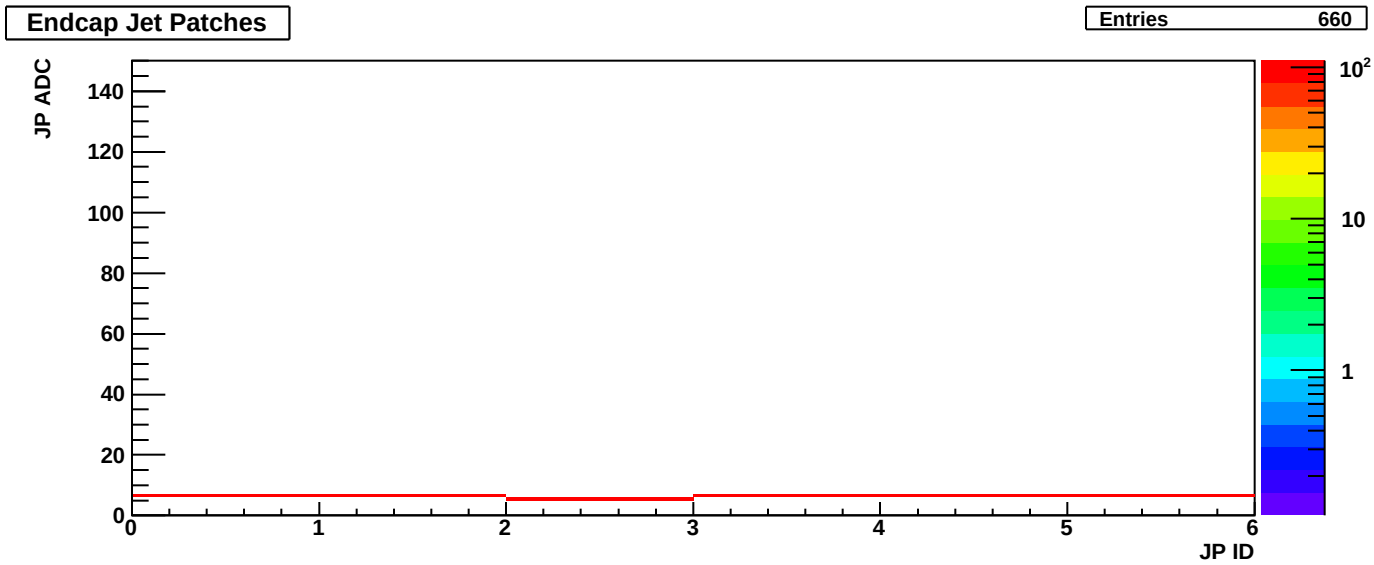

Barrel EMC L0 Input - High Tower
Entries 33000
High Tower
0
10
20
30
40
50
60
0
50
100
150
200
250
300
Trigger Patch
10^2
10
1

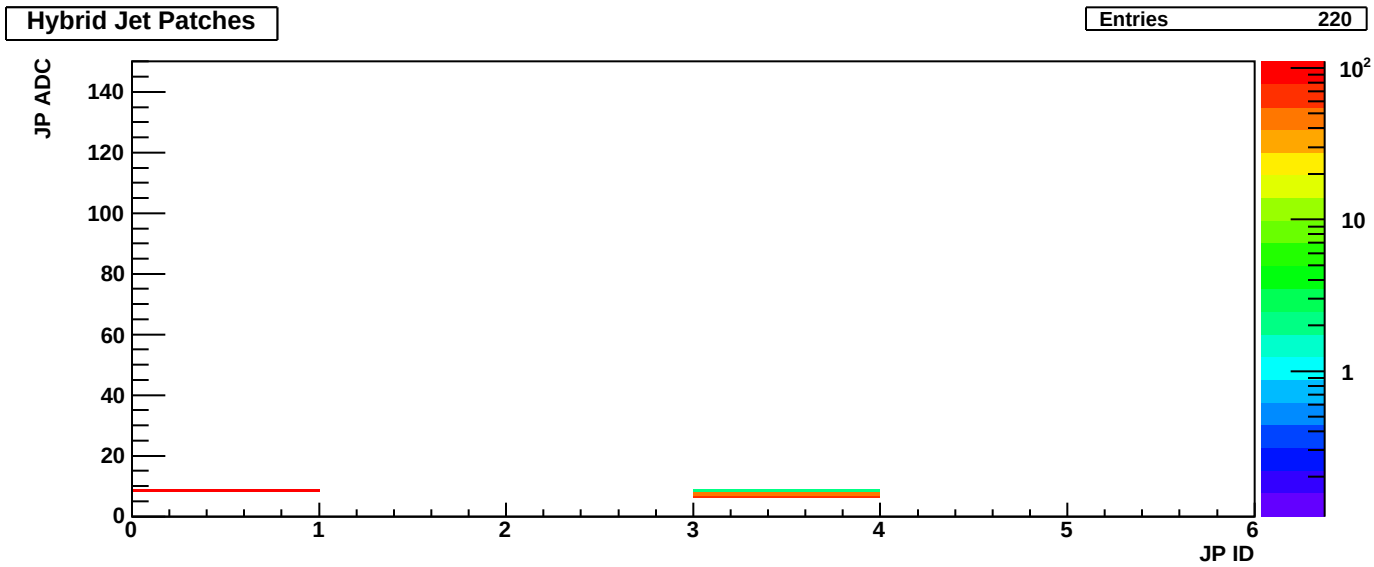

Barrel EMC L0 Input - Patch Sum
Entries 33000
Patch Sum
0
10
20
30
40
50
60
0
50
100
150
200
250
300
Trigger Patch
10^2
10
1

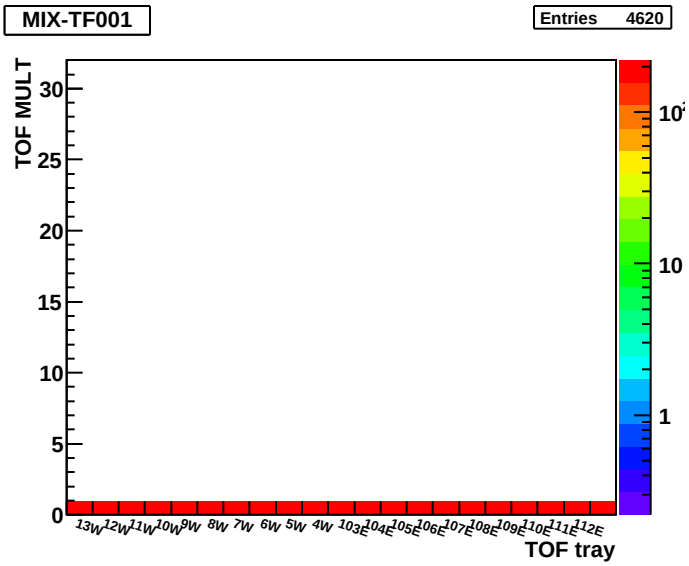

Endcap EMC L0 Input - High Tower
Entries 9900
High Tower
crate 3
crate 4
crate 5
crate 6
crate 1
crate 2
Trigger Patch
10^2
10
1

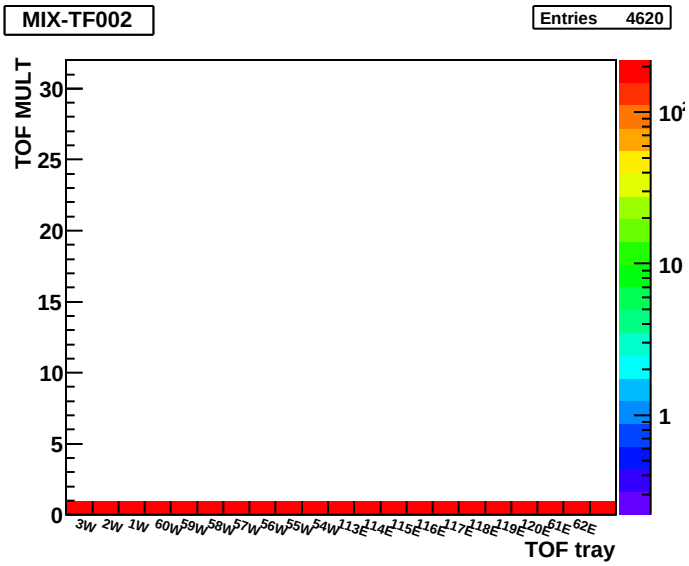

Endcap EMC L0 Input - Patch Sum
Entries 9900
Patch Sum
crate 3
crate 4
crate 5
crate 6
crate 1
crate 2
Trigger Patch
10^2
10
1

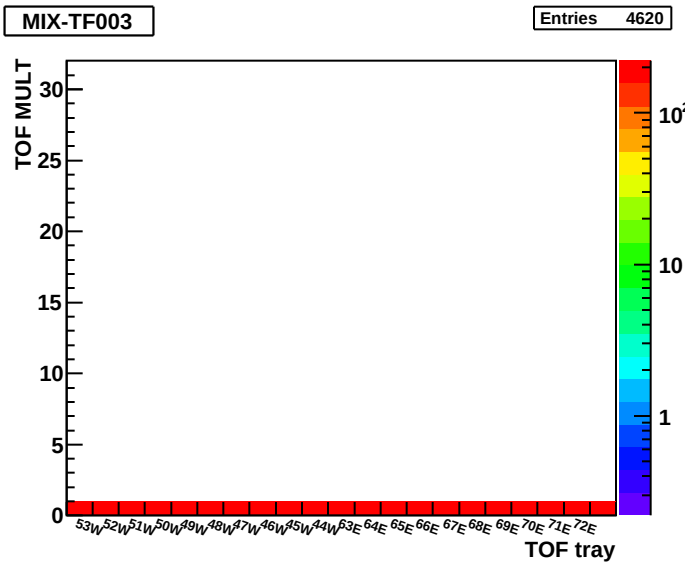

Barrel Jet Patches
Entries 1980
JP ADC
JP ID

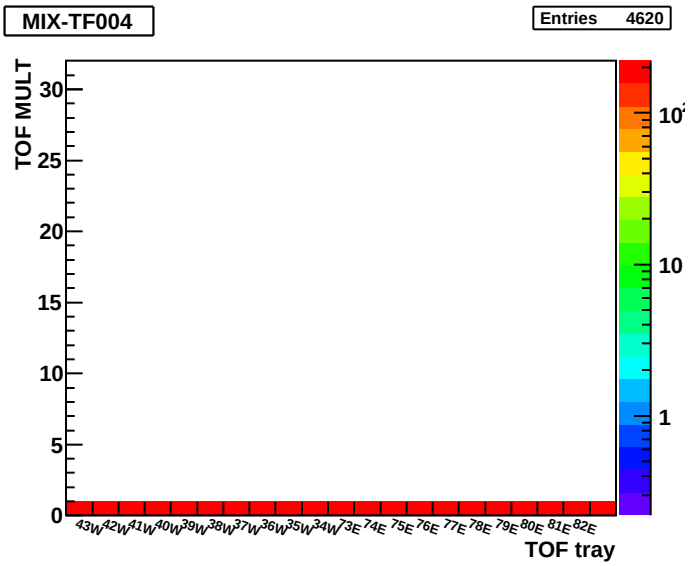

Endcap Jet Patches
Entries 660
JP ADC
JP ID

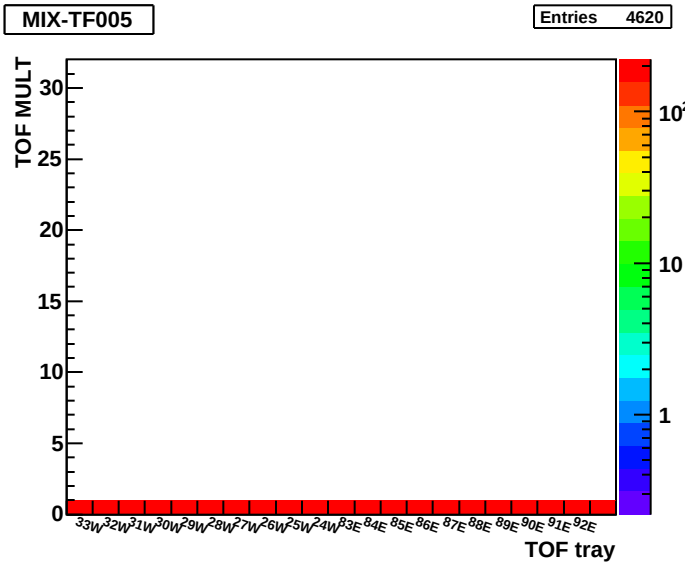

Hybrid Jet Patches
Entries 220
JP ADC
JP ID

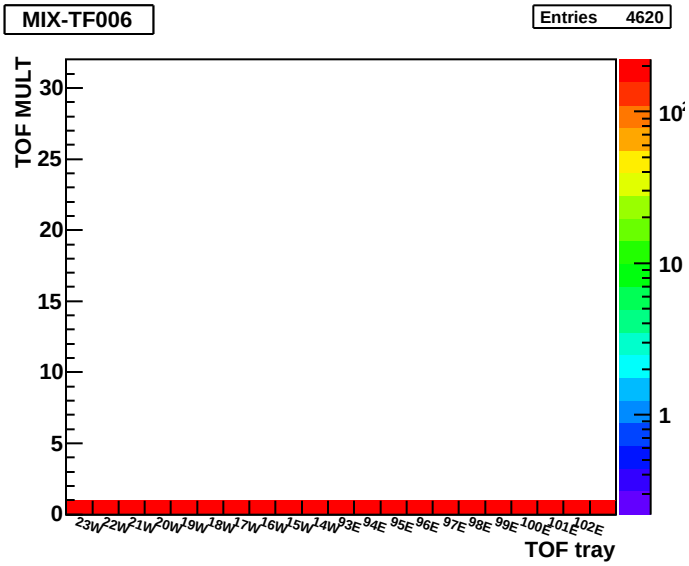

MIX-TF001
Entries 4620
TOF MULT
TOF tray

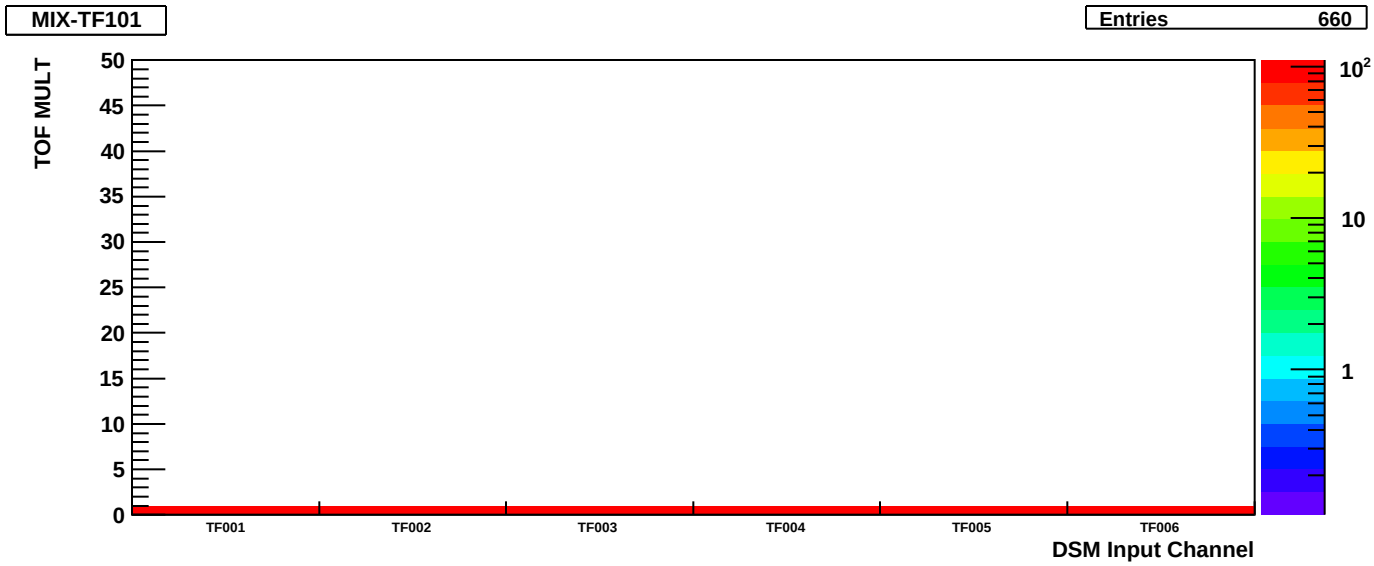

MIX-TF002
Entries 4620
TOF MULT
TOF tray

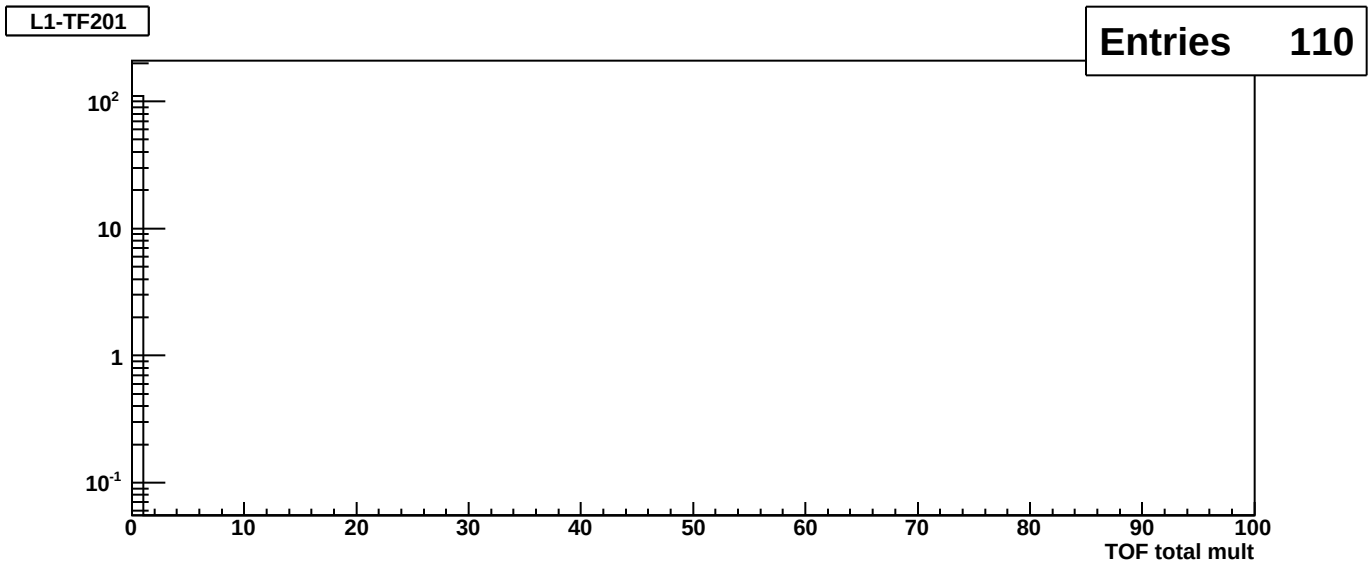

MIX-TF003
Entries 4620
TOF MULT
TOF tray

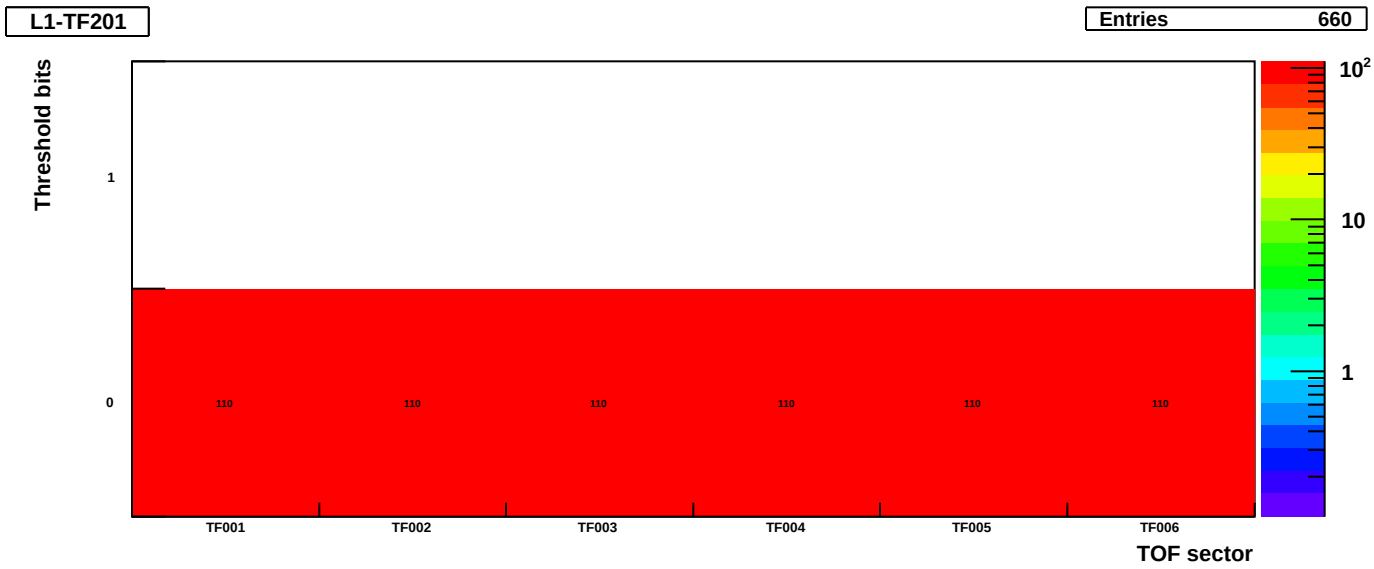

MIX-TF004
Entries 4620
TOF MULT
TOF tray

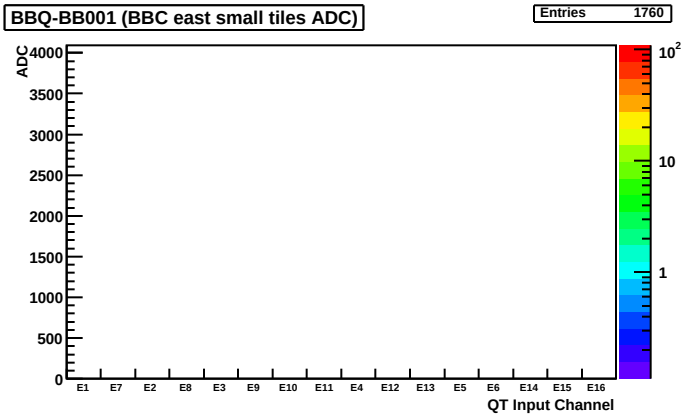

MIX-TF005
Entries 4620
TOF MULT
TOF tray

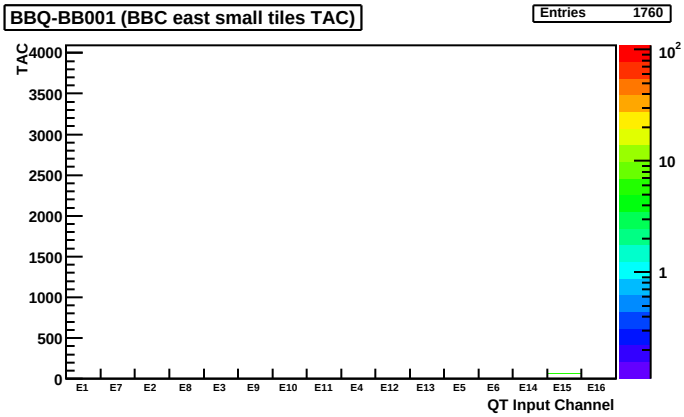

MIX-TF006
Entries 4620
TOF MULT
TOF tray

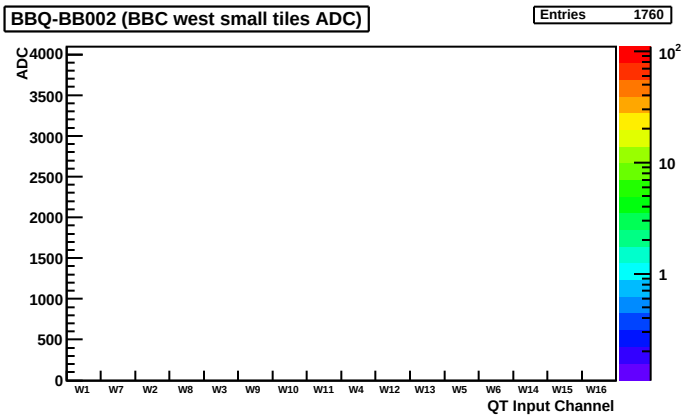

MIX-TF101
Entries 660
TOF MULT
50
45
40
35
30
25
20
15
10
5
0
TF001
TF002
TF003
TF004
TF005
TF006
DSM Input Channel
10^2
10
1

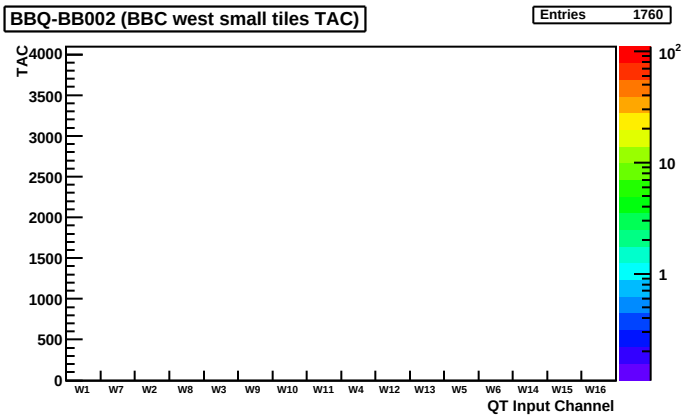

L1-TF201
Entries 110
10^2
10
1
10^{-1}
0
10
20
30
40
50
60
70
80
90
100
TOF total mult

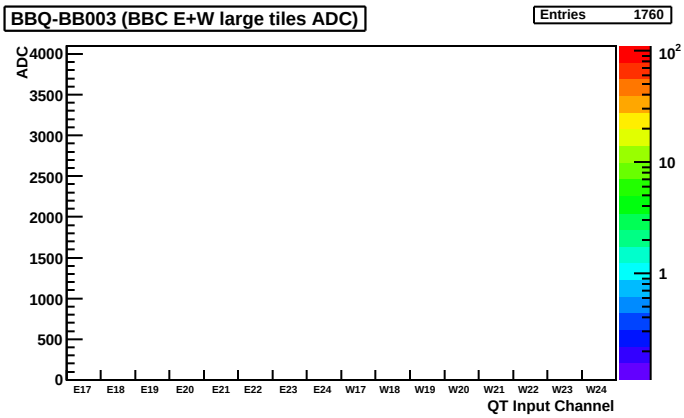

L1-TF201
Entries 660
Threshold bits
1
0
110
TF001
TF002
TF003
TF004
TF005
TF006
TOF sector
10^2
10
1

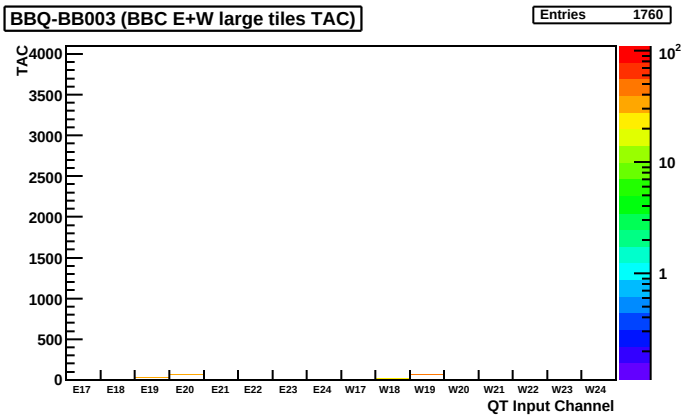

BBQ-BB001 (BBC east small tiles ADC)
Entries 1760
ADC
QT Input Channel

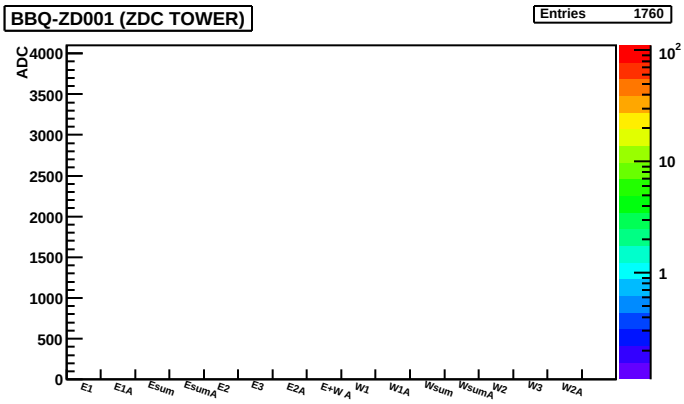

BBQ-BB001 (BBC east small tiles TAC)
Entries 1760
TAC
QT Input Channel

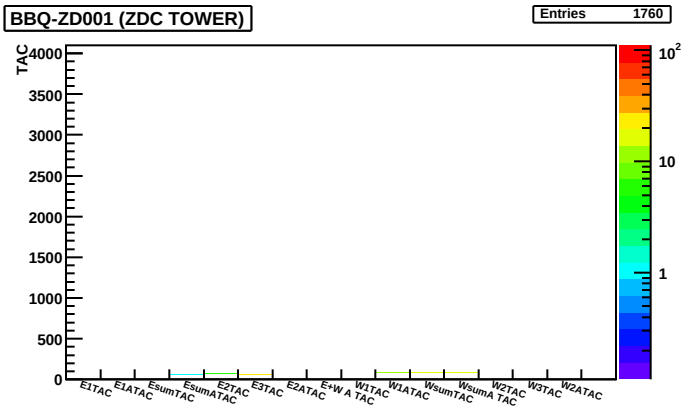

BBQ-BB002 (BBC west small tiles ADC)
Entries 1760
ADC
QT Input Channel

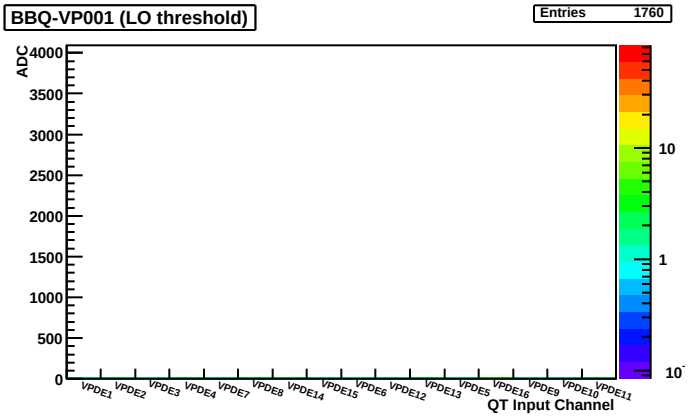

BBQ-BB002 (BBC west small tiles TAC)
Entries 1760
TAC
QT Input Channel

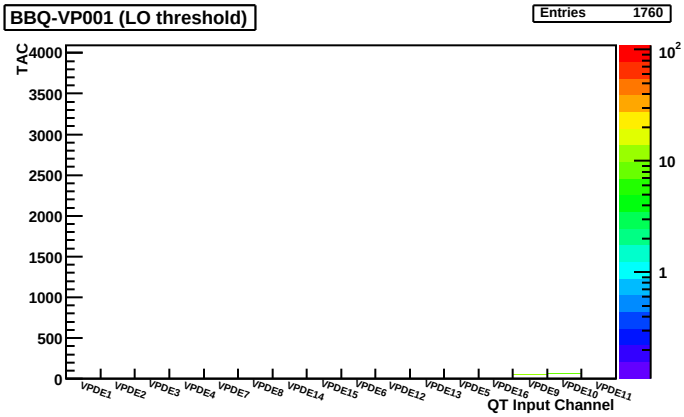

BBQ-BB003 (BBC E+W large tiles ADC)
Entries 1760
ADC
QT Input Channel

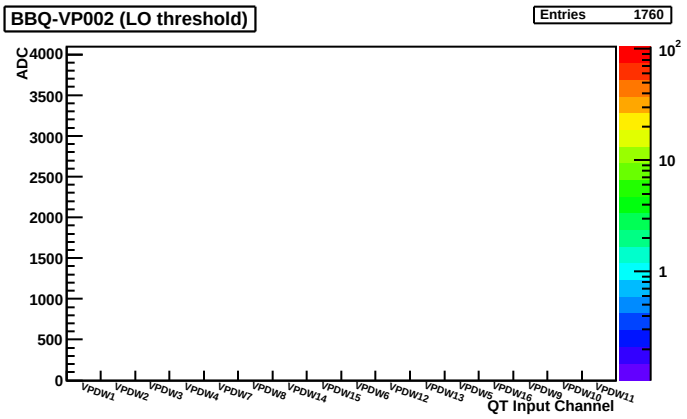

BBQ-BB003 (BBC E+W large tiles TAC)
Entries 1760
TAC
QT Input Channel

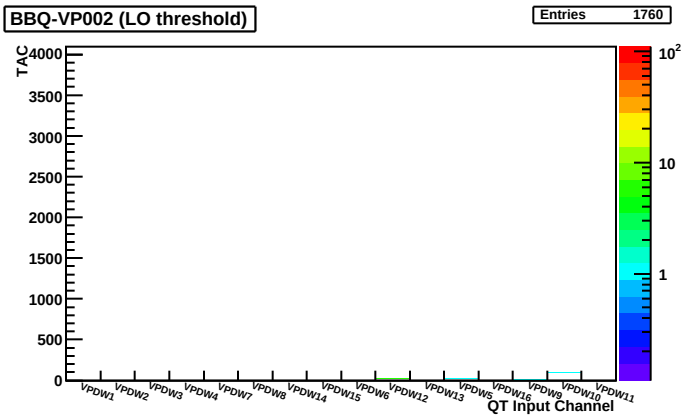

BBQ-ZD001 (ZDC TOWER)
Entries 1760
ADC

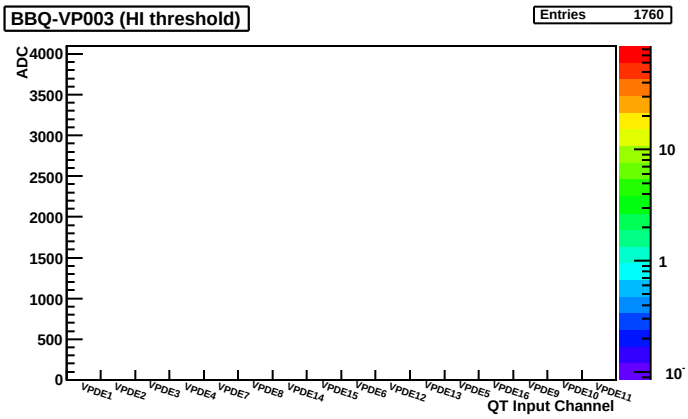

BBQ-ZD001 (ZDC TOWER)
Entries 1760
TAC

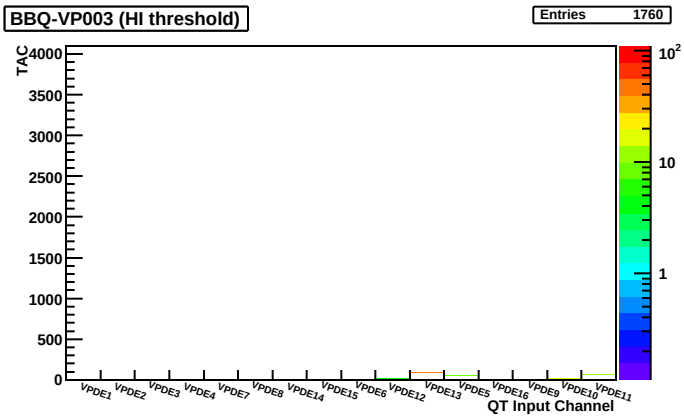

BBQ-VP001 (LO threshold)
Entries 1760
ADC
QT Input Channel

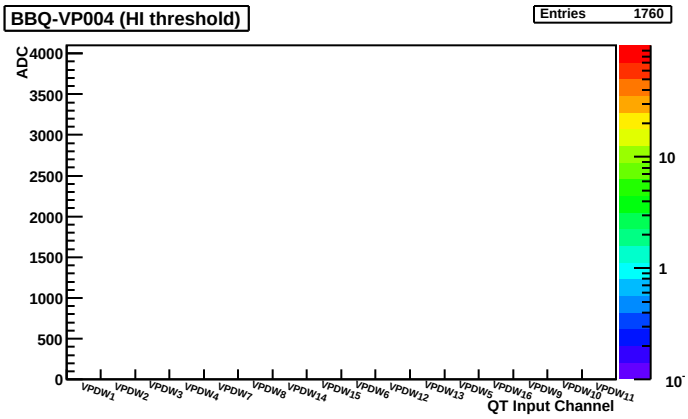

BBQ-VP001 (LO threshold)
Entries 1760
TAC
QT Input Channel

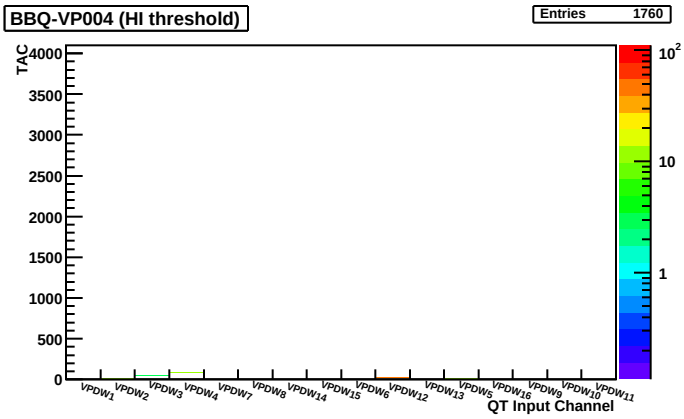

BBQ-VP002 (LO threshold)
Entries 1760
ADC
QT Input Channel

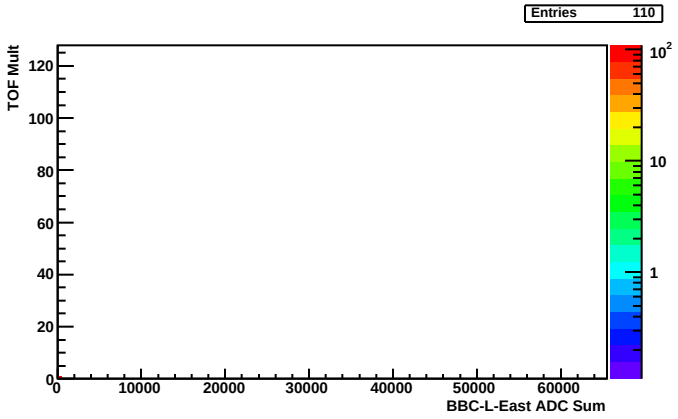

BBQ-VP002 (LO threshold)
Entries 1760
TAC
QT Input Channel

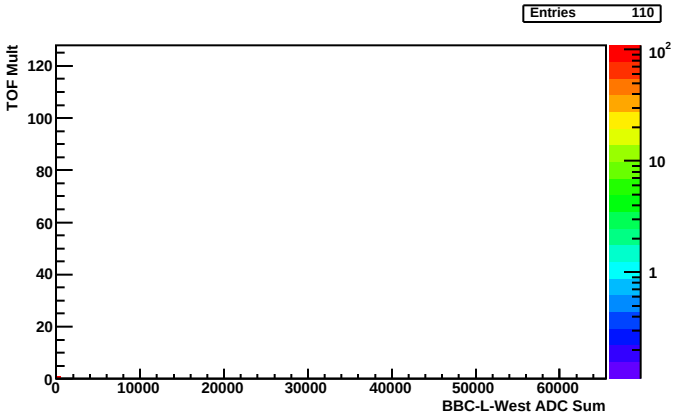

BBQ-VP003 (HI threshold)
Entries 1760
ADC
QT Input Channel

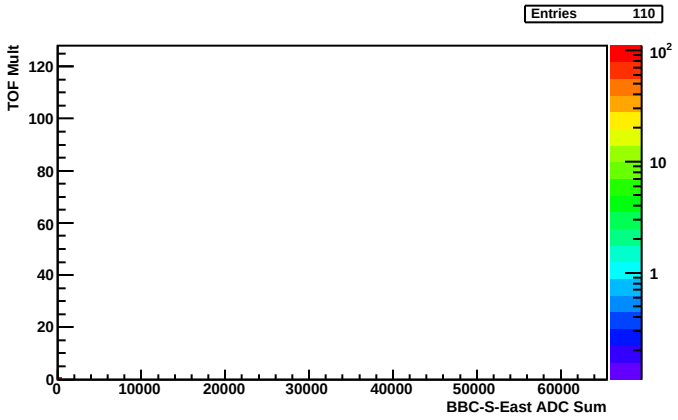

BBQ-VP003 (HI threshold)
Entries 1760
TAC
QT Input Channel

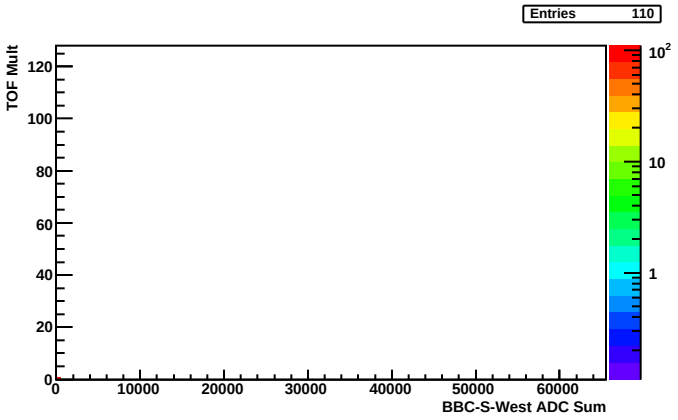

BBQ-VP004 (HI threshold)
Entries 1760
ADC
QT Input Channel

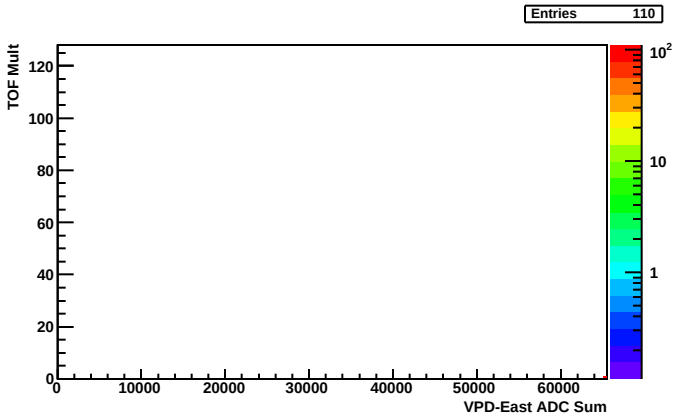

BBQ-VP004 (HI threshold)
Entries 1760
TAC
QT Input Channel

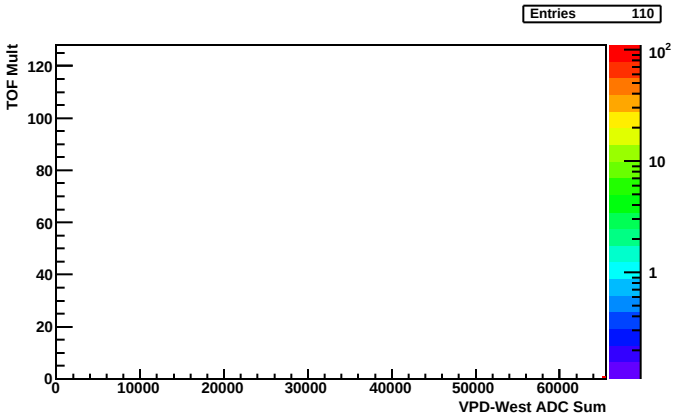

Entries 110
TOF Mult
BBC-L-East ADC Sum

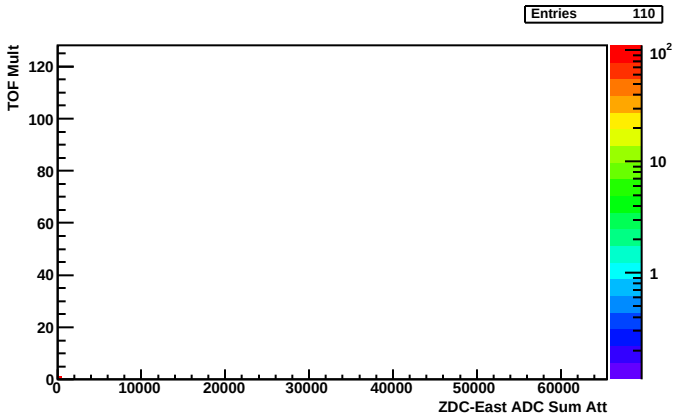

Entries 110
TOF Mult
BBC-L-West ADC Sum

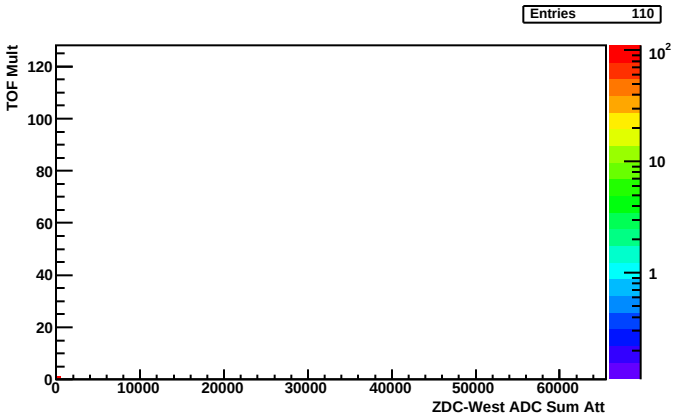

Entries 110
TOF Mult
BBC-S-East ADC Sum

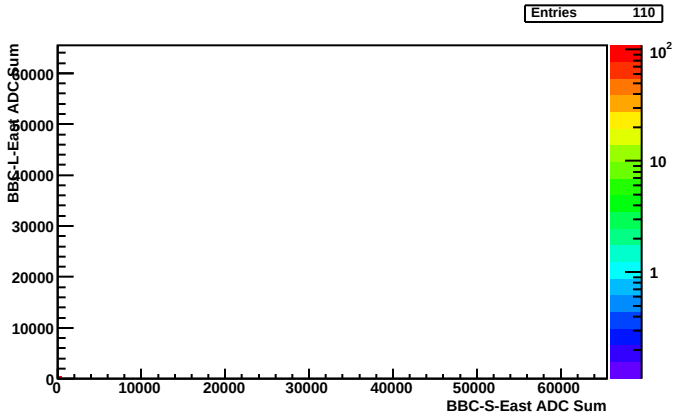

Entries 110
TOF Mult
BBC-S-West ADC Sum

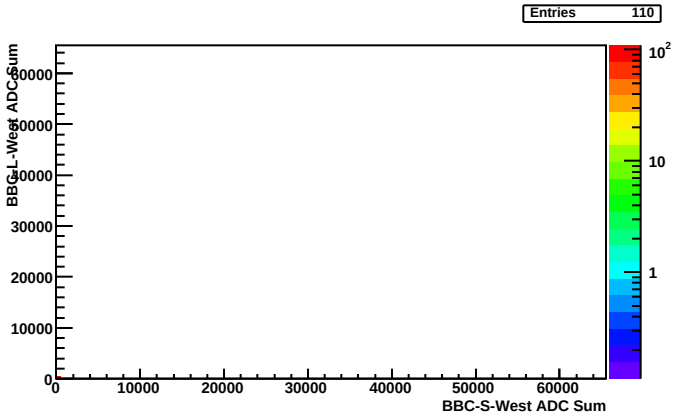

Entries 110
TOF Mult
VPD-East ADC Sum

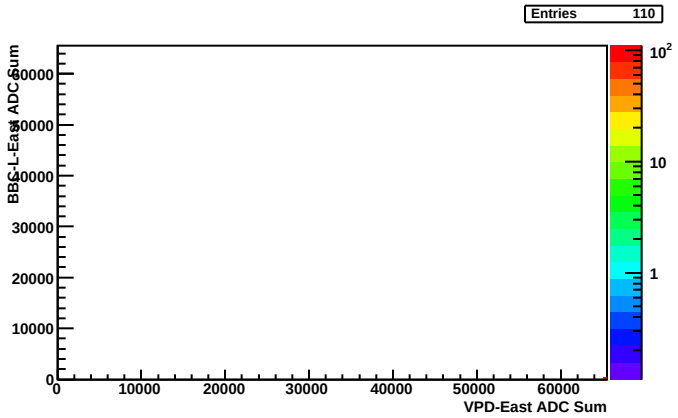

Entries 110
TOF Mult
VPD-West ADC Sum

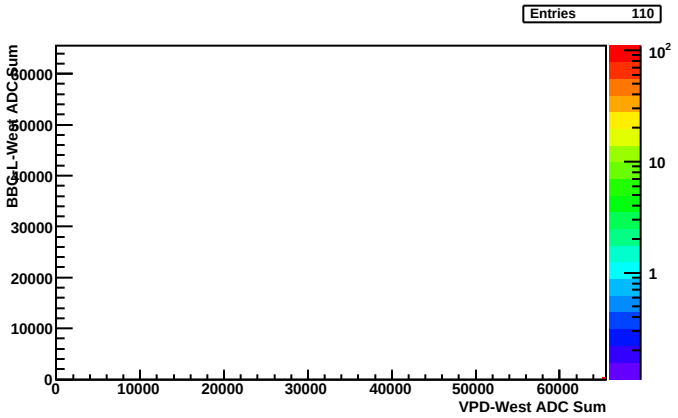

Entries 110
TOF Mult
ZDC-East ADC Sum Att

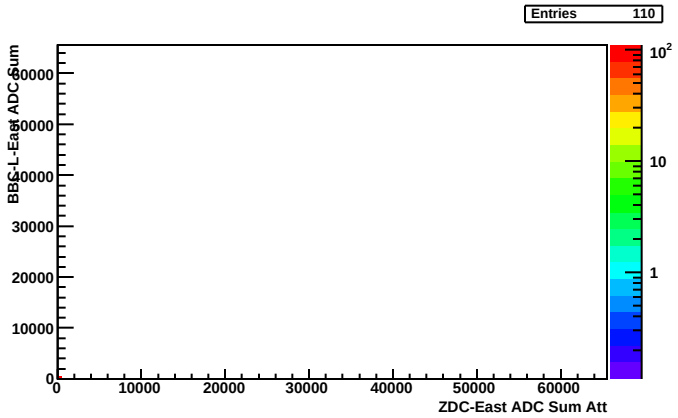

Entries 110
TOF Mult
ZDC-West ADC Sum Att

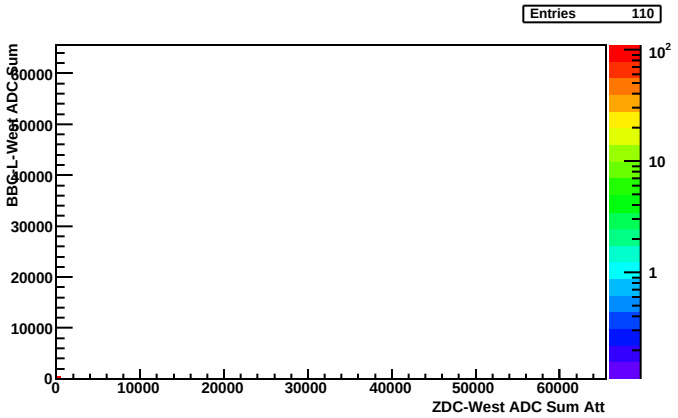

Entries 110
BBC-L-East ADC Sum
BBC-S-East ADC Sum

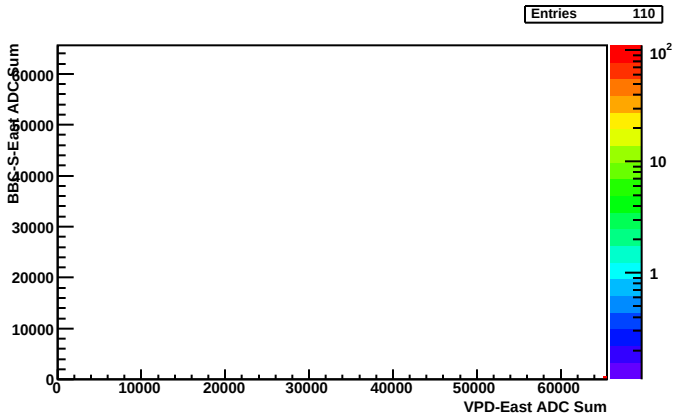

Entries 110
BBC-L-West ADC Sum
BBC-S-West ADC Sum

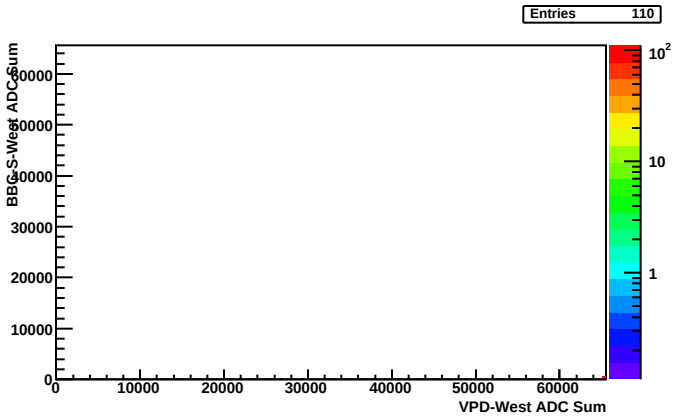

Entries 110
BBC-L-East ADC Sum
VPD-East ADC Sum

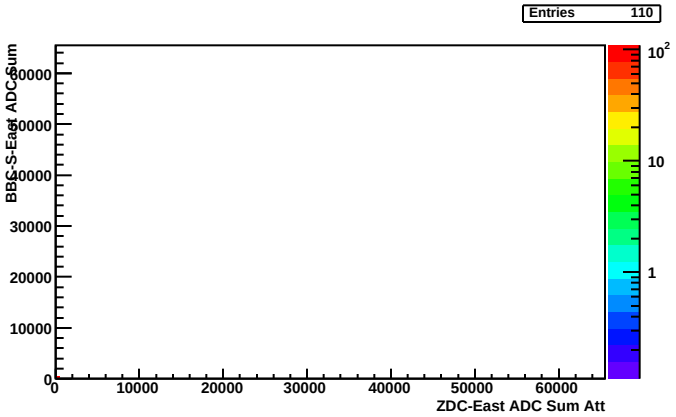

Entries 110
BBC-L-West ADC Sum
VPD-West ADC Sum

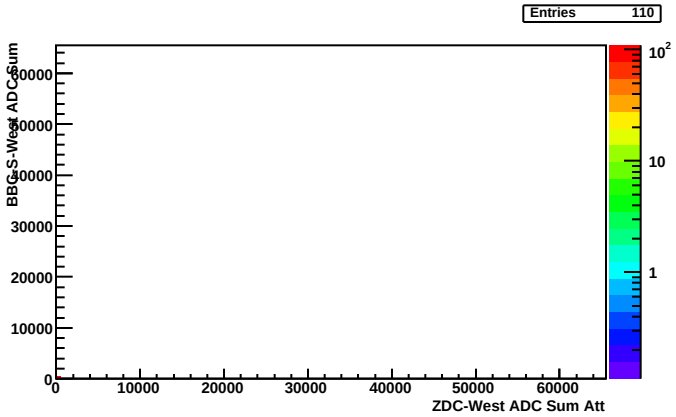

Entries 110
BBC-L-East ADC Sum
ZDC-East ADC Sum Att

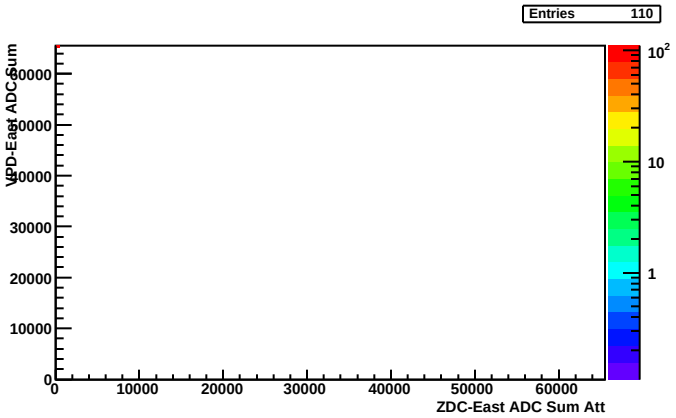

Entries 110
BBC-L-West ADC Sum
ZDC-West ADC Sum Att

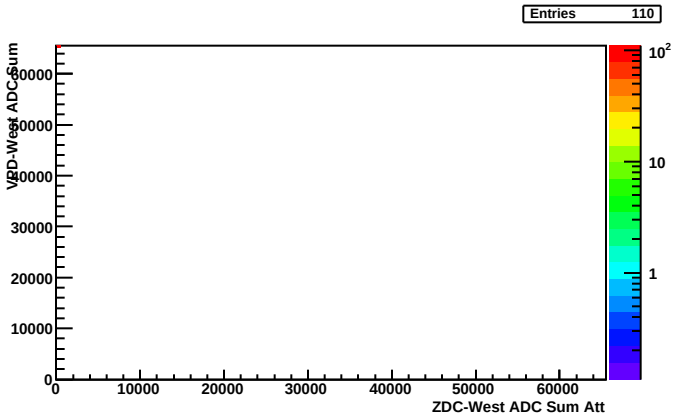

Entries 110
BBC-S-East ADC Sum
VPD-East ADC Sum

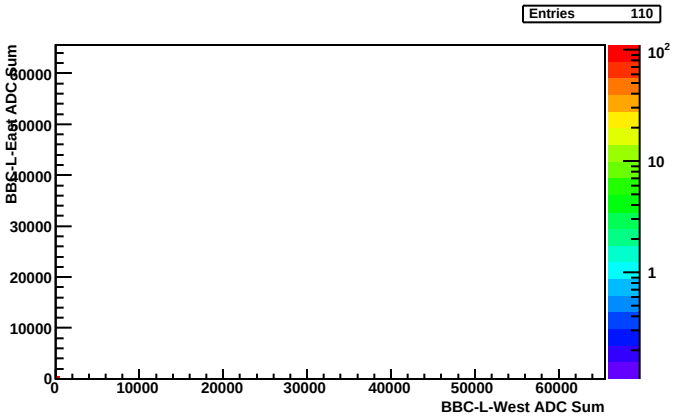

Entries 110
BBC-S-West ADC Sum
VPD-West ADC Sum


Entries 110
BBC-S-East ADC Sum
ZDC-East ADC Sum Att


Entries 110
BBC-S-West ADC Sum
ZDC-West ADC Sum Att


Entries 110
VPD-East ADC Sum
ZDC-East ADC Sum Att


Entries 110
VPD-West ADC Sum
ZDC-West ADC Sum Att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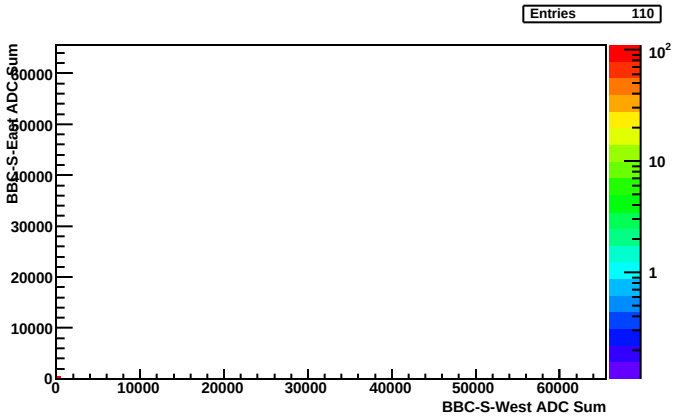
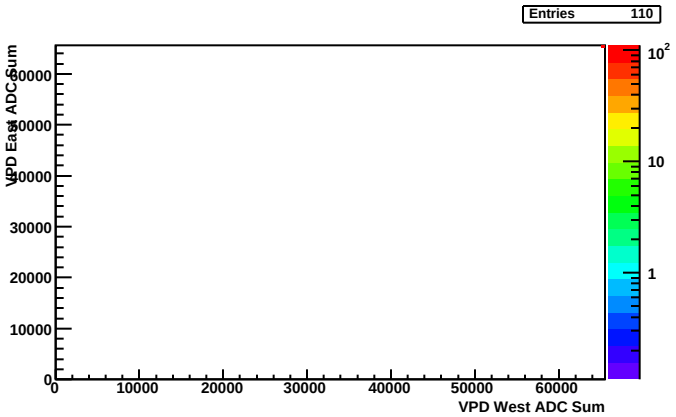
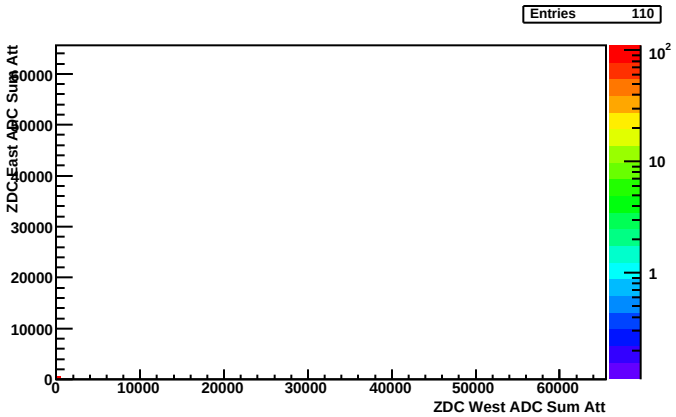
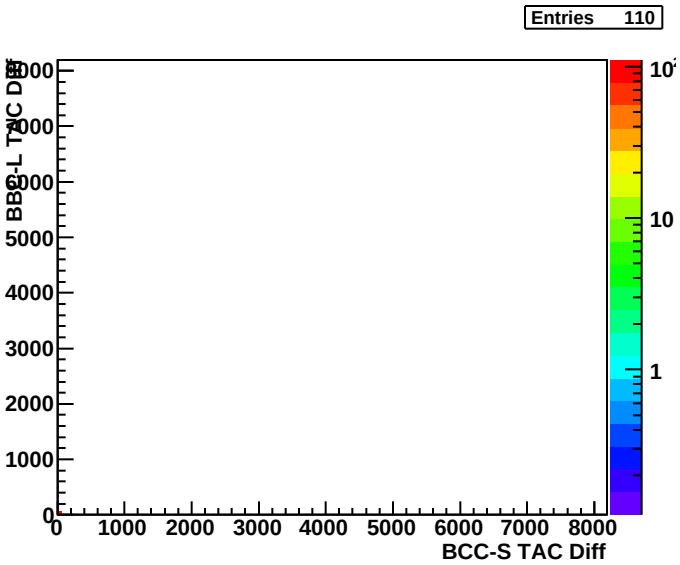
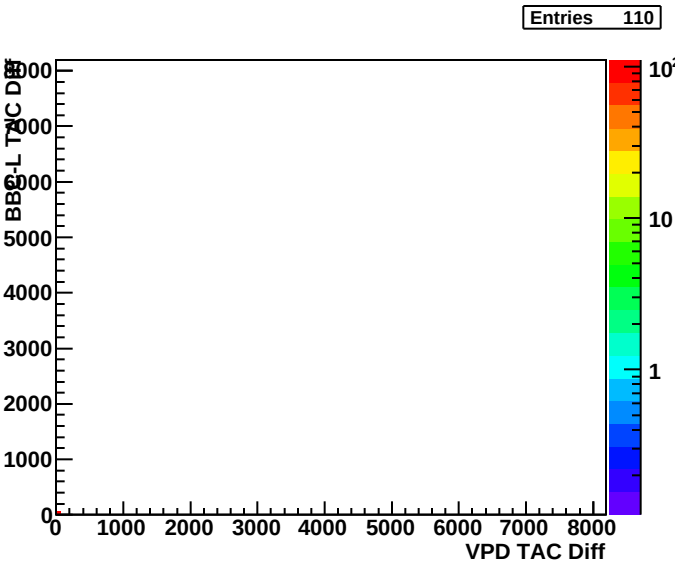
BBC-L-East ADC Sum
BBC-L-West ADC Sum

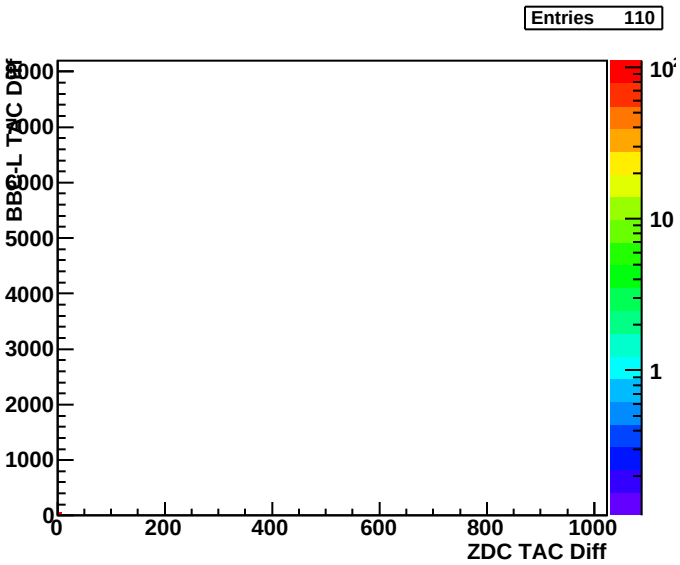

Entries 110
BBC-S-East ADC Sum
BBC-S-West ADC Sum

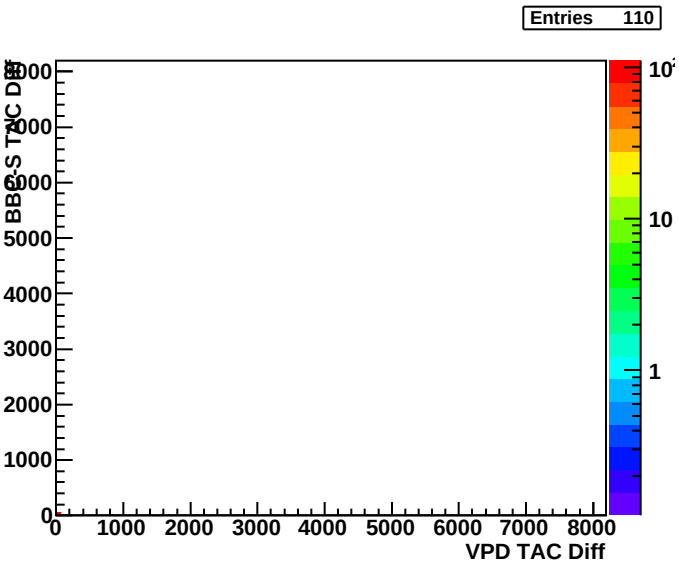

Entries 110
VPD East ADC Sum
VPD West ADC Sum

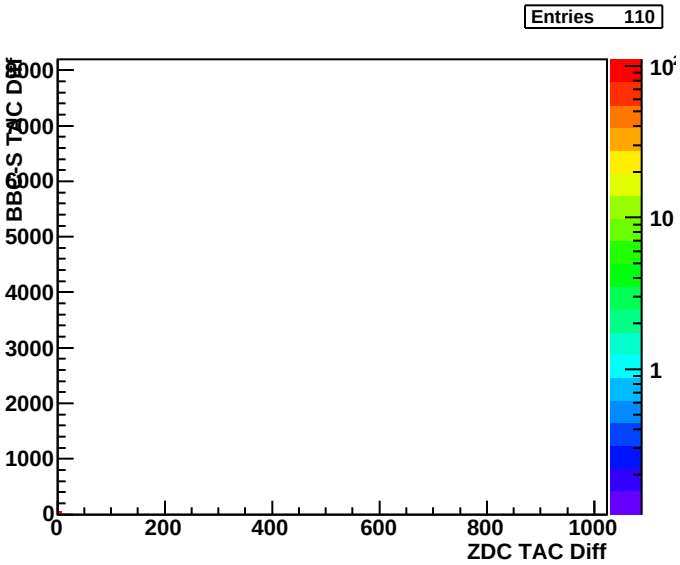

Entries 110
ZDC East ADC Sum Att
ZDC West ADC Sum Att

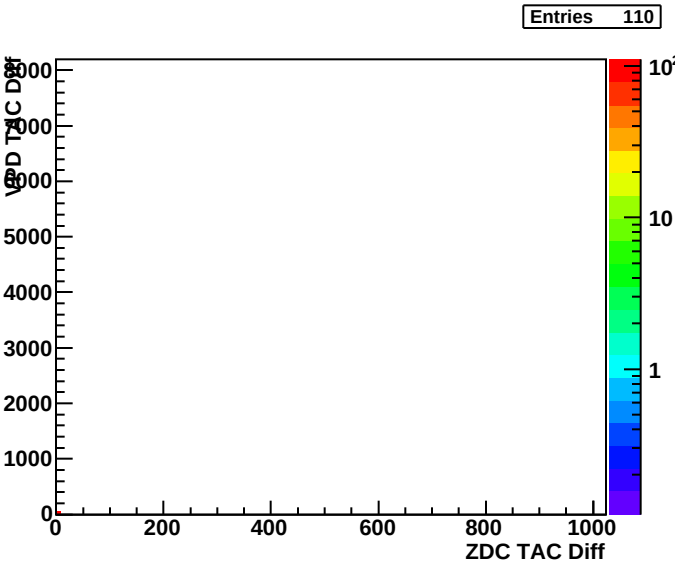

Entries 110
BBC-L TAC Diff
BCC-S TAC Diff

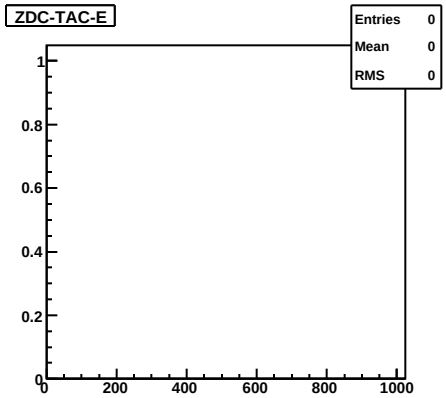

Entries 110
BBC-L TAC Diff
VPD TAC Diff

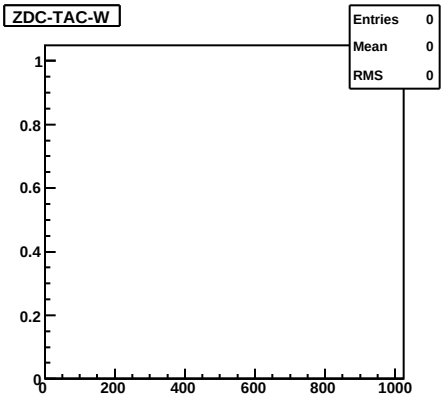

Entries 110
BBC-L TAC Diff
ZDC TAC Diff

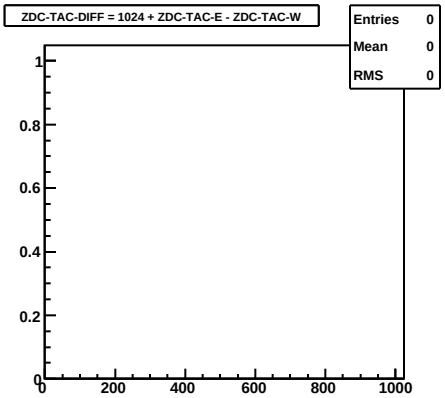

Entries 110
BBC-S TAC Diff
VPD TAC Diff

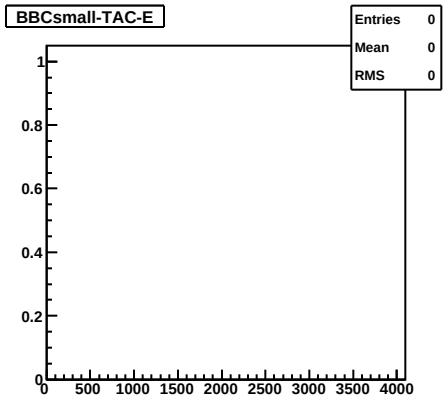

Entries 110
BBC-S TAC Diff
ZDC TAC Diff

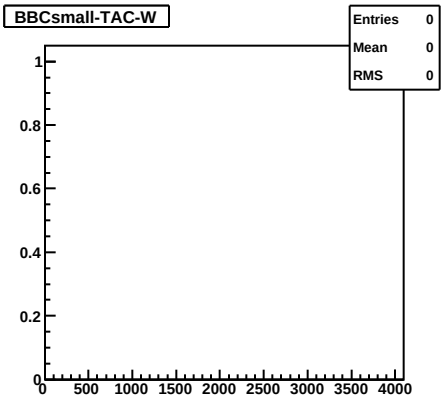

Entries 110
VPD TAC Diff
ZDC TAC Diff

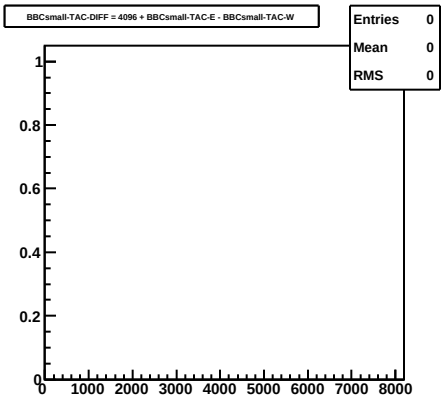

ZDC-TAC-E
Entries 0
Mean 0
RMS 0

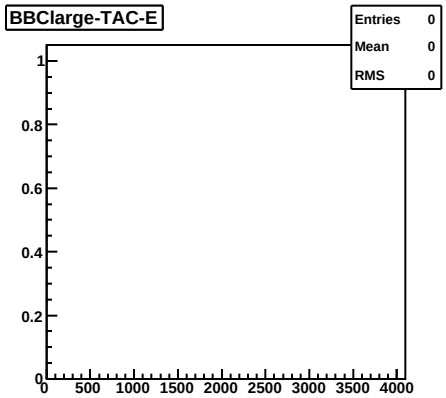

ZDC-TAC-W
Entries 0
Mean 0
RMS 0

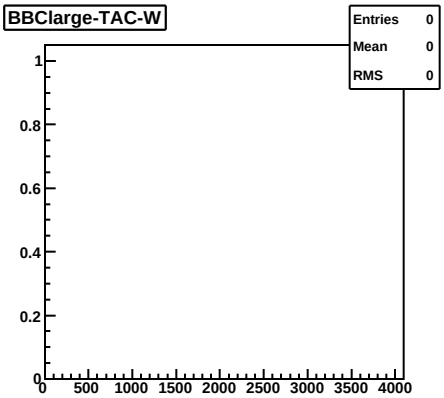

ZDC-TAC-DIFF = 1024 + ZDC-TAC-E - ZDC-TAC-W
Entries 0
Mean 0
RMS 0

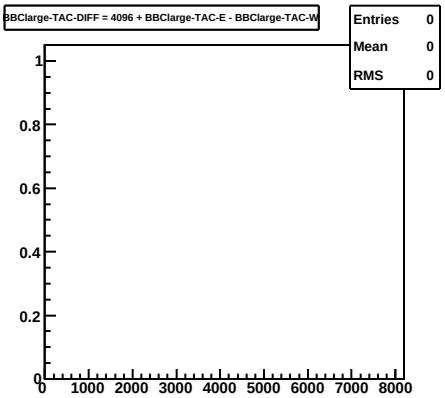

BBCsmall-TAC-E
Entries 0
Mean 0
RMS 0

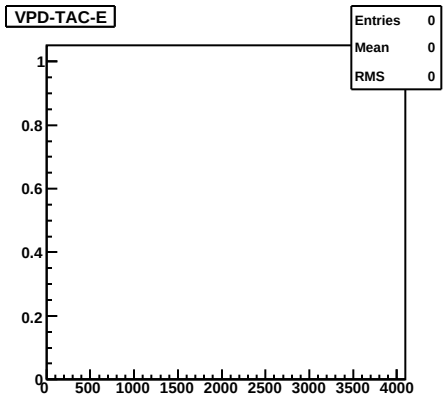

BBCsmall-TAC-W
Entries 0
Mean 0
RMS 0

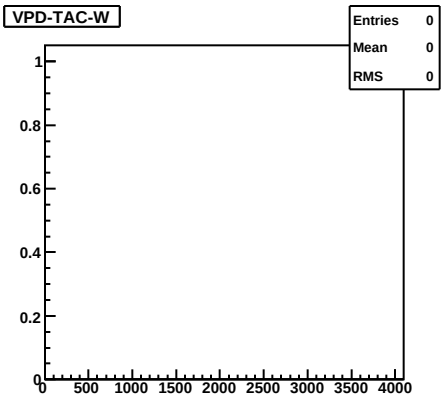

BBCsmall-TAC-DIFF = 4096 + BBCsmall-TAC-E - BBCsmall-TAC-W
Entries 0
Mean 0
RMS 0

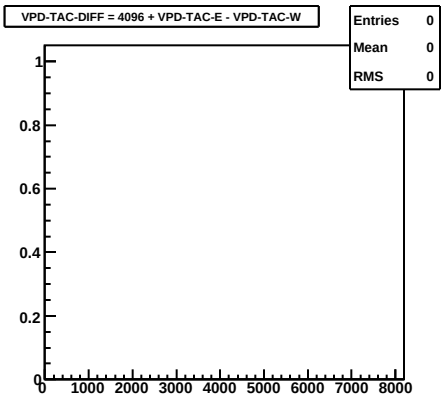

BBClarge-TAC-E
Entries 0
Mean 0
RMS 0

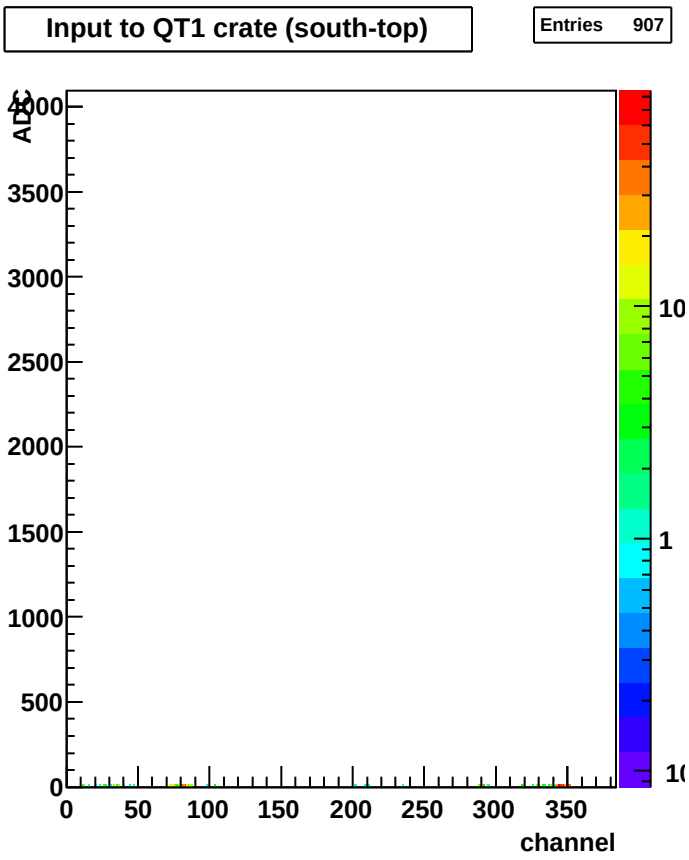

BBClarge-TAC-W
Entries 0
Mean 0
RMS 0

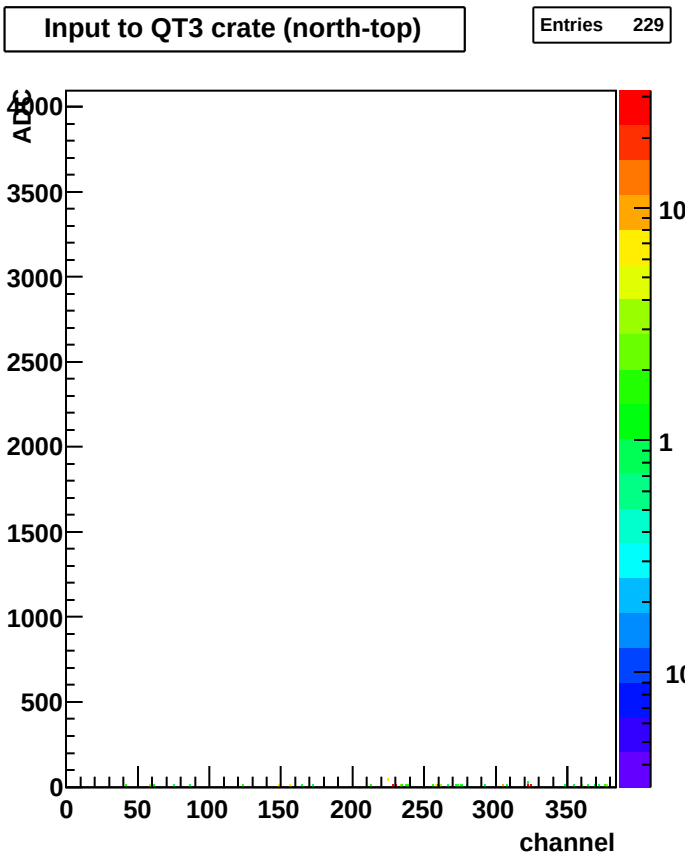

BBClarge-TAC-DIFF = 4096 + BBClarge-TAC-E - BBClarge-TAC-W
Entries 0
Mean 0
RMS 0

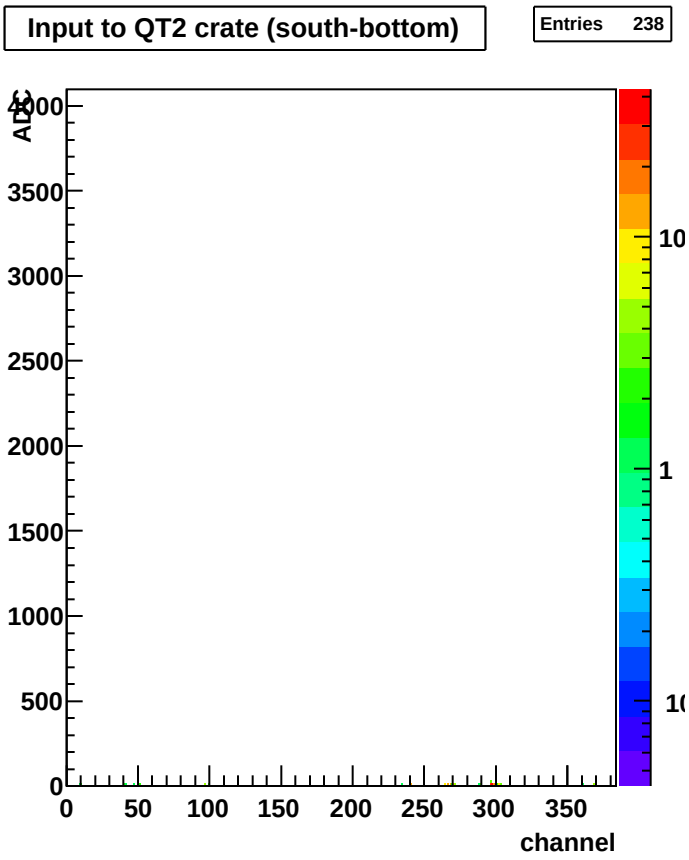

VPD-TAC-E
Entries 0
Mean 0
RMS 0

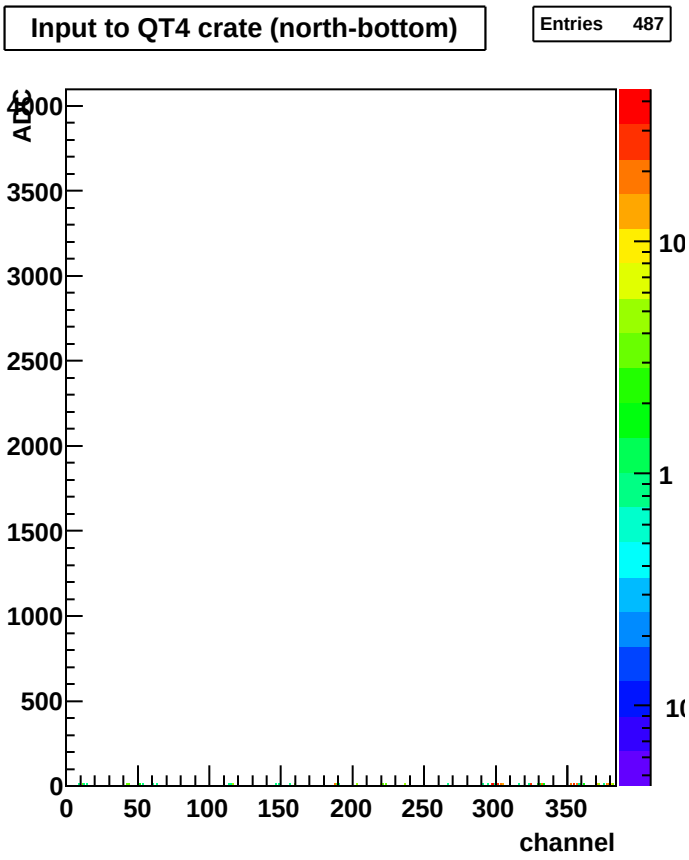

VPD-TAC-W
Entries 0
Mean 0
RMS 0

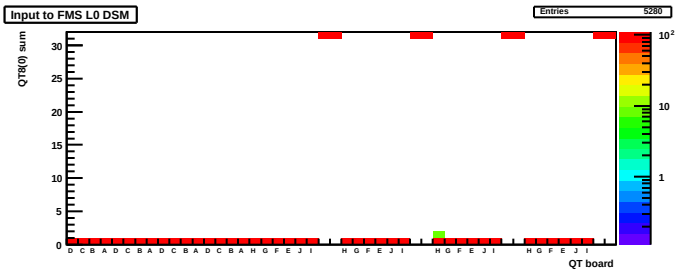

VPD-TAC-DIFF = 4096 + VPD-TAC-E - VPD-TAC-W
Entries 0
Mean 0
RMS 0

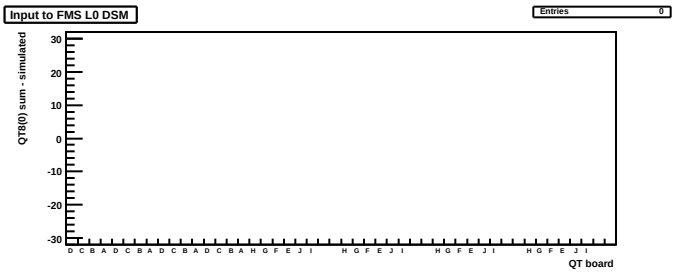

Input to QT1 crate (south-top)
Entries 907
ADC
channel

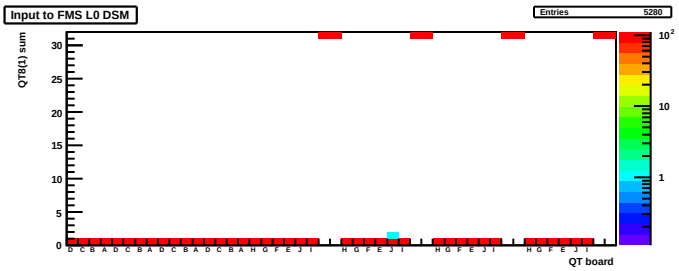

Input to QT3 crate (north-top)
Entries 229
ADC
channel

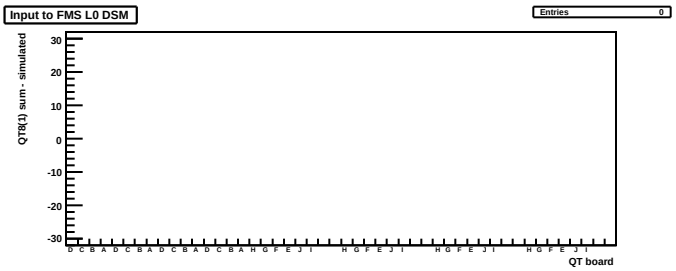

Input to QT2 crate (south-bottom)
Entries 238
ADC
channel

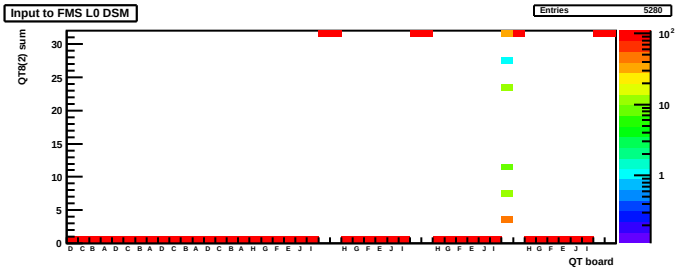

Input to QT4 crate (north-bottom)
Entries 487
ADC
channel

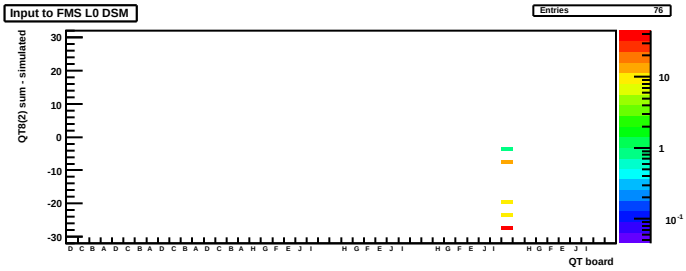

Input to FMS L0 DSM
Entries 5280
QT8(0) sum
QT board

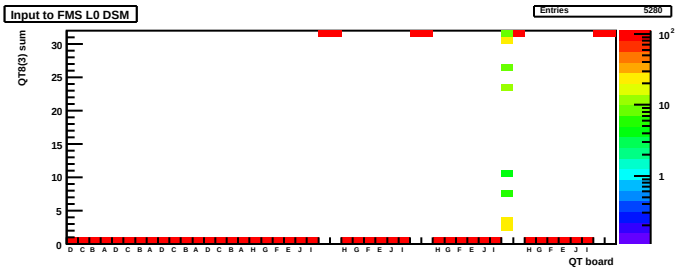

Input to FMS L0 DSM
Entries 0
QT8(0) sum - simulated
QT board

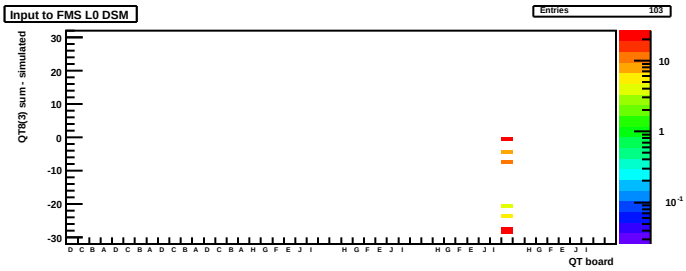

Input to FMS L0 DSM
Entries 5280
QT8(1) sum
QT board

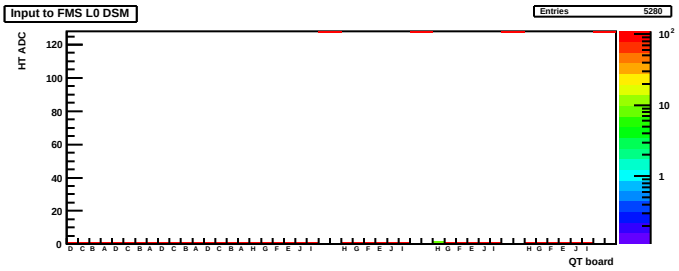

Input to FMS L0 DSM
Entries 0
QT8(1) sum - simulated
QT board

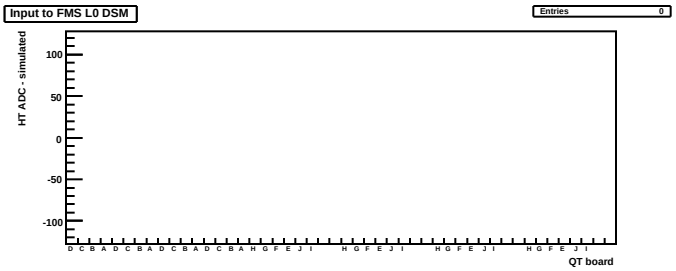

Input to FMS L0 DSM
Entries 5280
QT8(2) sum
QT board

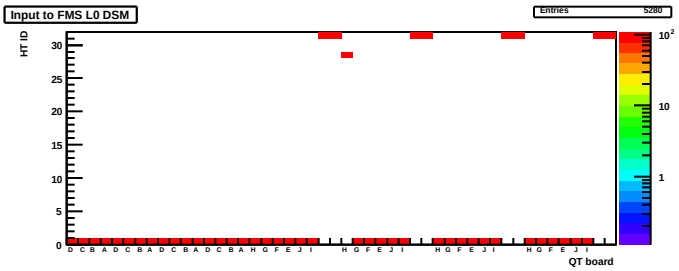

Input to FMS L0 DSM
Entries 76
QT8(2) sum - simulated
QT board

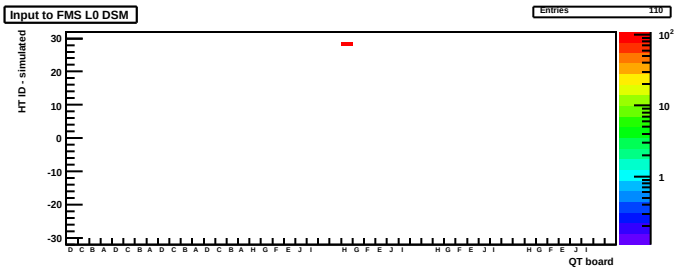

Input to FMS L0 DSM
Entries 5280
QT8(3) sum
QT board

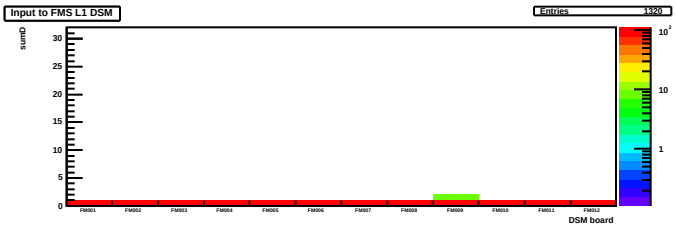

Input to FMS L0 DSM
Entries 103
QT8(3) sum - simulated
QT board

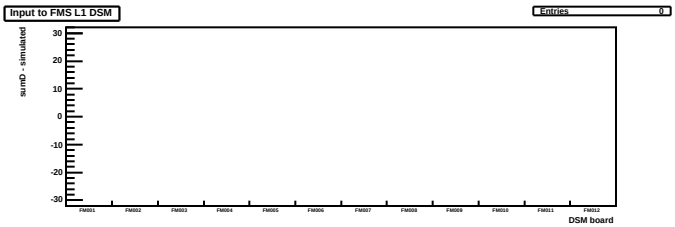

Input to FMS L0 DSM
Entries 5280
HT ADC
QT board

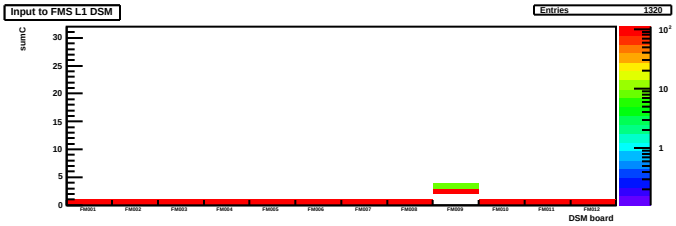

Input to FMS L0 DSM
Entries 0
HT ADC - simulated
QT board

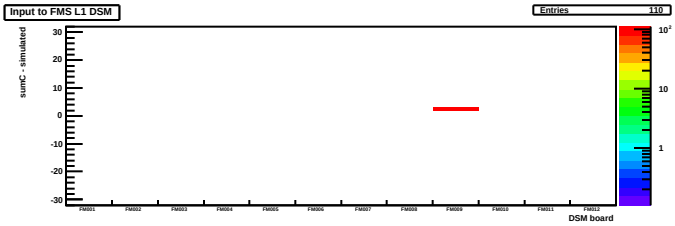

Input to FMS L0 DSM
Entries 5280
HT ID
QT board

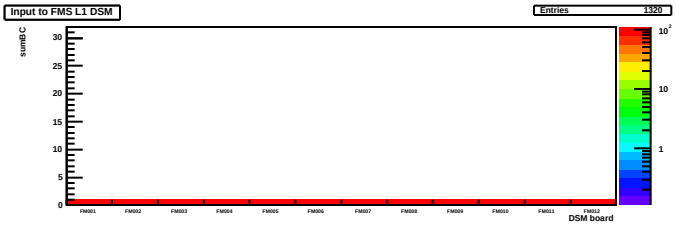

Input to FMS L0 DSM
Entries 110
HT ID - simulated
QT board

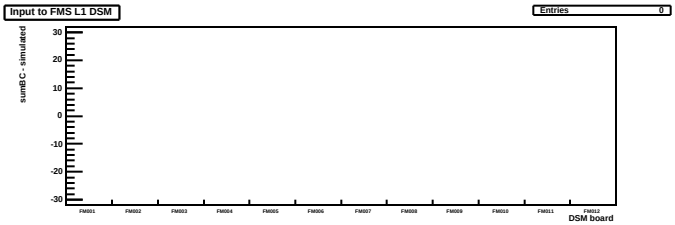

Input to FMS L1 DSM
Entries 1320
sumD
DSM board

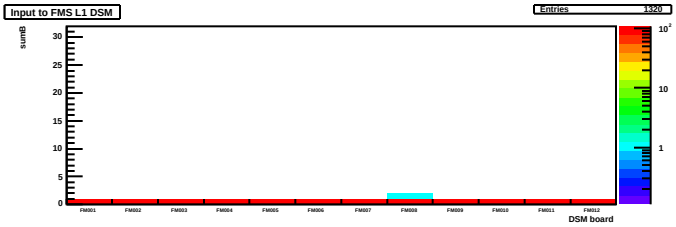

Input to FMS L1 DSM
Entries 0
sumD - simulated
DSM board

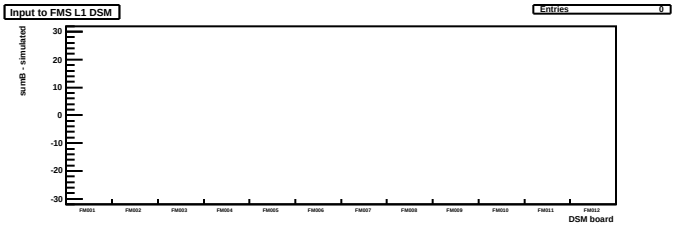

Input to FMS L1 DSM
Entries 1320
sumC
DSM board

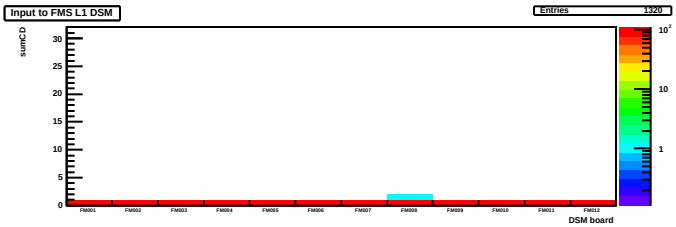

Input to FMS L1 DSM
Entries 110
sumC - simulated
DSM board

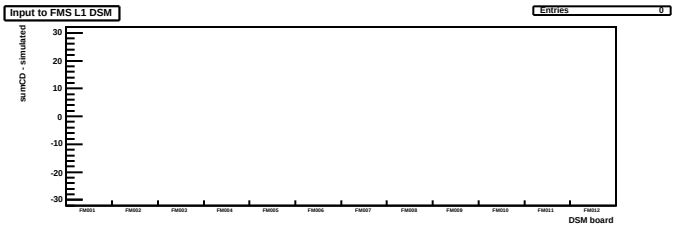

Input to FMS L1 DSM
Entries 1320
sumBC
DSM board

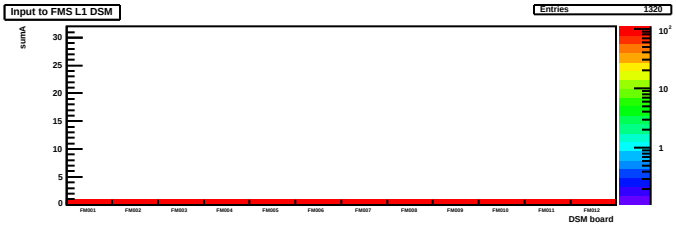

Input to FMS L1 DSM
Entries 0
sumBC - simulated
DSM board

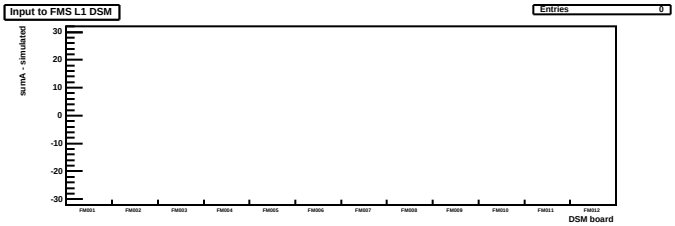

Input to FMS L1 DSM
Entries 1320
sumB
DSM board

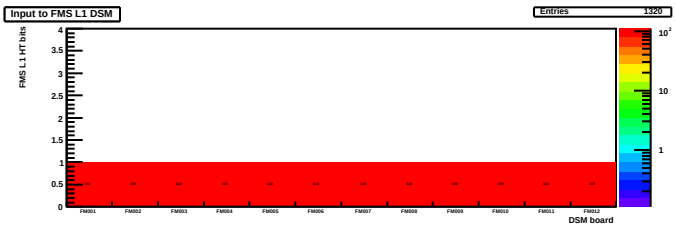

Input to FMS L1 DSM
Entries 0
sumB - simulated
DSM board

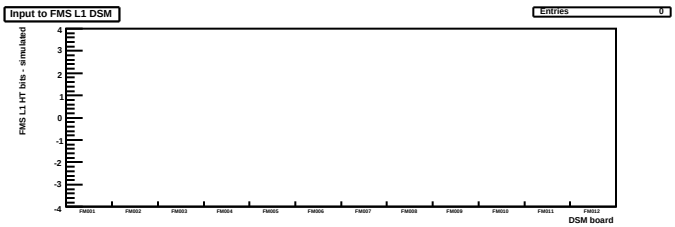

Input to FMS L1 DSM
Entries 1320
sumCD
DSM board

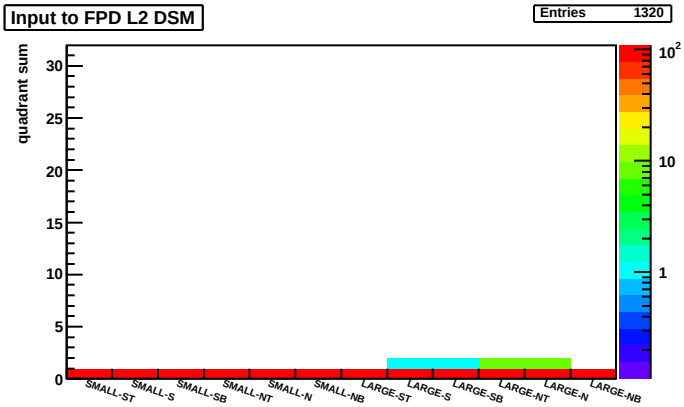

Input to FMS L1 DSM
Entries 0
sumCD - simulated
DSM board

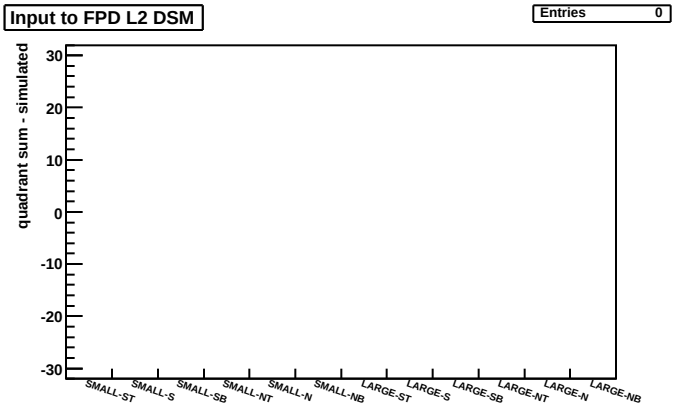

Input to FMS L1 DSM
Entries 1320
sumA
DSM board

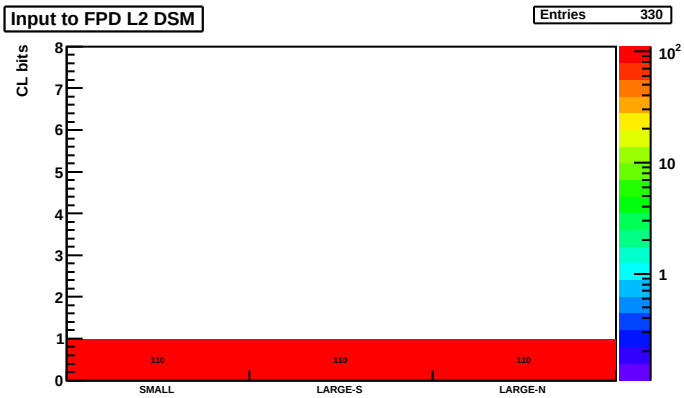

Input to FMS L1 DSM
Entries 0
sumA - simulated
DSM board

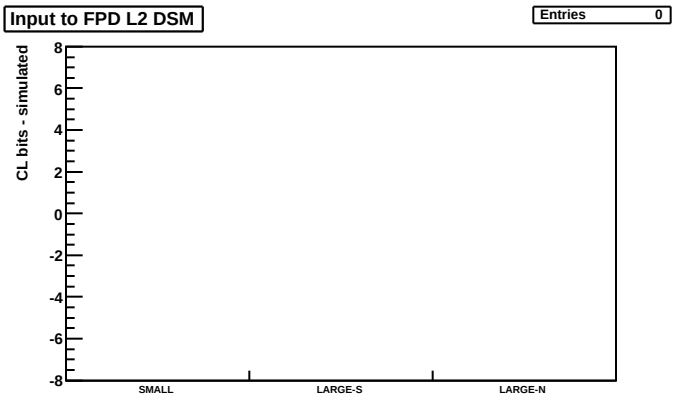

Input to FMS L1 DSM
Entries 1320
FMS L1 HT bits
DSM board

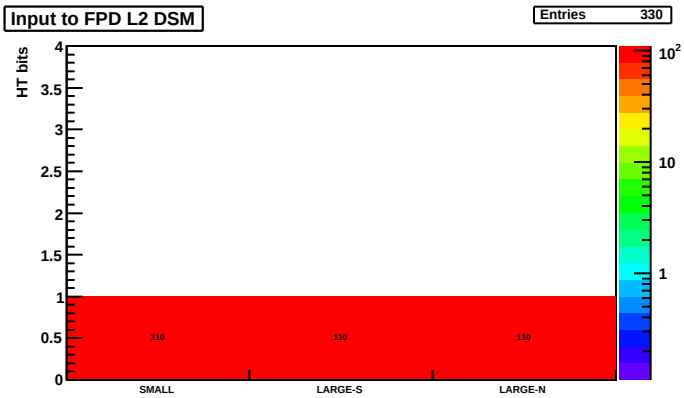

Input to FMS L1 DSM
Entries 0
FMS L1 HT bits - simulated
DSM board

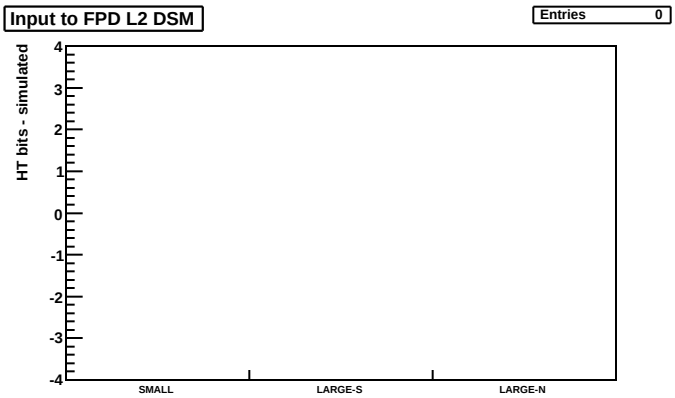

Input to FPD L2 DSM
Entries 1320
quadrant sum
SMALL-ST
SMALL-S
SMALL-SB
SMALL-NT
SMALL-N
SMALL-NB
LARGE-ST
LARGE-S
LARGE-SB
LARGE-NT
LARGE-N
LARGE-NB

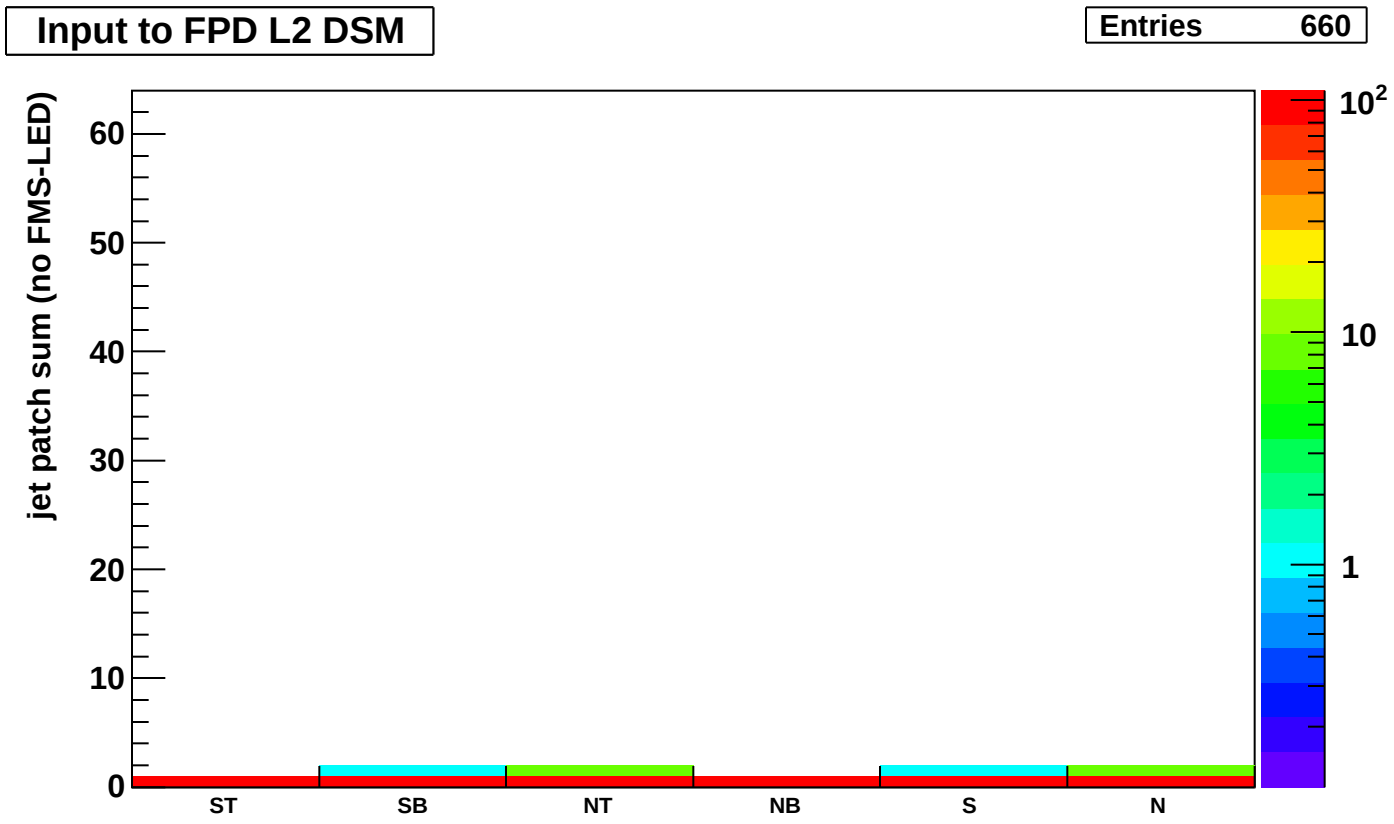

Input to FPD L2 DSM
Entries 0
quadrant sum - simulated
SMALL-ST
SMALL-S
SMALL-SB
SMALL-NT
SMALL-N
SMALL-NB
LARGE-ST
LARGE-S
LARGE-SB
LARGE-NT
LARGE-N
LARGE-NB

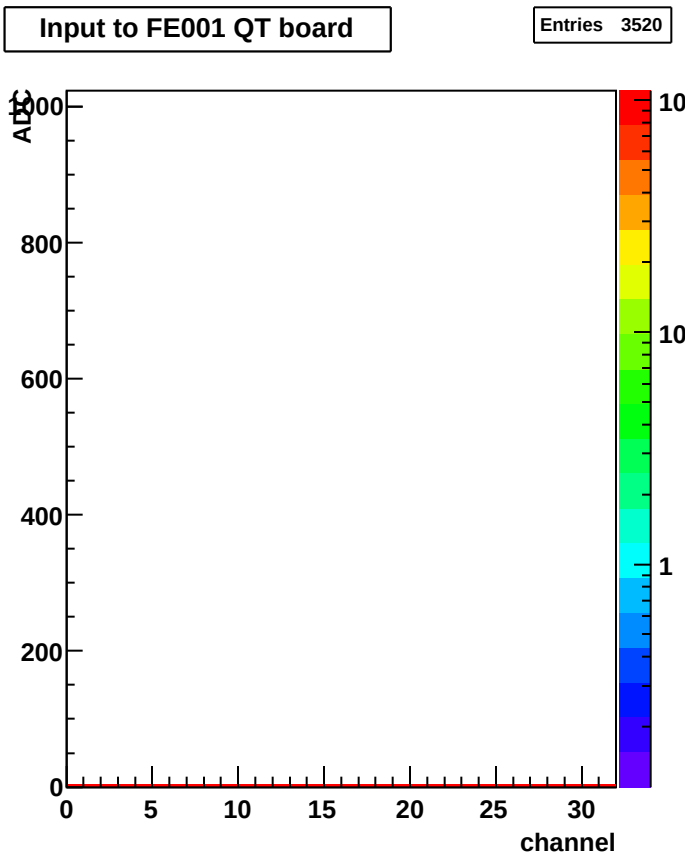

Input to FPD L2 DSM
Entries 330
CL bits
110
110
110
SMALL
LARGE-S
LARGE-N

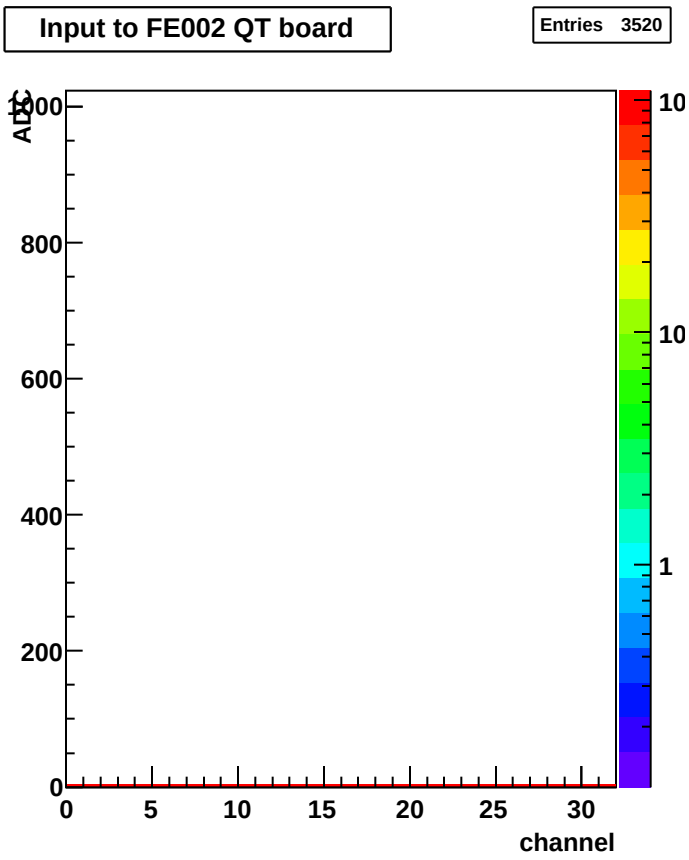

Input to FPD L2 DSM
Entries 0
CL bits - simulated
SMALL
LARGE-S
LARGE-N

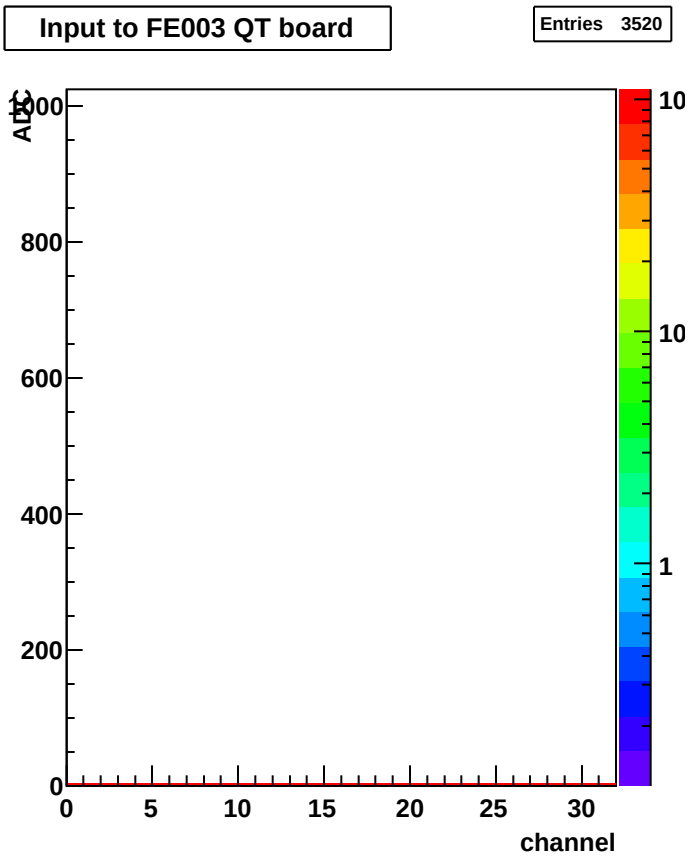

Input to FPD L2 DSM
Entries 330
HT bits
110
110
110
SMALL
LARGE-S
LARGE-N

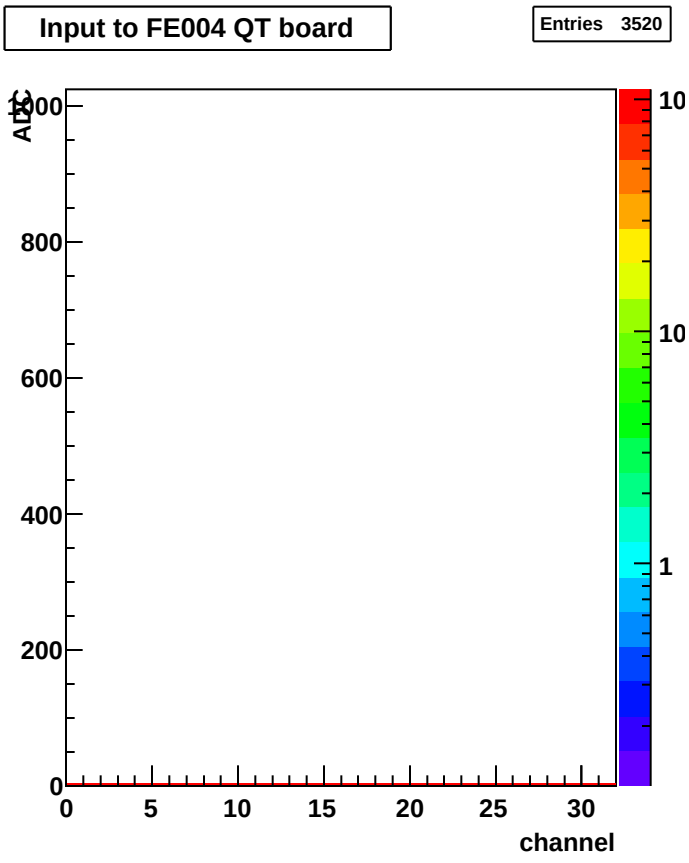

Input to FPD L2 DSM
Entries 0
HT bits - simulated
SMALL
LARGE-S
LARGE-N

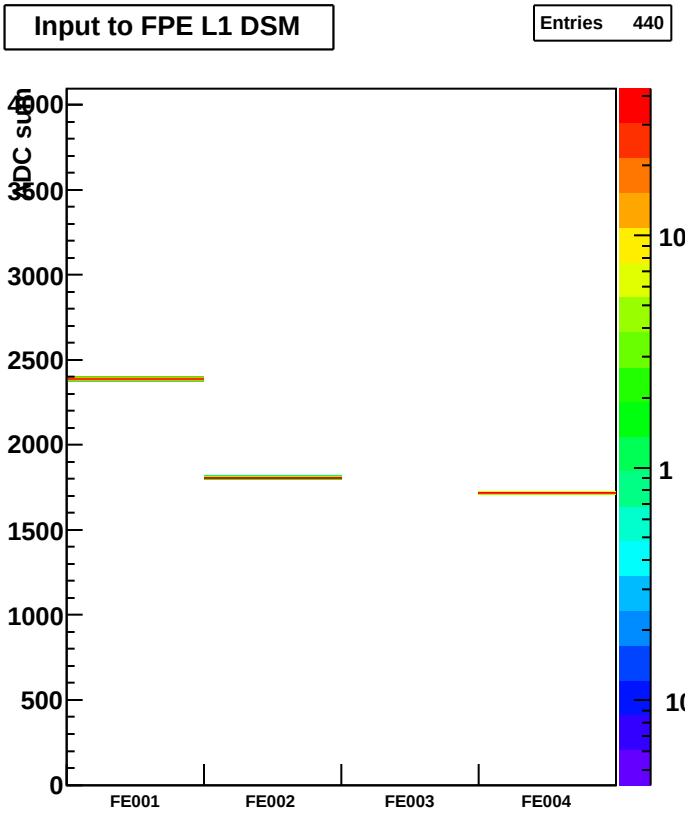

Input to FPD L2 DSM
Entries 660
jet patch sum (no FMS-LED)
0
10
20
30
40
50
60
ST
SB
NT
NB
S
N
10^2
10
1


Input to FE001 QT board
Entries 3520
ADC
channel

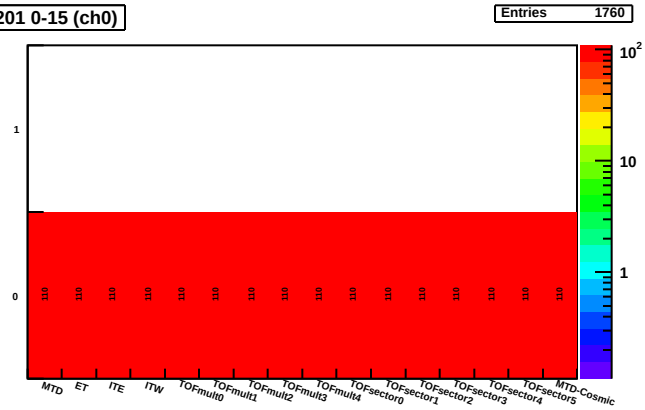

Input to FE002 QT board
Entries 3520
ADC
channel


Input to FE003 QT board
Entries 3520
ADC
channel

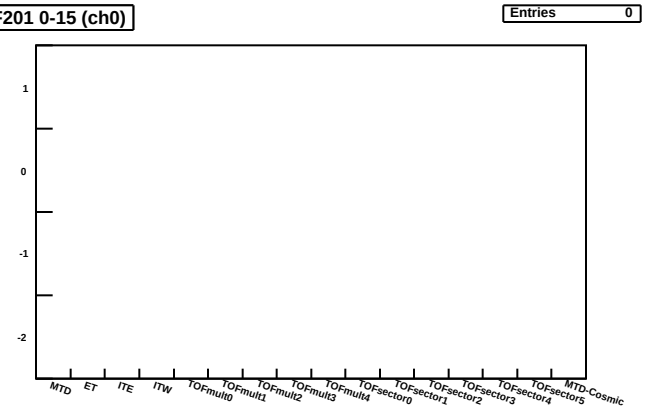

Input to FE004 QT board
Entries 3520
ADC
channel


Input to FPE L1 DSM
Entries 440
ADC sum
4000
3500
3000
2500
2000
1500
1000
500
0
FE001
FE002
FE003
FE004
10
1

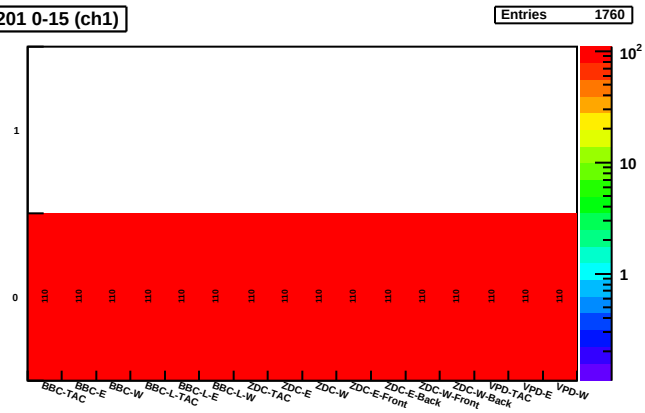
TF201 0-15 (ch0)



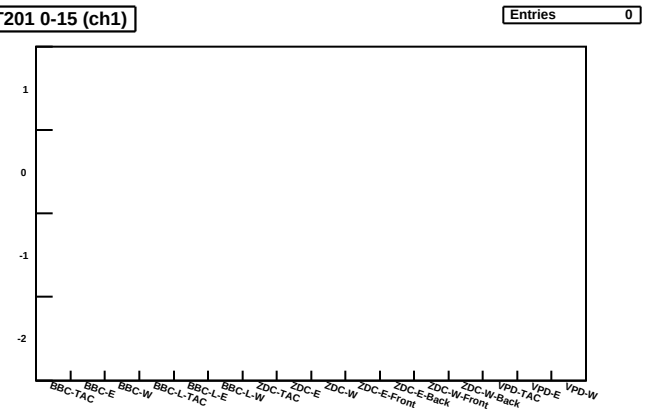
TF201 0-15 (ch0)



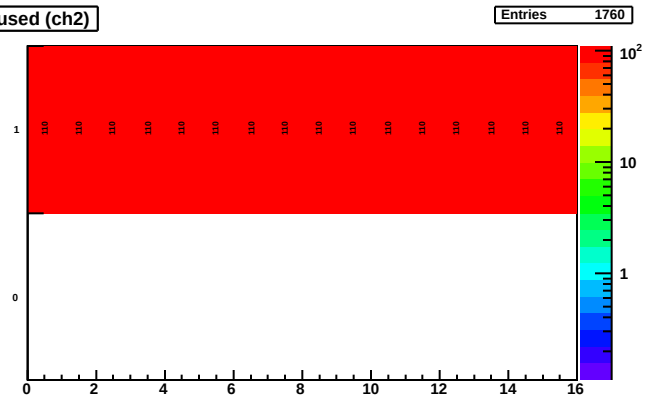
VT201 0-15 (ch1)

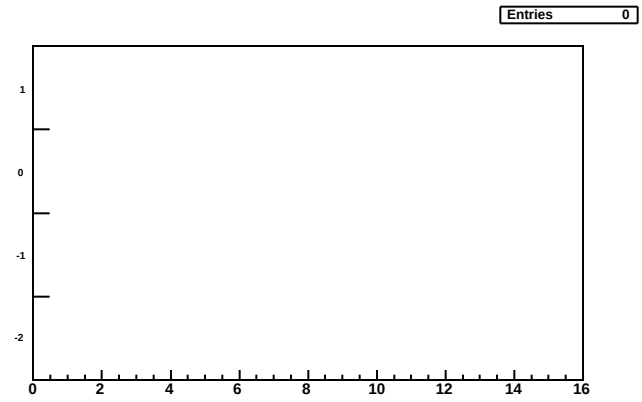


VT201 0-15 (ch1)

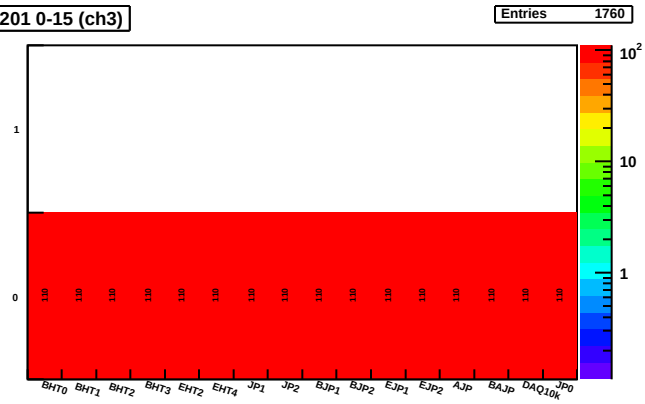


Unused (ch2)





EM201 0-15 (ch3)



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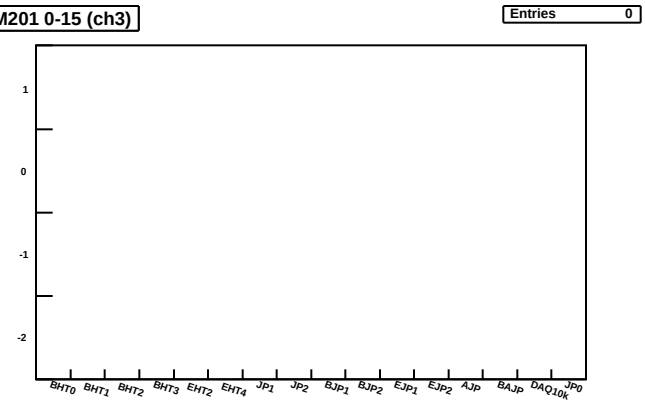
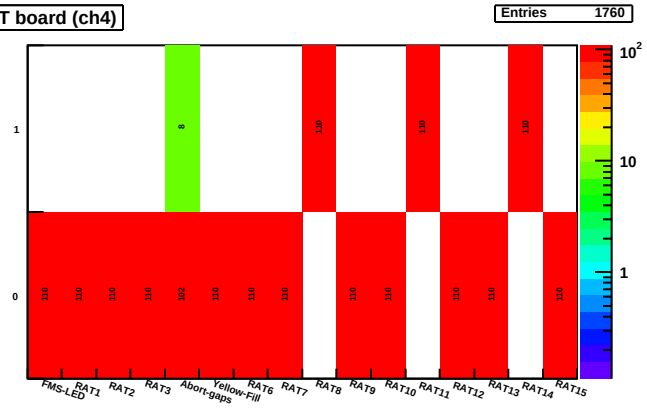
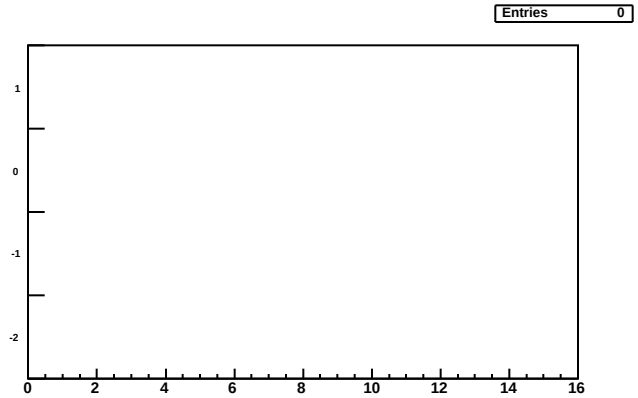
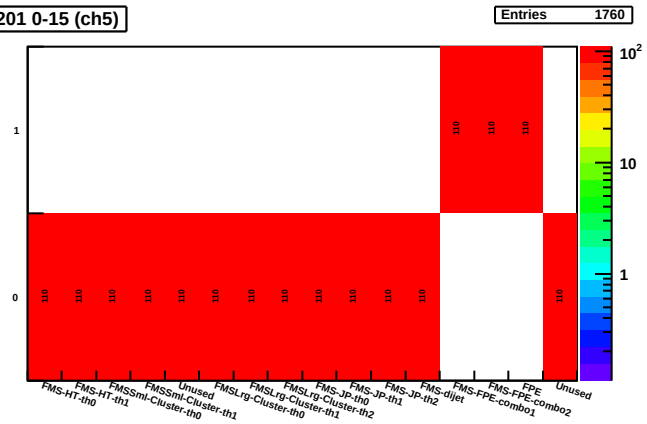


RAT board (ch4)





FP201 0-15 (ch5)



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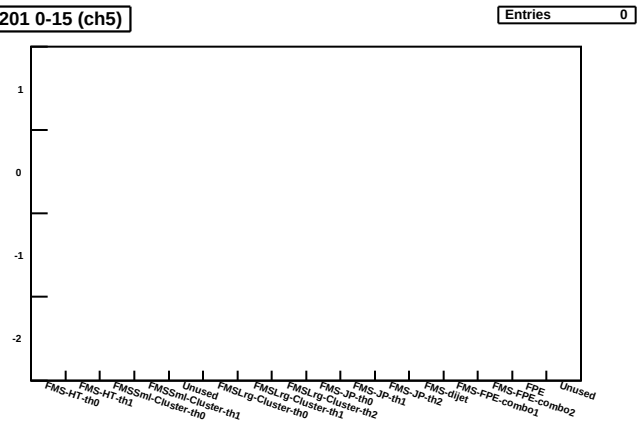

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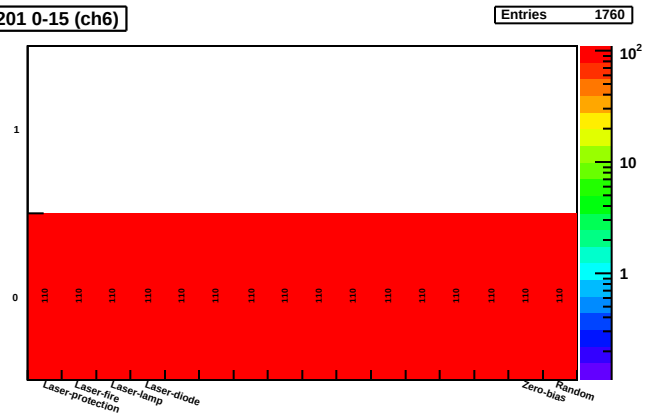

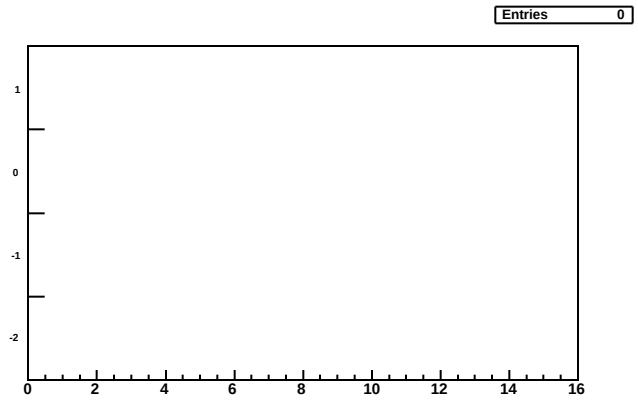
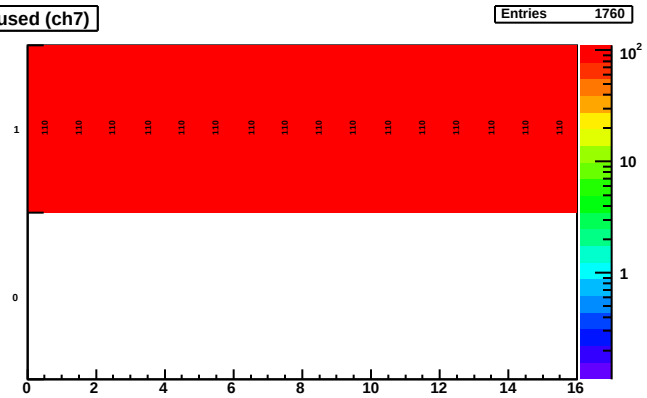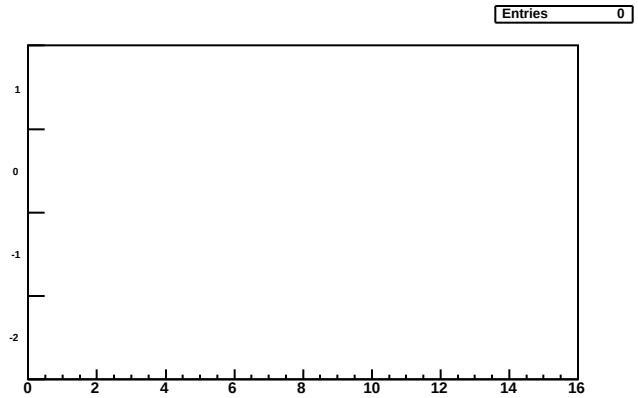
Unused (ch7)