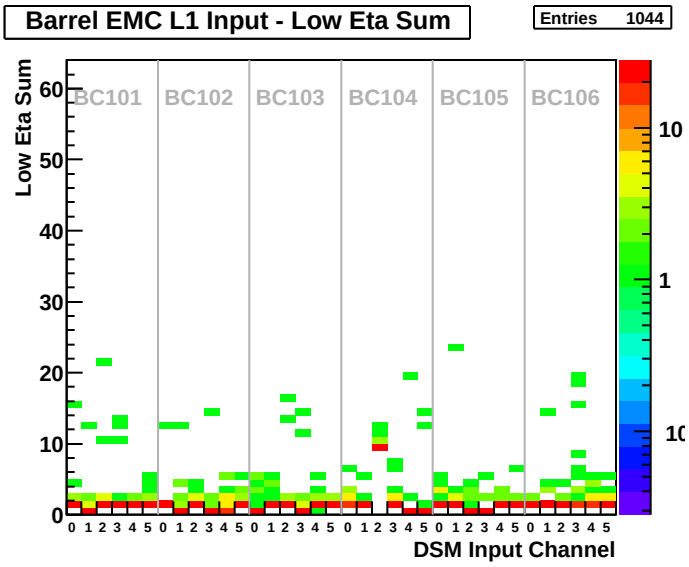
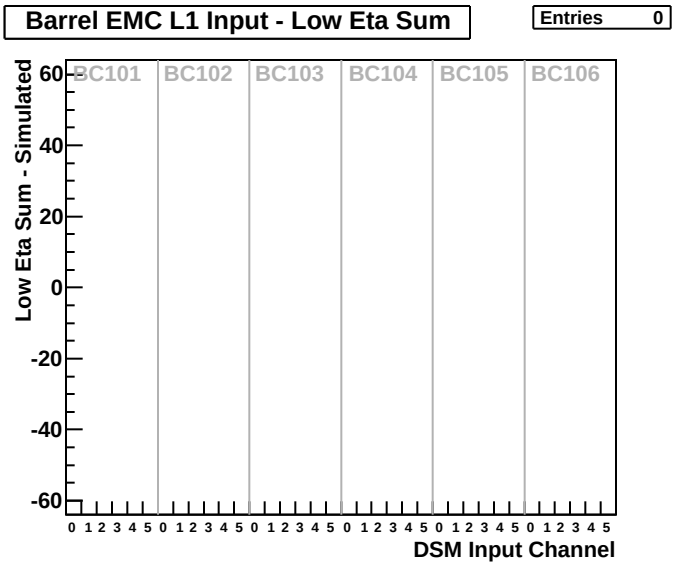
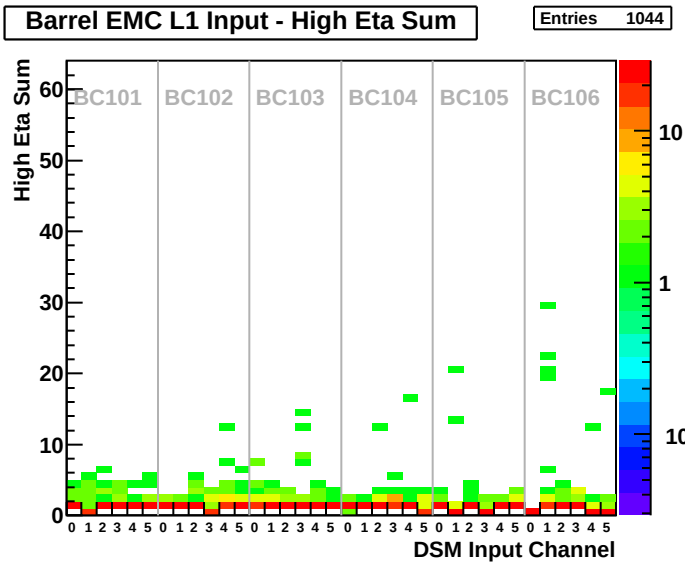
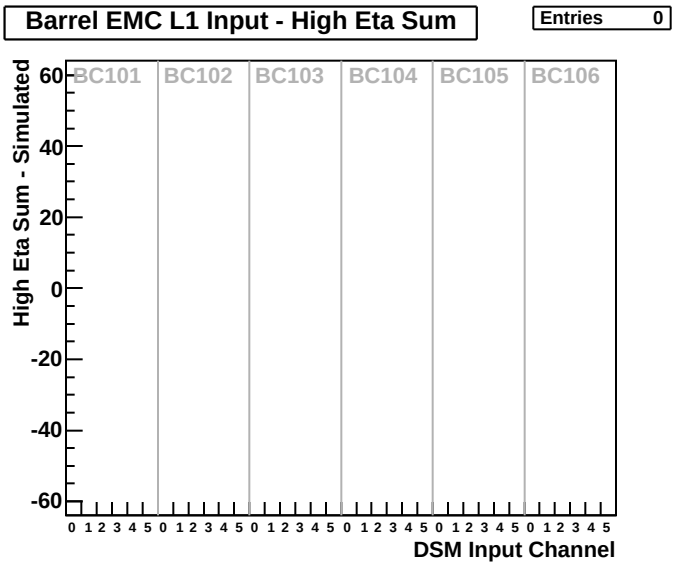
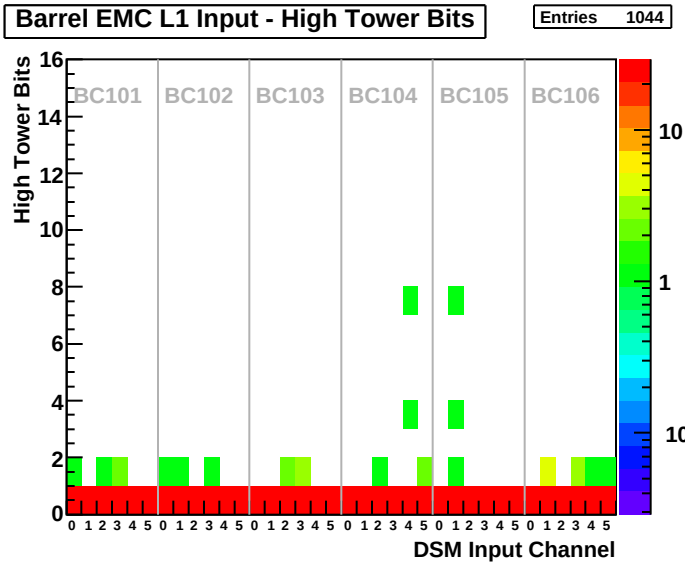
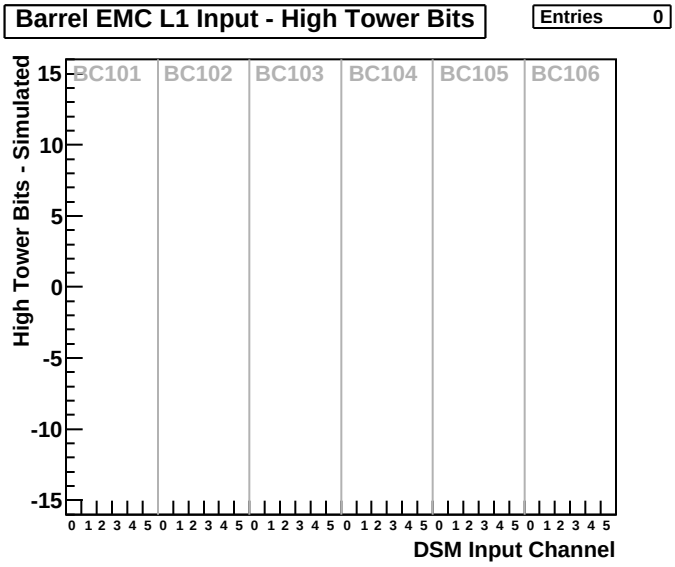

Barrel EMC L1 Input - Low Eta Sum
Entries 1044
Low Eta Sum
BC101
BC102
BC103
BC104
BC105
BC106
DSM Input Channel

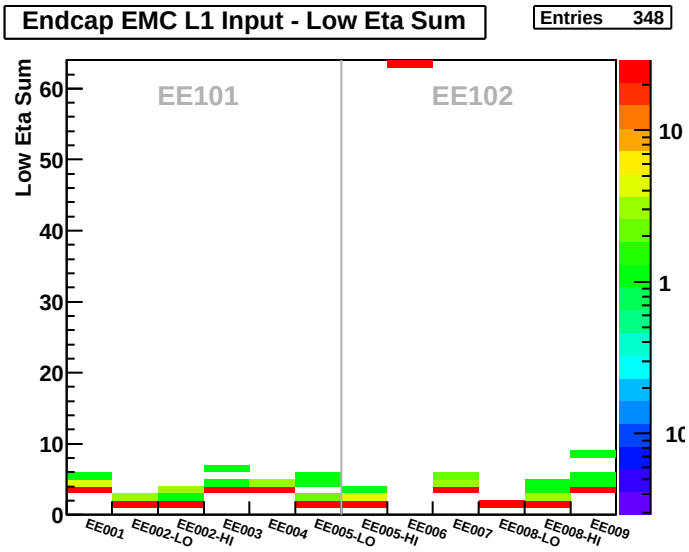

Barrel EMC L1 Input - Low Eta Sum
Entries 0
Low Eta Sum - Simulated
BC101
BC102
BC103
BC104
BC105
BC106
DSM Input Channel

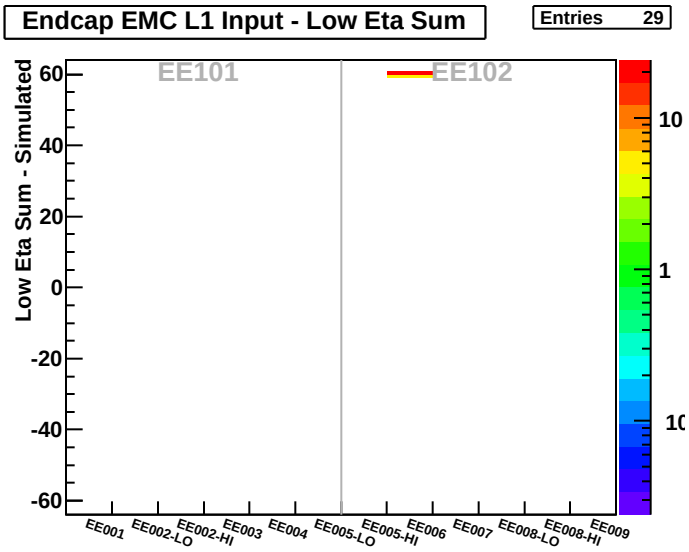

Barrel EMC L1 Input - High Eta Sum
Entries 1044
High Eta Sum
BC101
BC102
BC103
BC104
BC105
BC106
DSM Input Channel

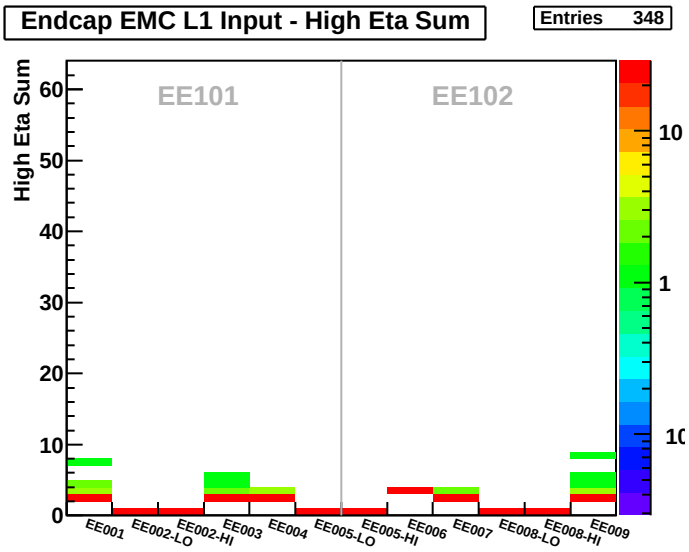

Barrel EMC L1 Input - High Eta Sum
Entries 0
High Eta Sum - Simulated
BC101
BC102
BC103
BC104
BC105
BC106
DSM Input Channel

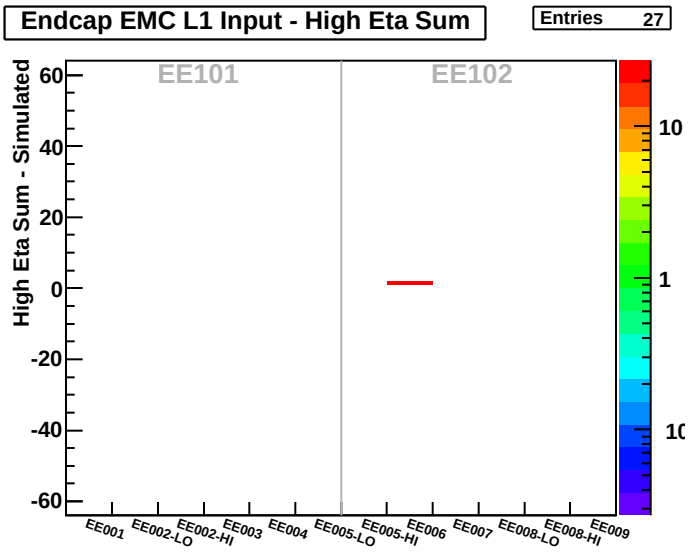

Barrel EMC L1 Input - High Tower Bits
Entries 1044
High Tower Bits
BC101
BC102
BC103
BC104
BC105
BC106
DSM Input Channel

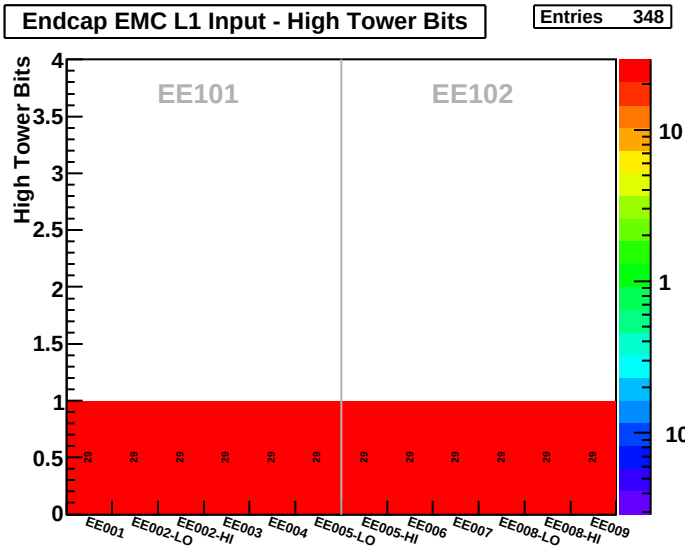

Barrel EMC L1 Input - High Tower Bits
Entries 0
High Tower Bits - Simulated
BC101
BC102
BC103
BC104
BC105
BC106
DSM Input Channel

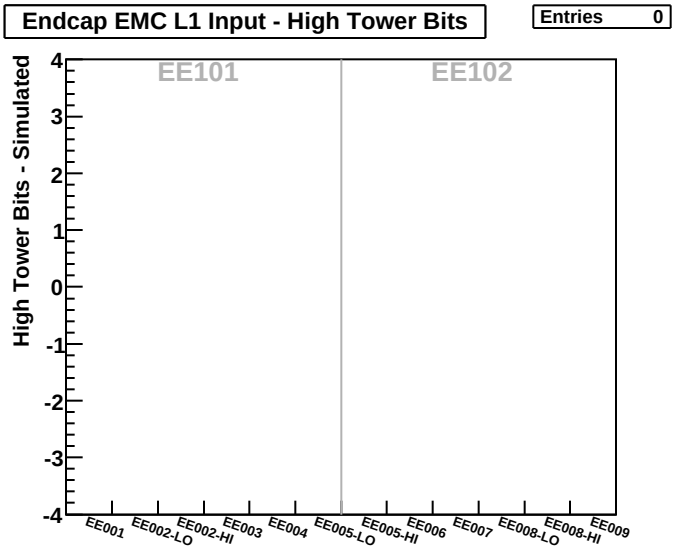

Endcap EMC L1 Input - Low Eta Sum
Entries 348
Low Eta Sum
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

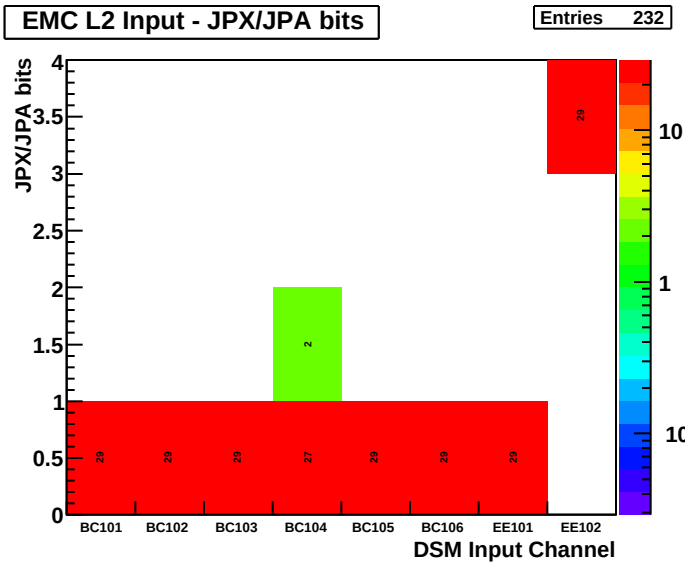

Endcap EMC L1 Input - Low Eta Sum
Entries 29
Low Eta Sum - Simulated
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

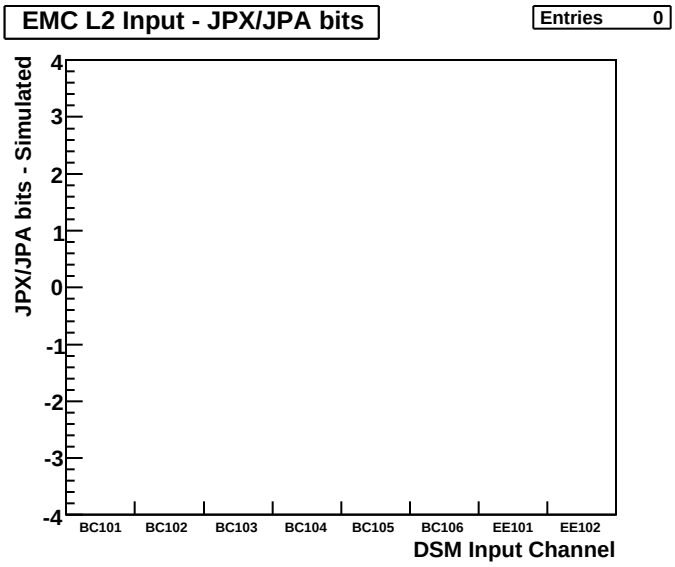

Endcap EMC L1 Input - High Eta Sum
Entries 348
High Eta Sum
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

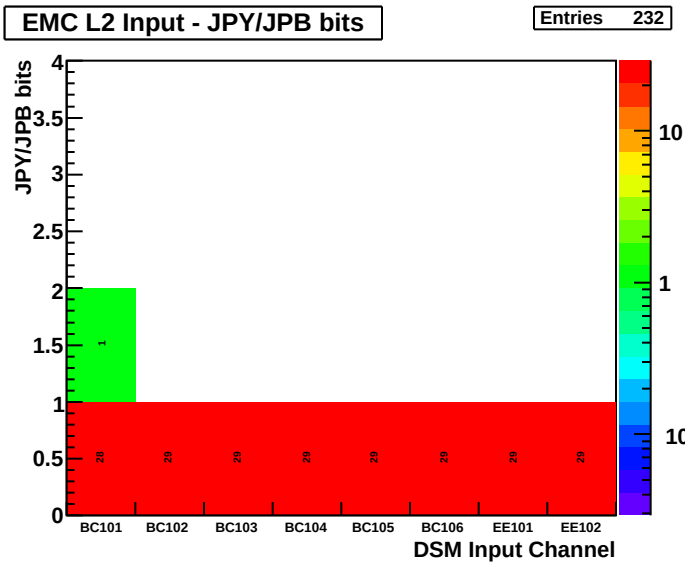

Endcap EMC L1 Input - High Eta Sum
Entries 27
High Eta Sum - Simulated
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

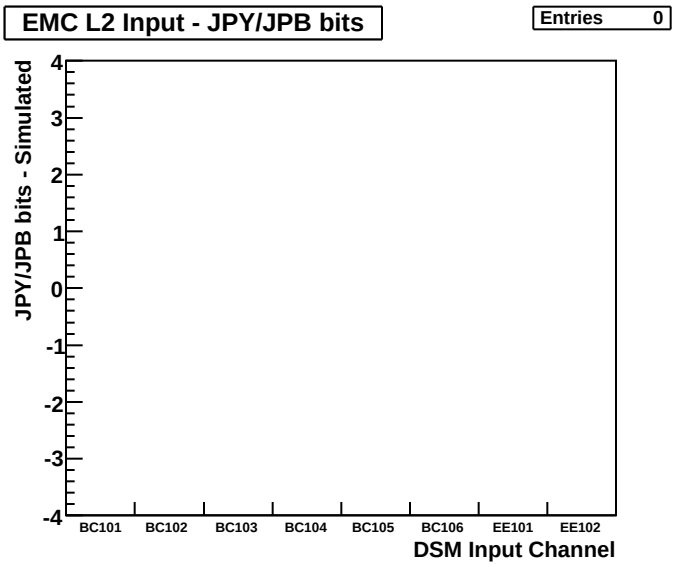

Endcap EMC L1 Input - High Tower Bits
Entries 348
High Tower Bits
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

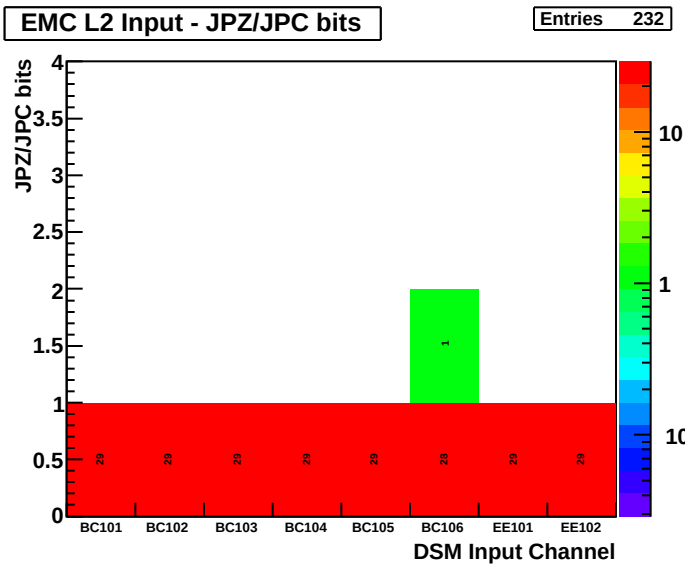

Endcap EMC L1 Input - High Tower Bits
Entries 0
High Tower Bits - Simulated
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

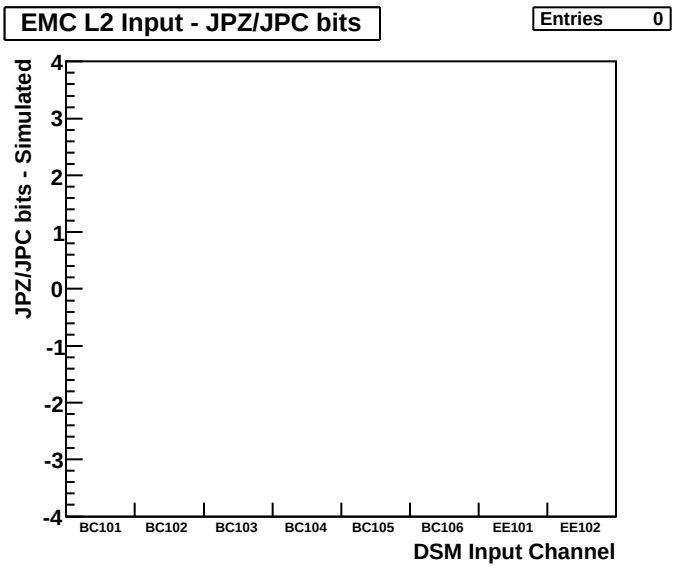

EMC L2 Input - JPX/JPA bits
Entries 232
JPX/JPA bits
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

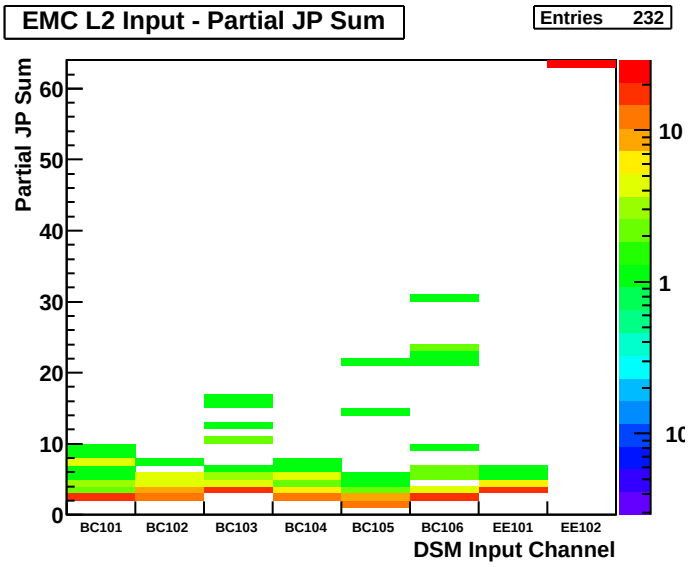

EMC L2 Input - JPX/JPA bits
Entries 0
JPX/JPA bits - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

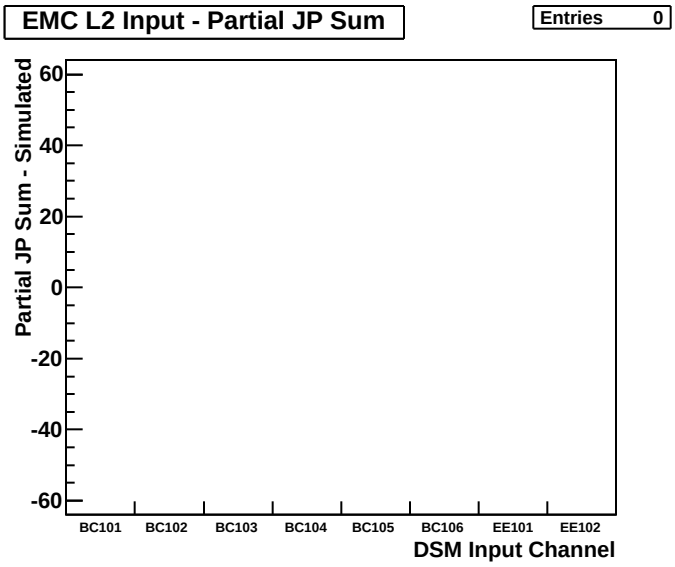

EMC L2 Input - JPY/JPB bits
Entries 232
JPY/JPB bits
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

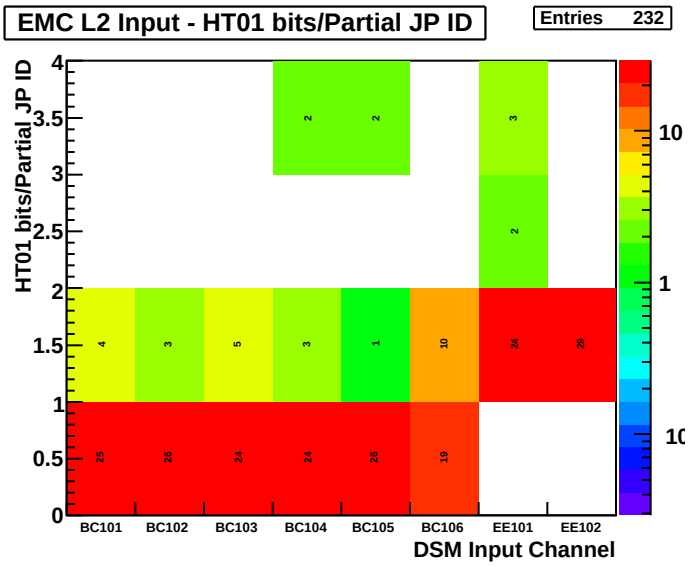

EMC L2 Input - JPY/JPB bits
Entries 0
JPY/JPB bits - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

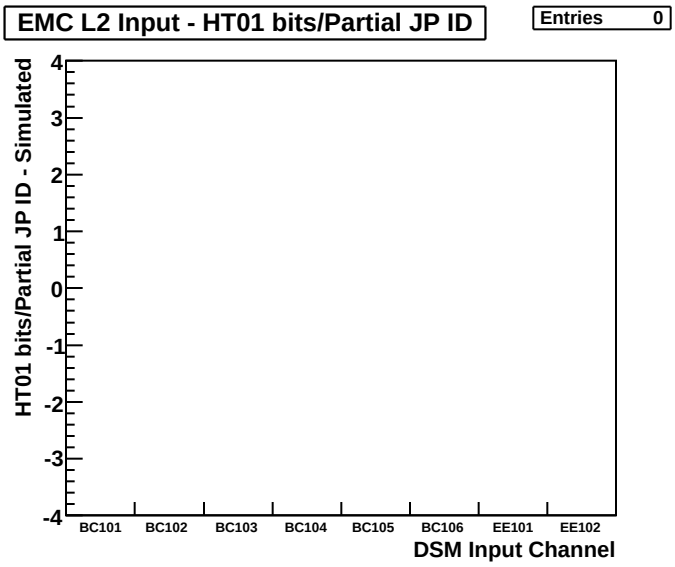

EMC L2 Input - JPZ/JPC bits
Entries 232
JPZ/JPC bits
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

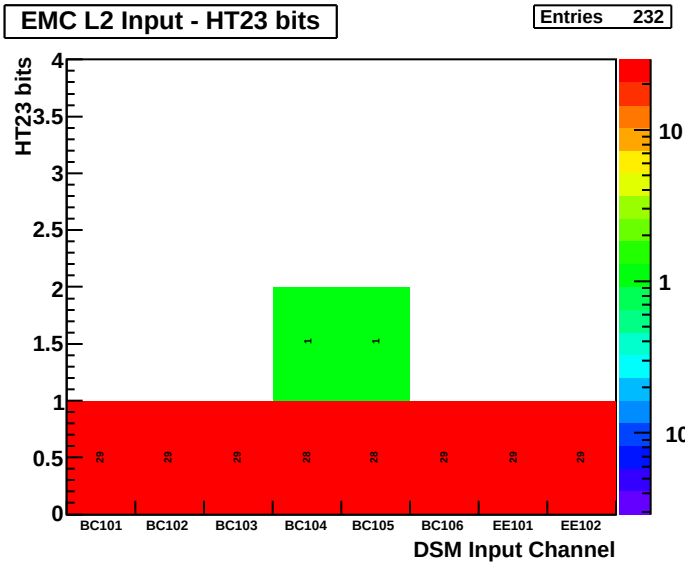

EMC L2 Input - JPZ/JPC bits
Entries 0
JPZ/JPC bits - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

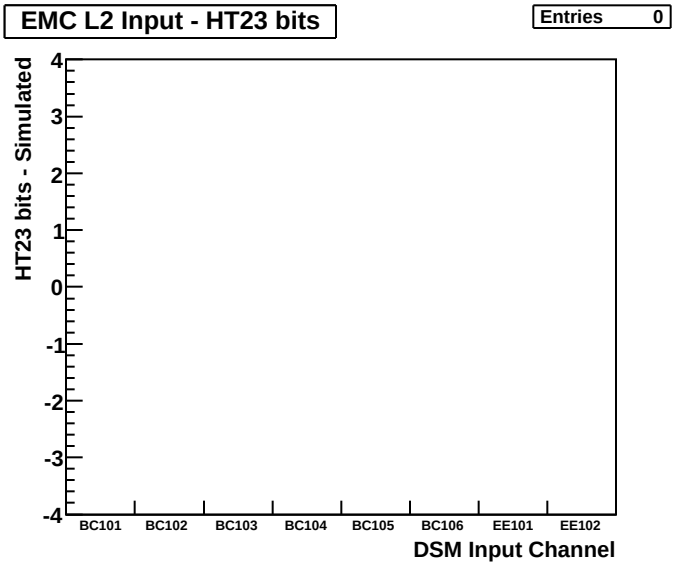

EMC L2 Input - Partial JP Sum
Entries 232
Partial JP Sum
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

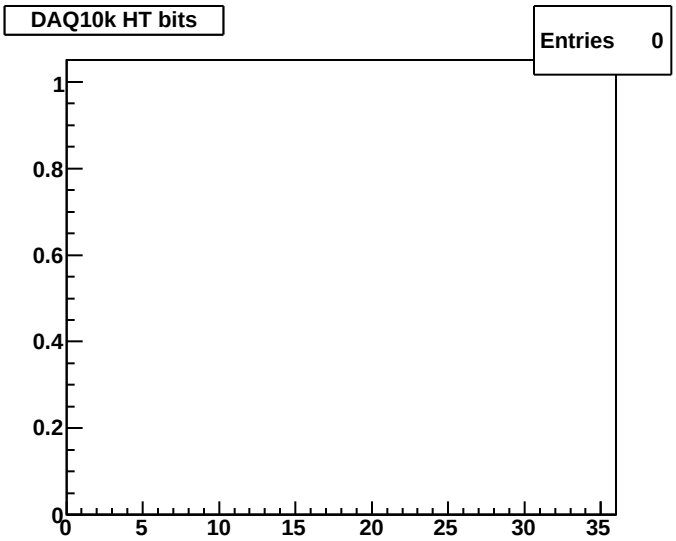

EMC L2 Input - Partial JP Sum
Entries 0
Partial JP Sum - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

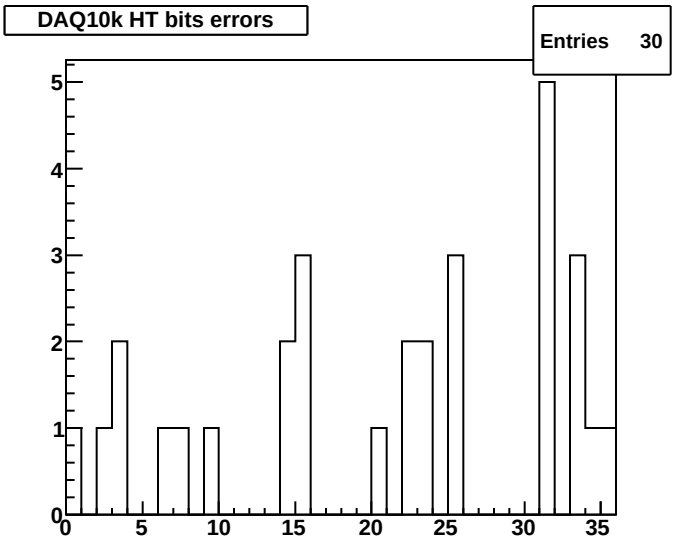

EMC L2 Input - HT01 bits/Partial JP ID
Entries 232
HT01 bits/Partial JP ID
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

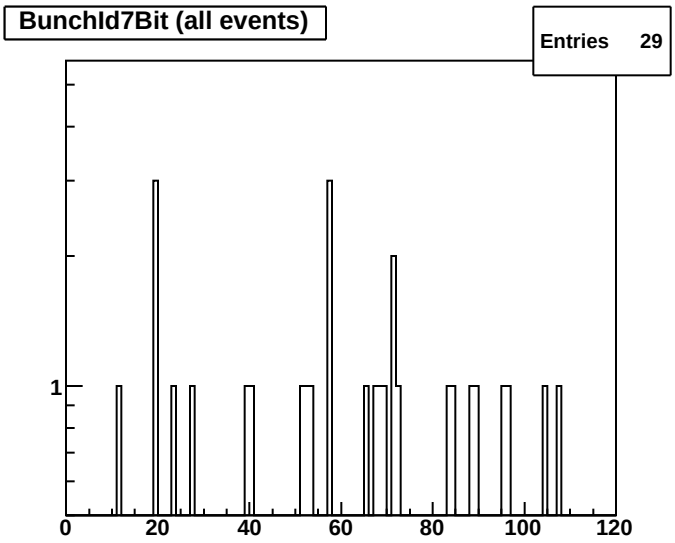

EMC L2 Input - HT01 bits/Partial JP ID
Entries 0
HT01 bits/Partial JP ID - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

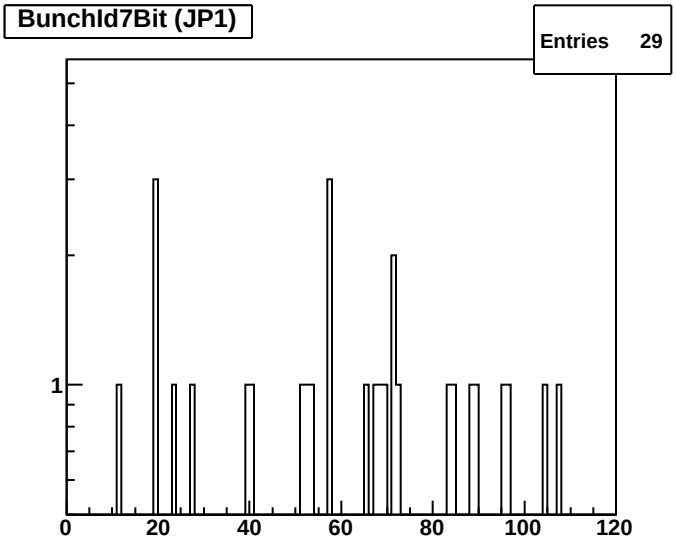

EMC L2 Input - HT23 bits
Entries 232
HT23 bits
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

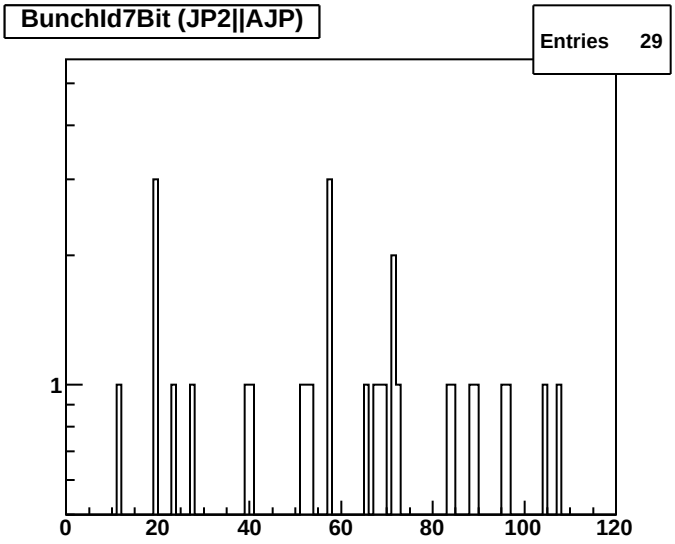

EMC L2 Input - HT23 bits
Entries 0
HT23 bits - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

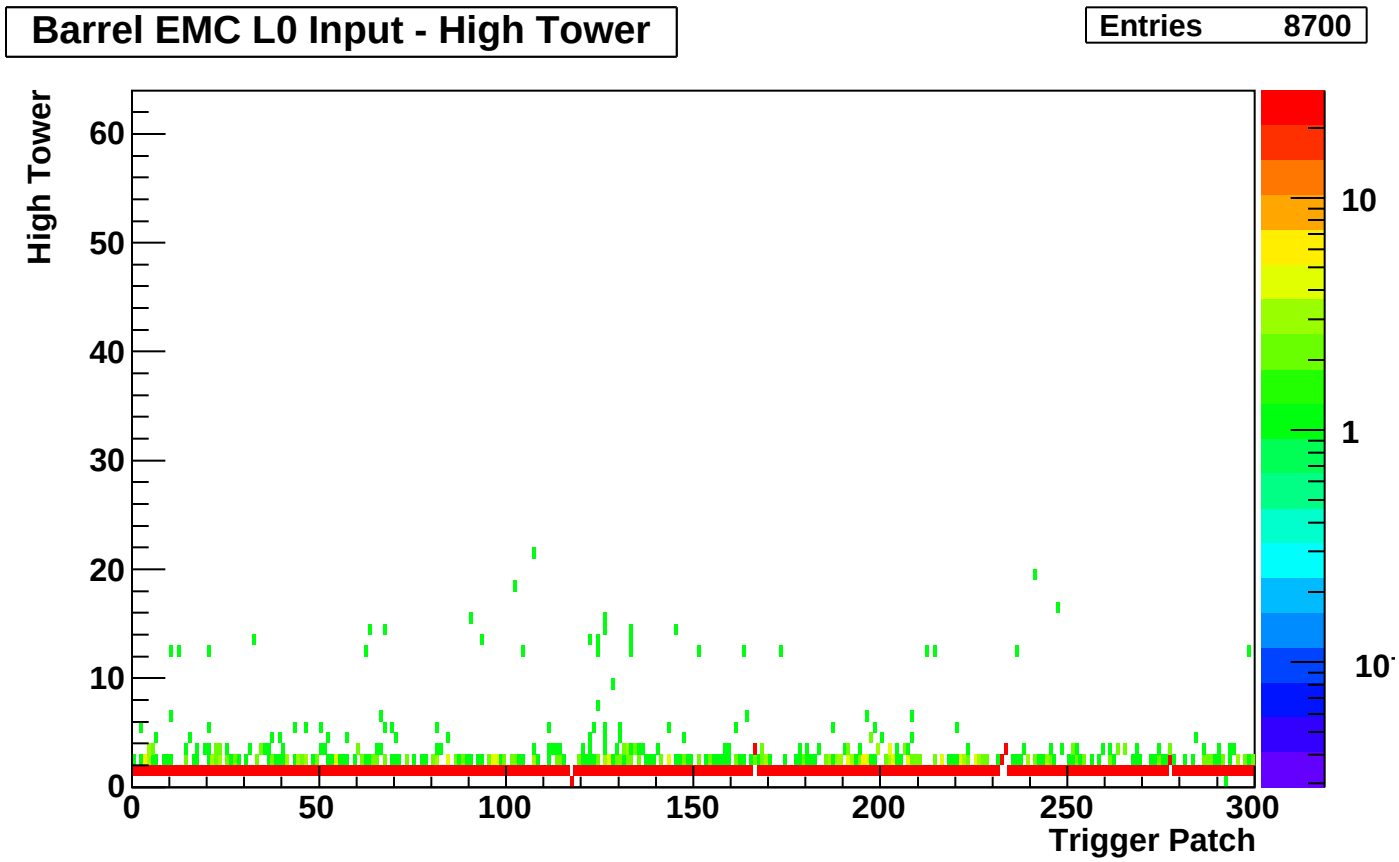

DAQ10k HT bits
Entries 0
1
0.8
0.6
0.4
0.2
0
0 5 10 15 20 25 30 35

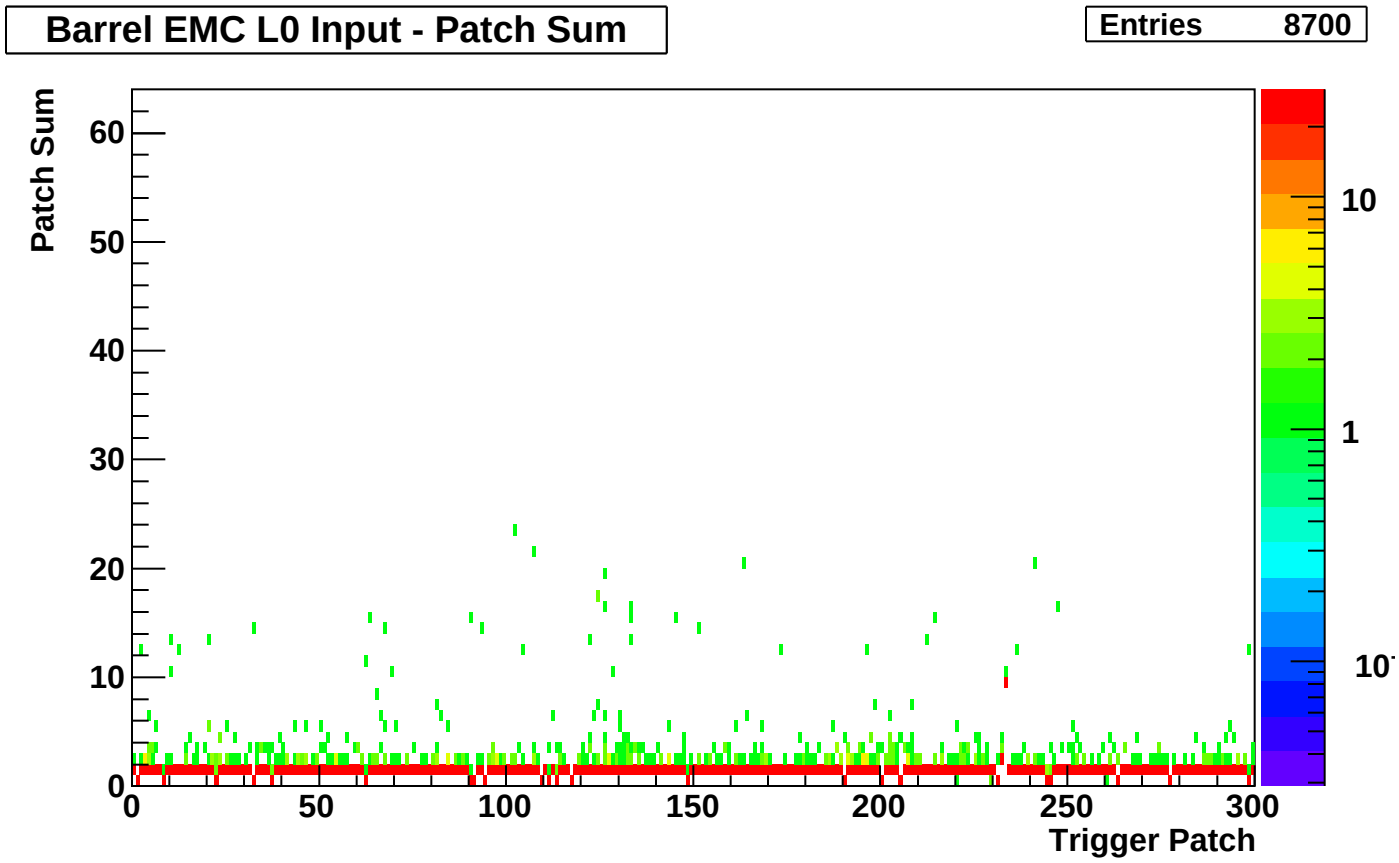

DAQ10k HT bits errors
Entries 30
5
4
3
2
1
0
0 5 10 15 20 25 30 35

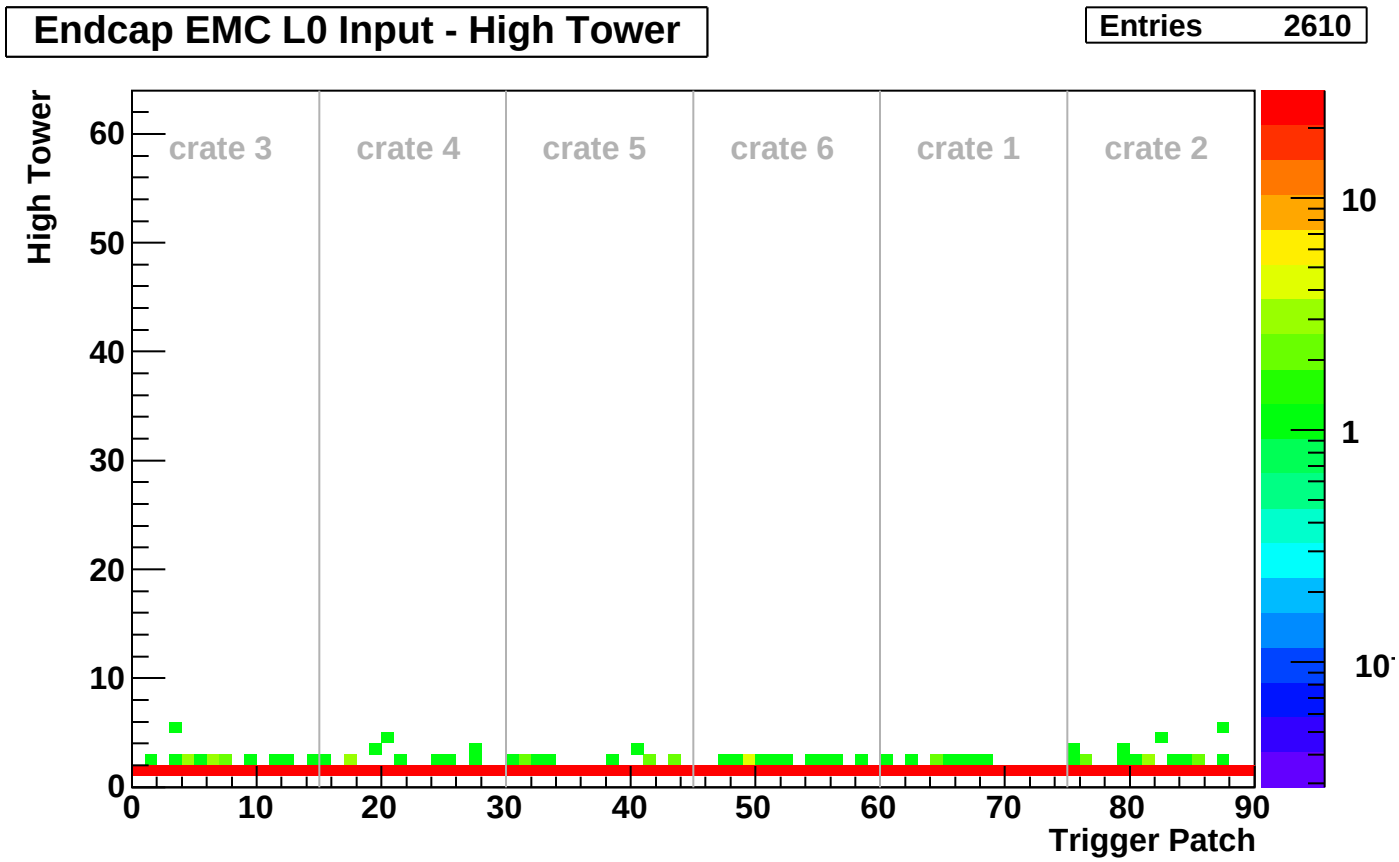

BunchId7Bit (all events)
Entries 29
1
0 20 40 60 80 100 120

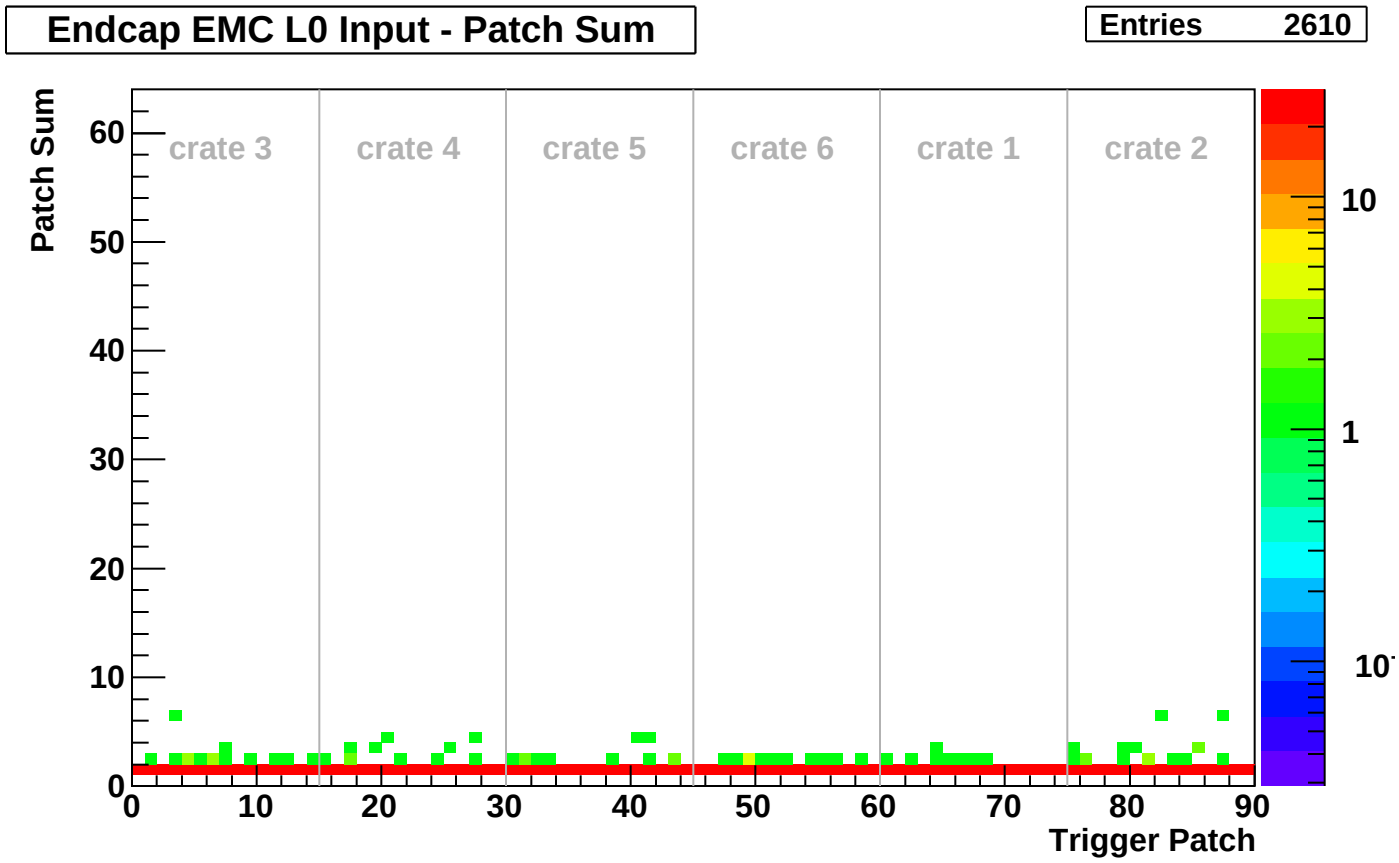

BunchId7Bit (JP1)
Entries 29
1
0 20 40 60 80 100 120

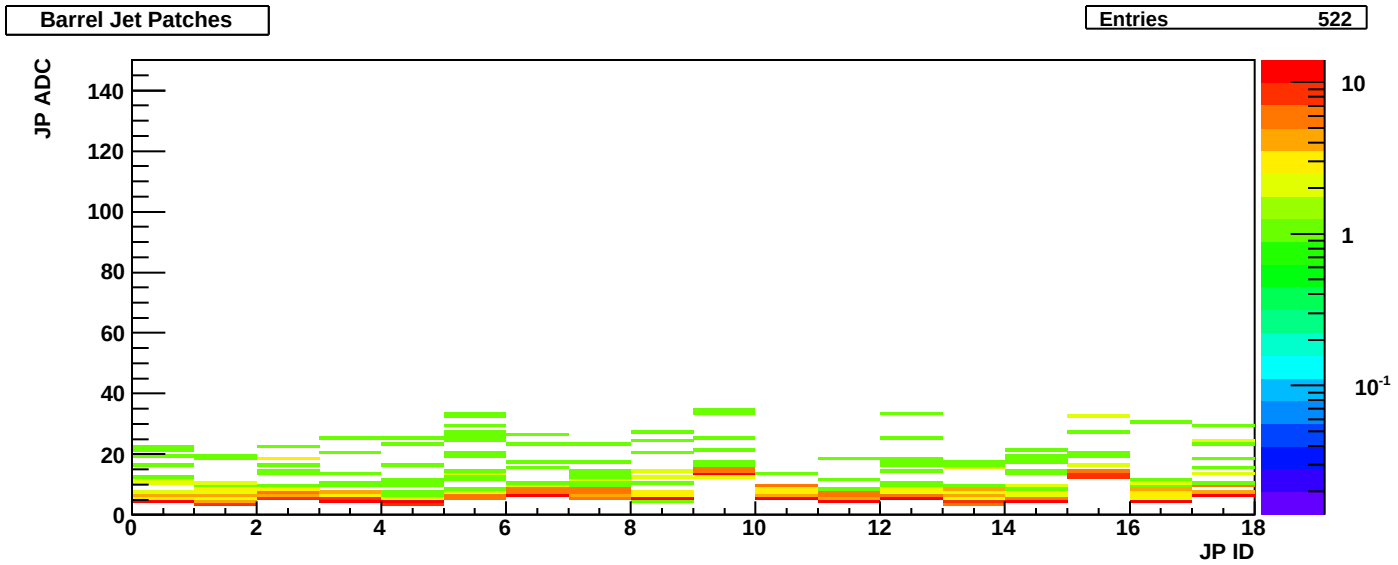

BunchId7Bit (JP2||AJP)
Entries 29
1
0 20 40 60 80 100 120

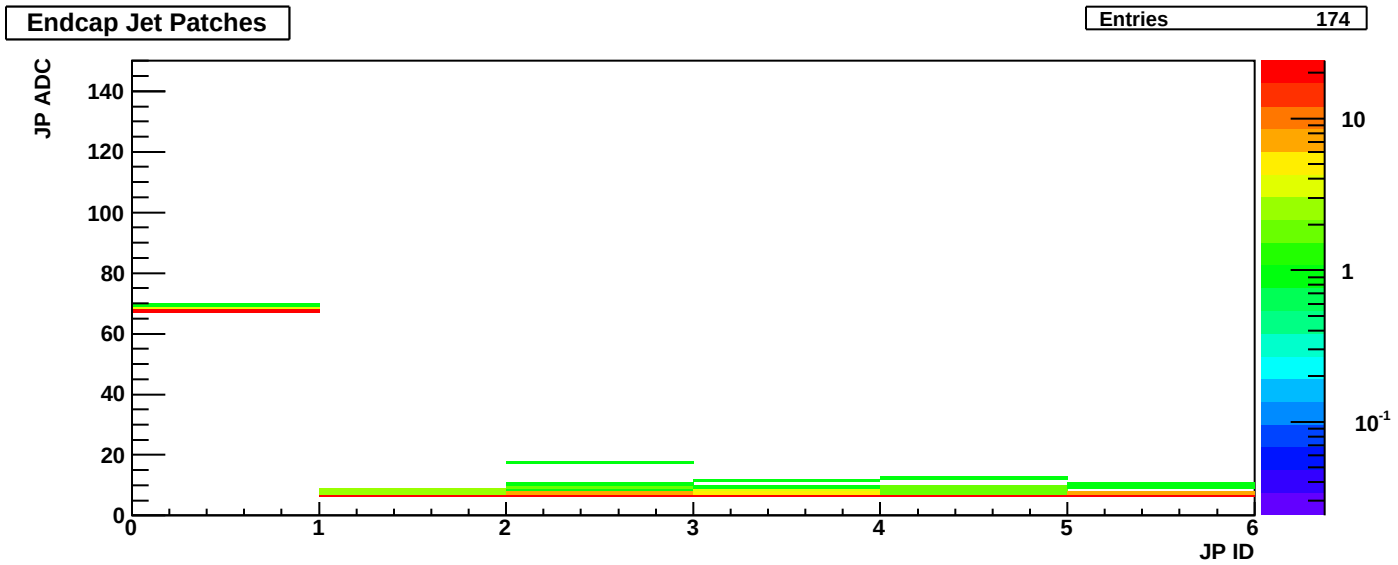

Barrel EMC L0 Input - High Tower
Entries 8700
High Tower
Trigger Patch
0
10
20
30
40
50
60
0
50
100
150
200
250
300
10
1
10

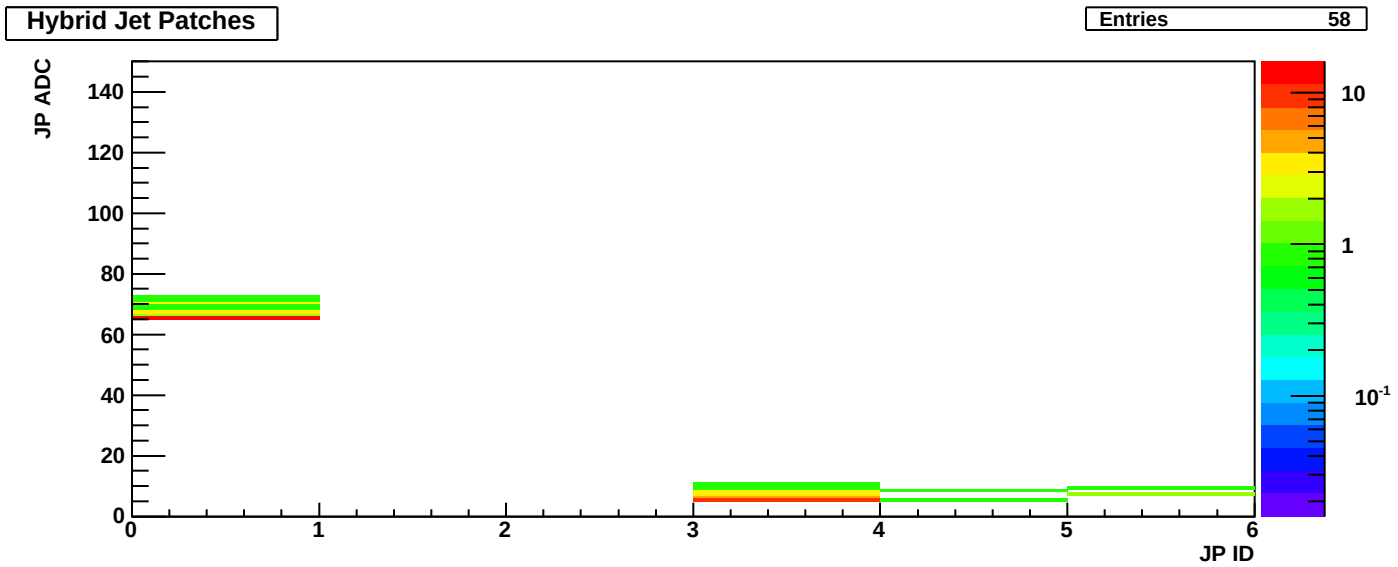

Barrel EMC L0 Input - Patch Sum
Entries 8700
Patch Sum
Trigger Patch
0
10
20
30
40
50
60
0
50
100
150
200
250
300
10
1
10

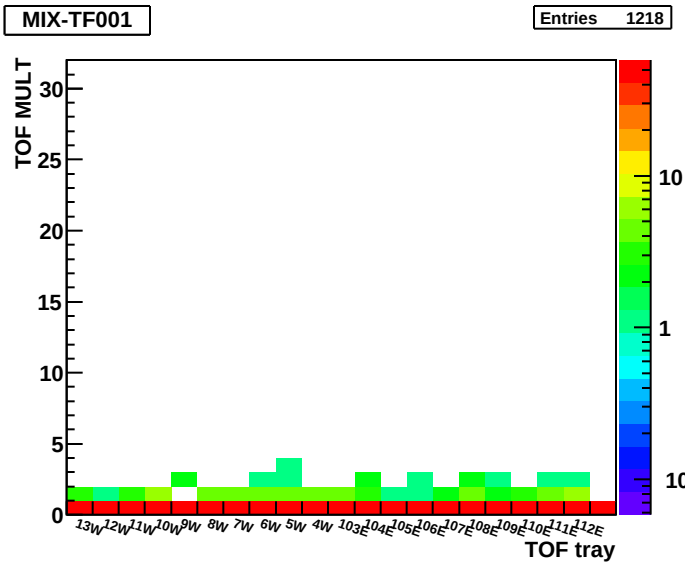

Endcap EMC L0 Input - High Tower
Entries 2610
High Tower
crate 3
crate 4
crate 5
crate 6
crate 1
crate 2
Trigger Patch

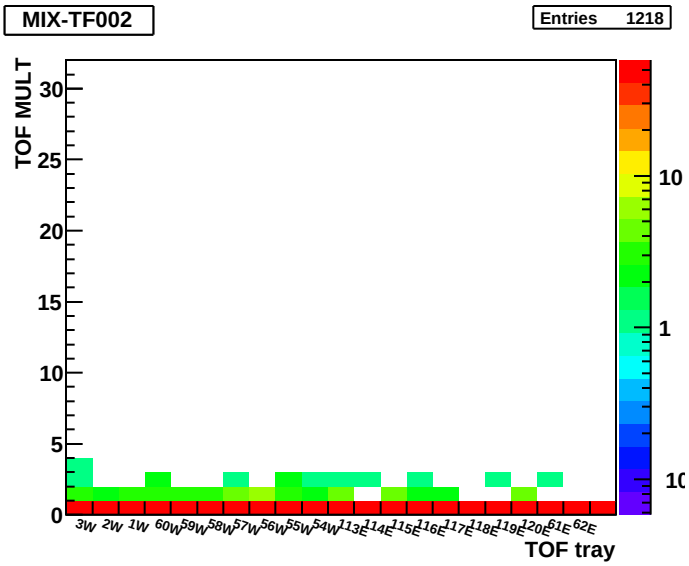

Endcap EMC L0 Input - Patch Sum
Entries 2610
Patch Sum
crate 3
crate 4
crate 5
crate 6
crate 1
crate 2
Trigger Patch

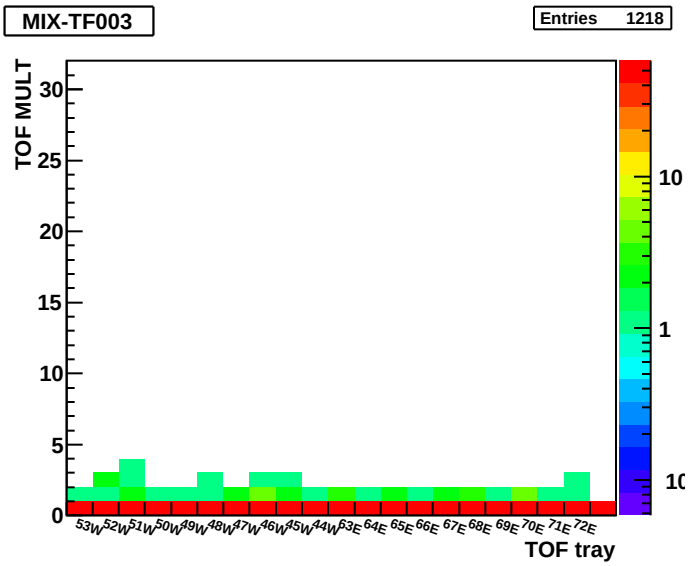

Barrel Jet Patches
Entries 522
JP ADC
JP ID

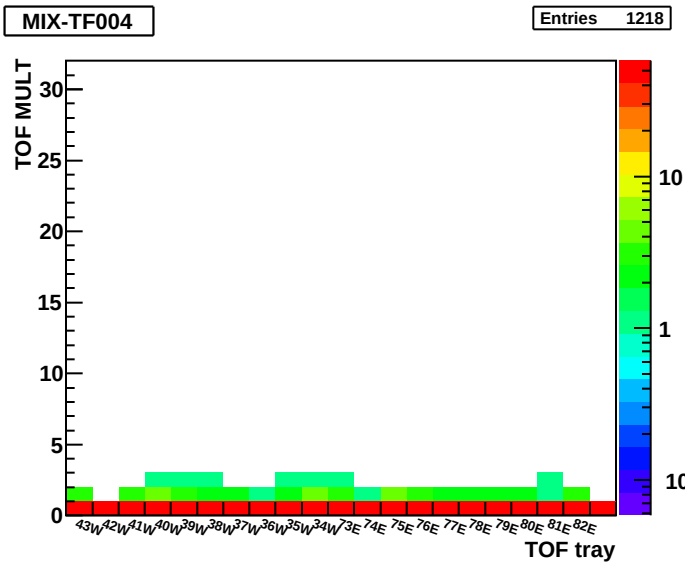

Endcap Jet Patches
Entries 174
JP ADC
JP ID

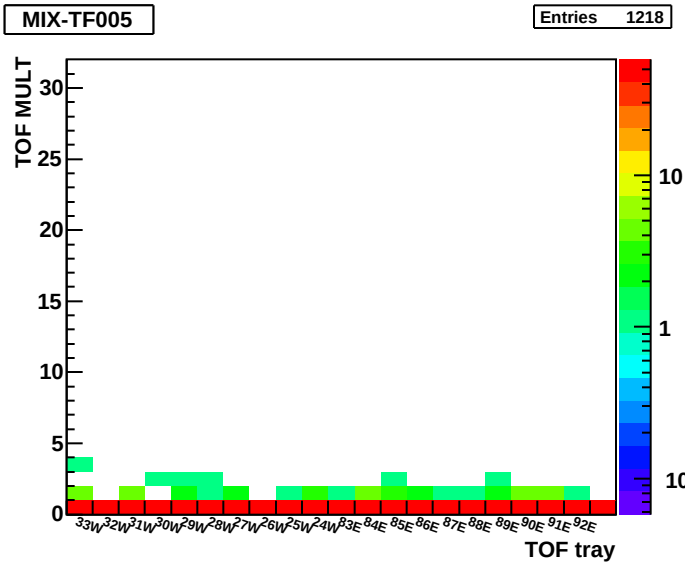

Hybrid Jet Patches
Entries 58
JP ADC
JP ID

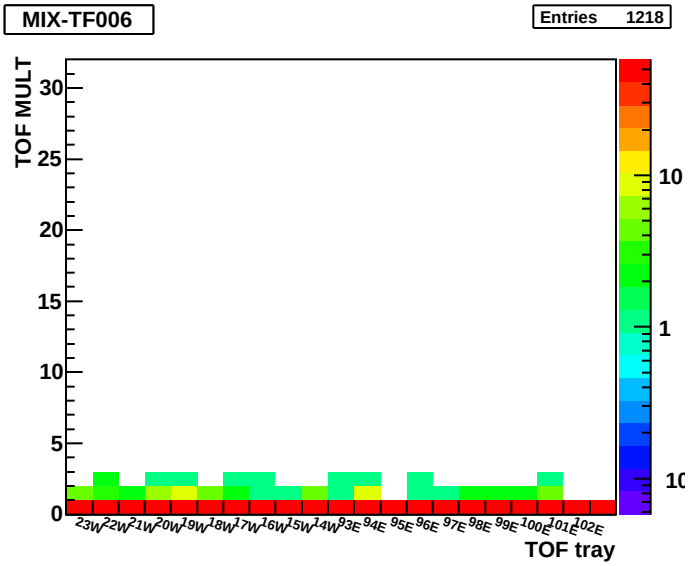

MIX-TF001
Entries 1218
TOF MULT
TOF tray

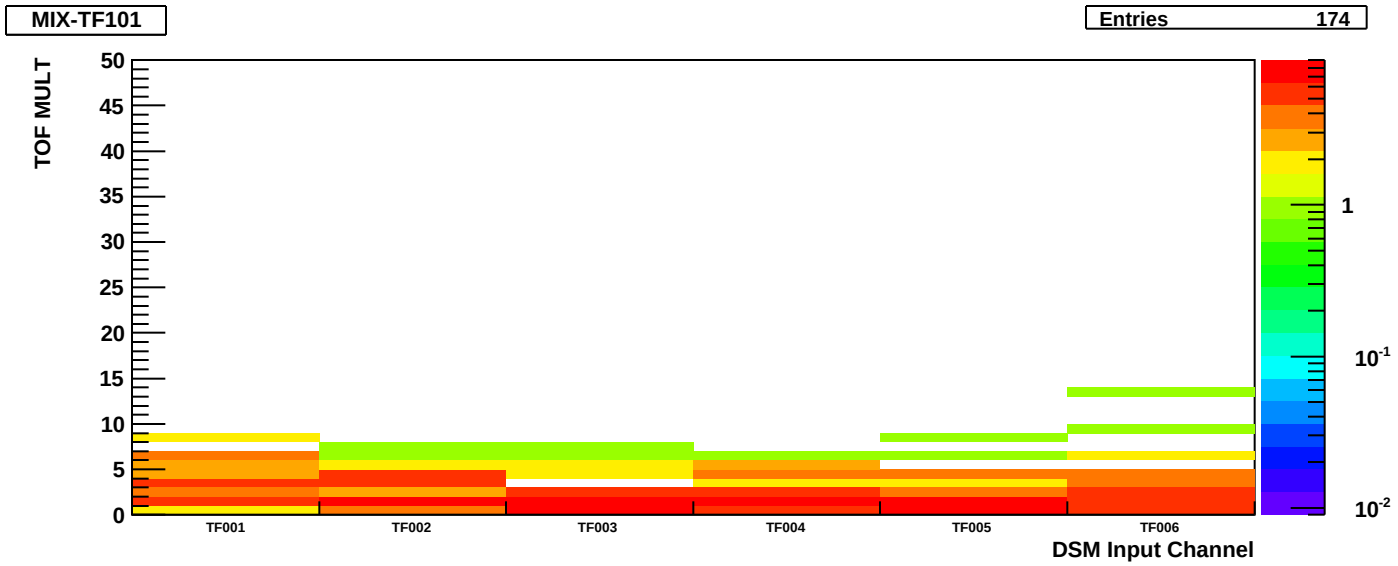

MIX-TF002
Entries 1218
TOF MULT
TOF tray

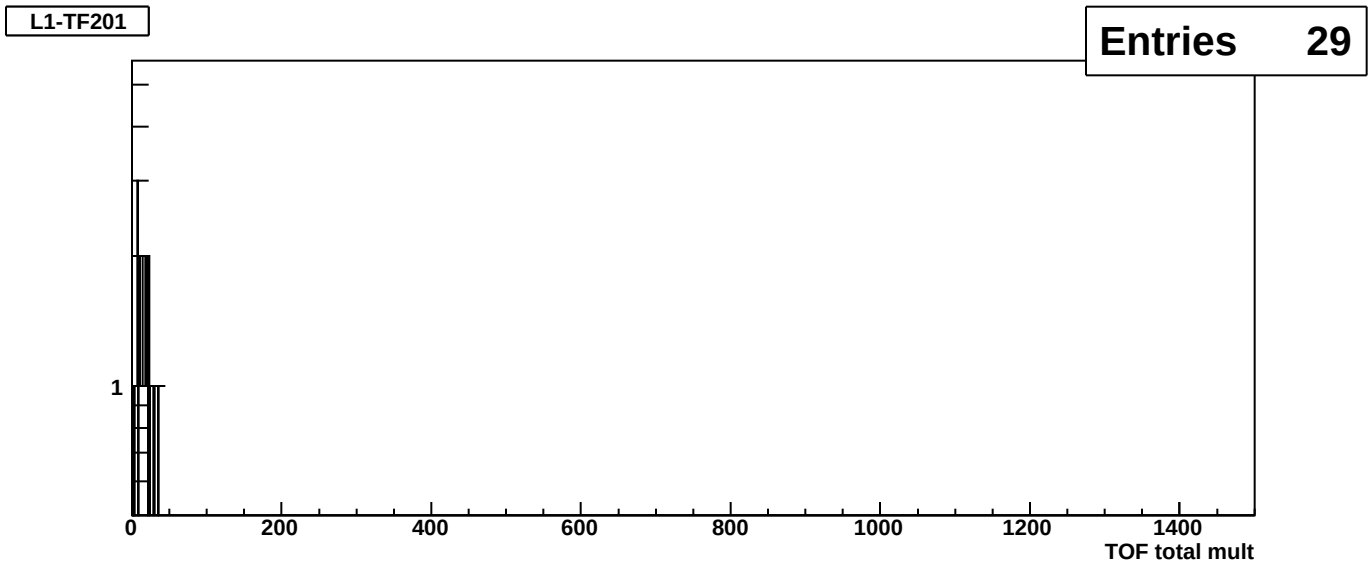

MIX-TF003
Entries 1218
TOF MULT
TOF tray

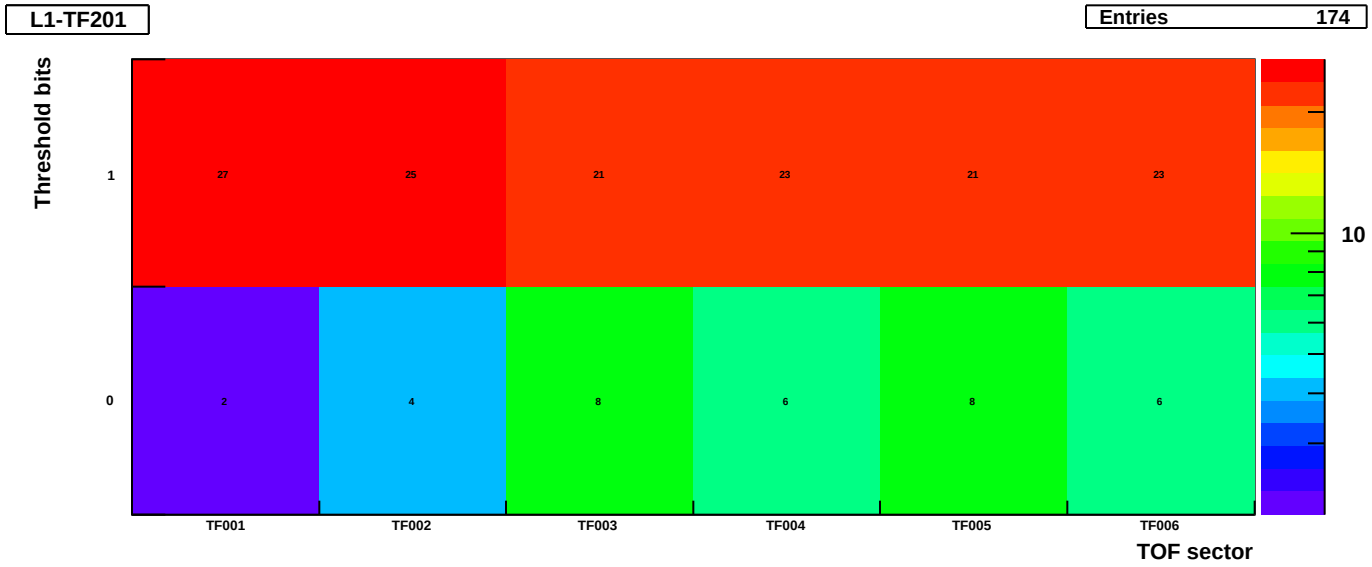

MIX-TF004
Entries 1218
TOF MULT
TOF tray

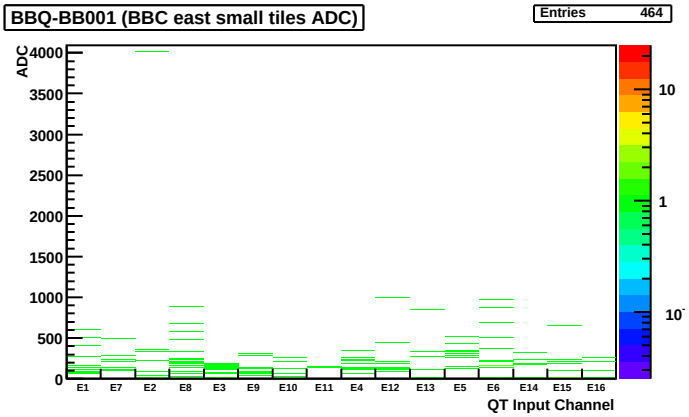

MIX-TF005
Entries 1218
TOF MULT
TOF tray

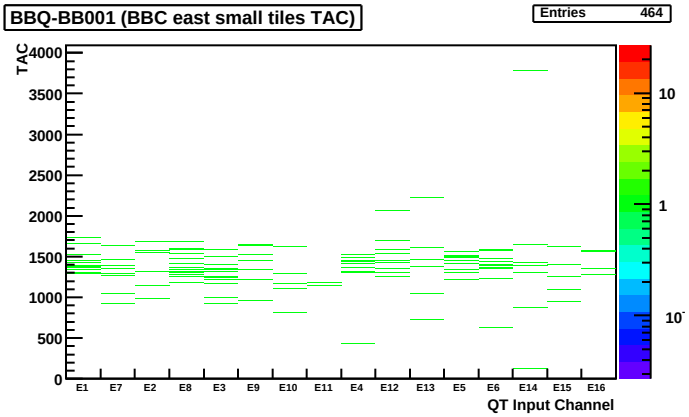

MIX-TF006
Entries 1218
TOF MULT
TOF tray

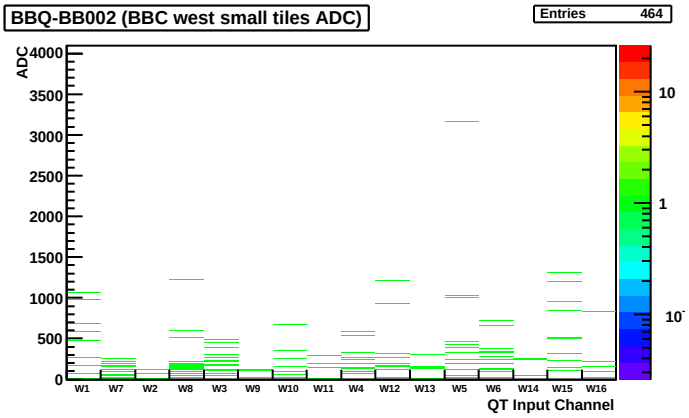

MIX-TF101
Entries 174
TOF MULT
50
45
40
35
30
25
20
15
10
5
0
TF001
TF002
TF003
TF004
TF005
TF006
DSM Input Channel
1
10^{-1}
10^{-2}

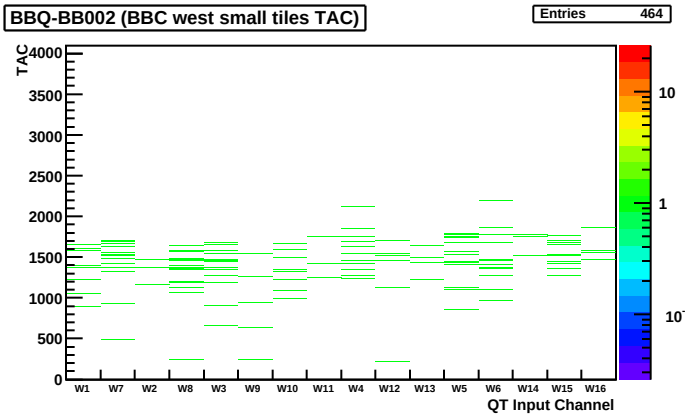

L1-TF201
Entries 29
1
0
200
400
600
800
1000
1200
1400
TOF total mult

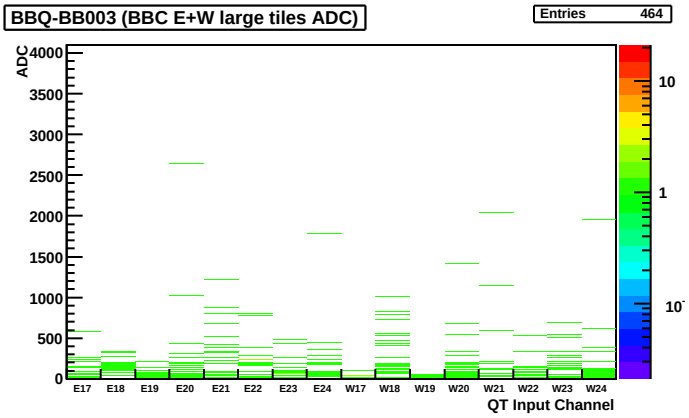

L1-TF201
Entries 174
Threshold bits
1
0
27
25
21
23
21
23
2
4
8
6
8
6
TF001
TF002
TF003
TF004
TF005
TF006
TOF sector
10

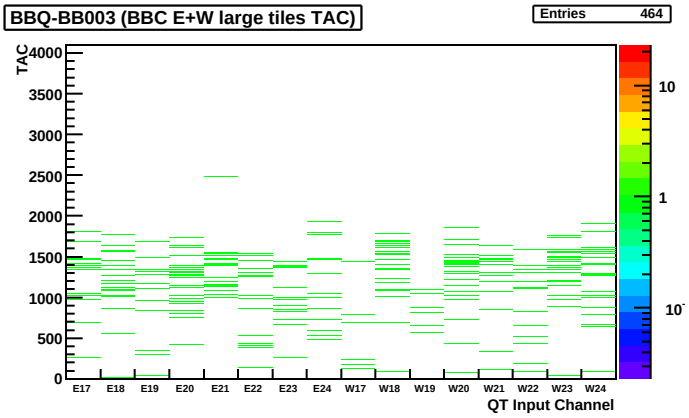

BBQ-BB001 (BBC east small tiles ADC)
Entries 464
ADC
QT Input Channel

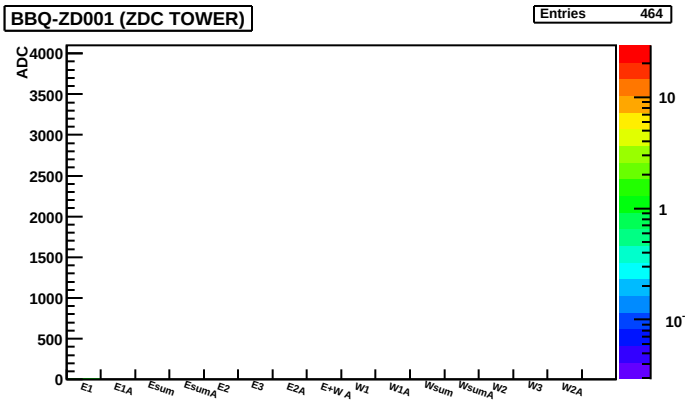

BBQ-BB001 (BBC east small tiles TAC)
Entries 464
TAC
QT Input Channel

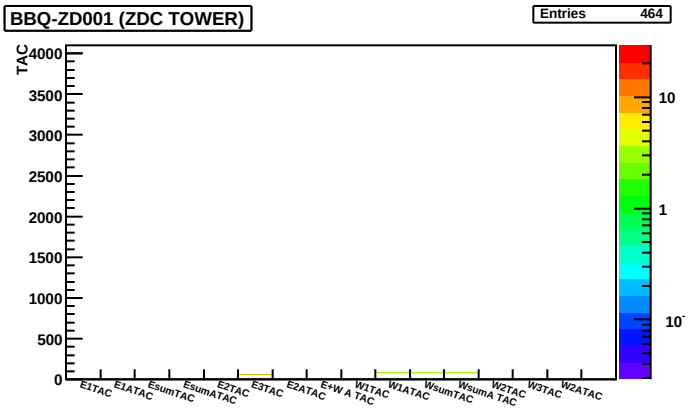

BBQ-BB002 (BBC west small tiles ADC)
Entries 464
ADC
QT Input Channel

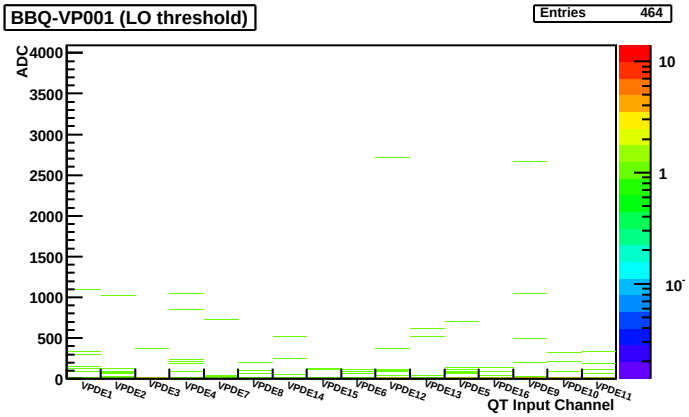

BBQ-BB002 (BBC west small tiles TAC)
Entries 464
TAC
QT Input Channel

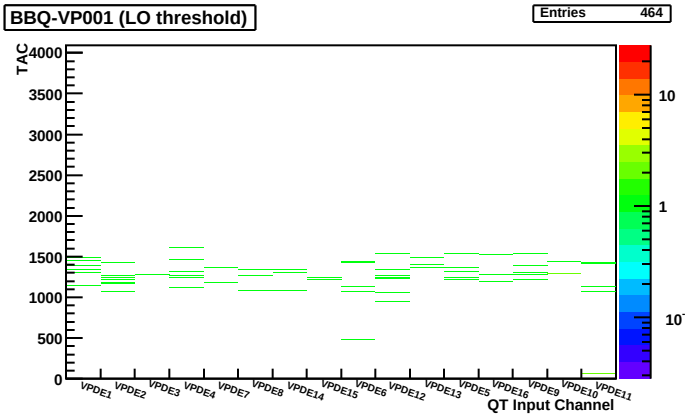

BBQ-BB003 (BBC E+W large tiles ADC)
Entries 464
ADC
QT Input Channel

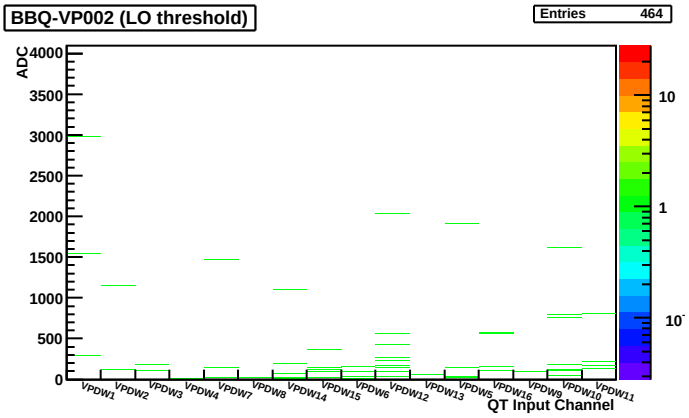

BBQ-BB003 (BBC E+W large tiles TAC)
Entries 464
TAC
QT Input Channel

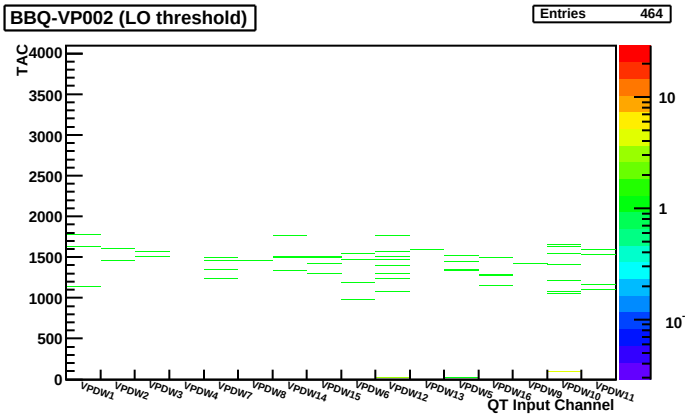

BBQ-ZD001 (ZDC TOWER)
Entries 464
ADC

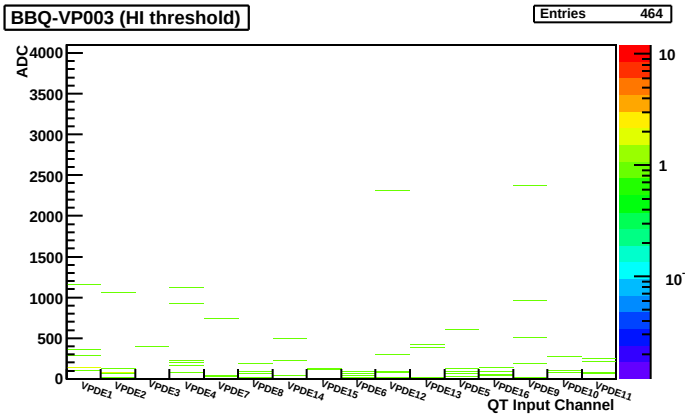

BBQ-ZD001 (ZDC TOWER)
Entries 464
TAC

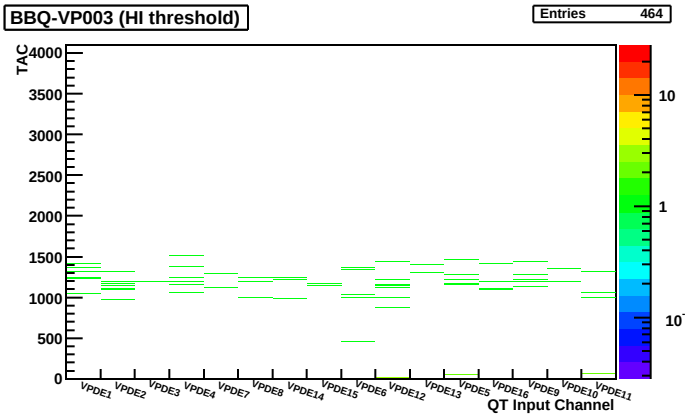

BBQ-VP001 (LO threshold)
Entries 464
ADC
QT Input Channel

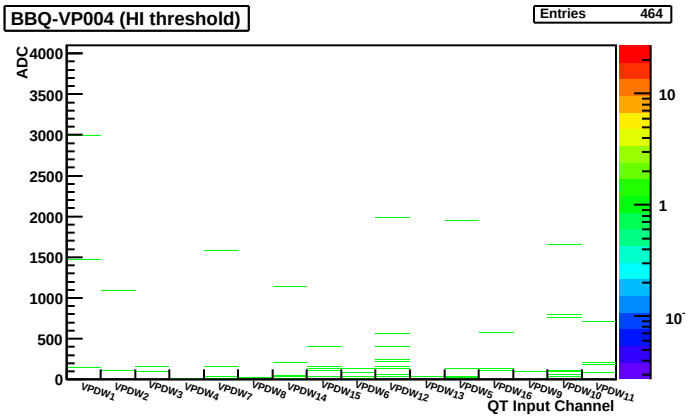

BBQ-VP001 (LO threshold)
Entries 464
TAC
QT Input Channel

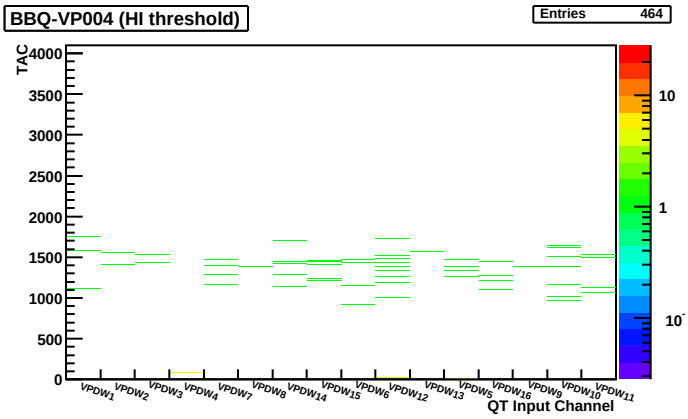

BBQ-VP002 (LO threshold)
Entries 464
ADC
QT Input Channel

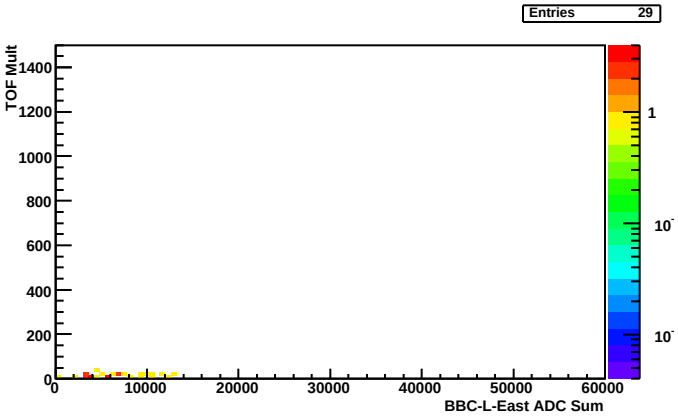

BBQ-VP002 (LO threshold)
Entries 464
TAC
QT Input Channel

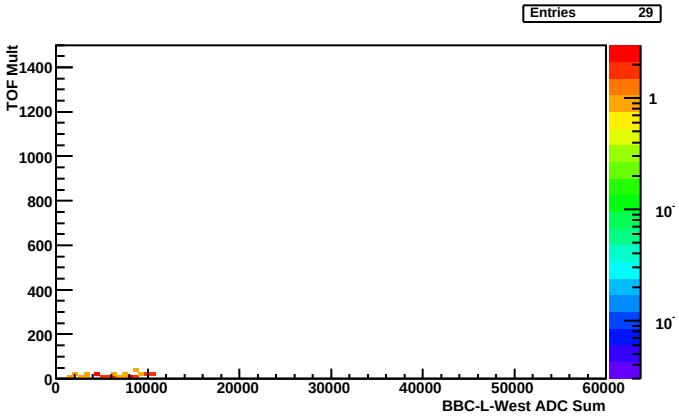

BBQ-VP003 (HI threshold)
Entries 464
ADC
QT Input Channel

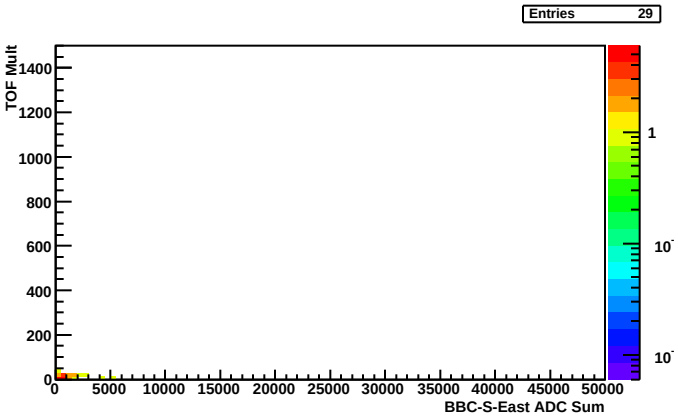

BBQ-VP003 (HI threshold)
Entries 464
TAC
QT Input Channel

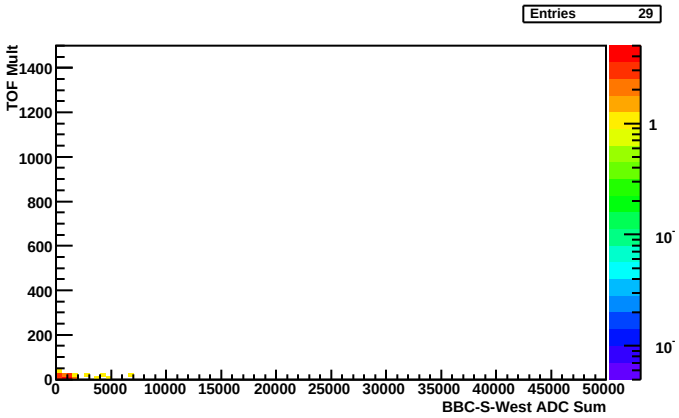

BBQ-VP004 (HI threshold)
Entries 464
ADC
QT Input Channel

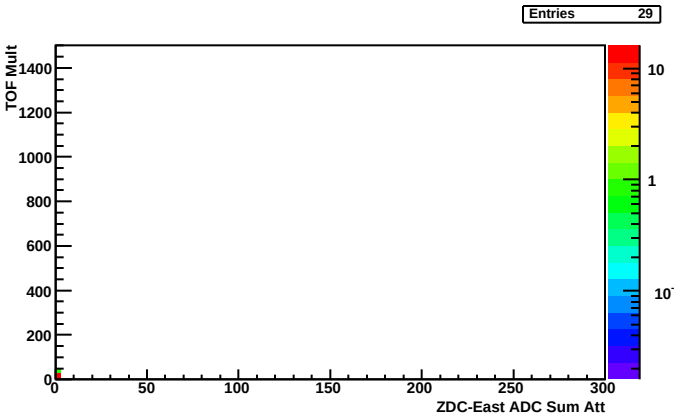

BBQ-VP004 (HI threshold)
Entries 464
TAC
QT Input Channel

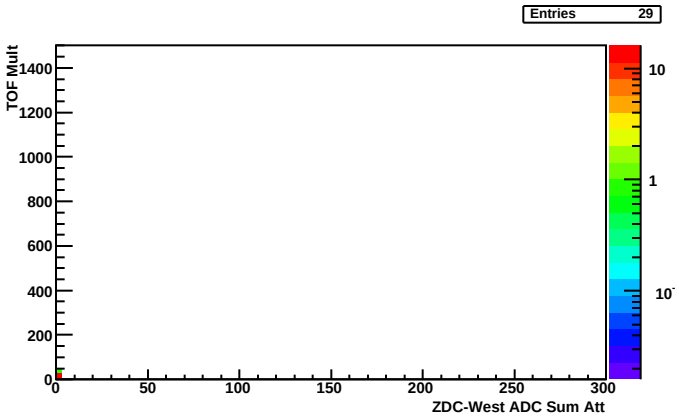

Entries 29
TOF Mult
BBC-L-East ADC Sum

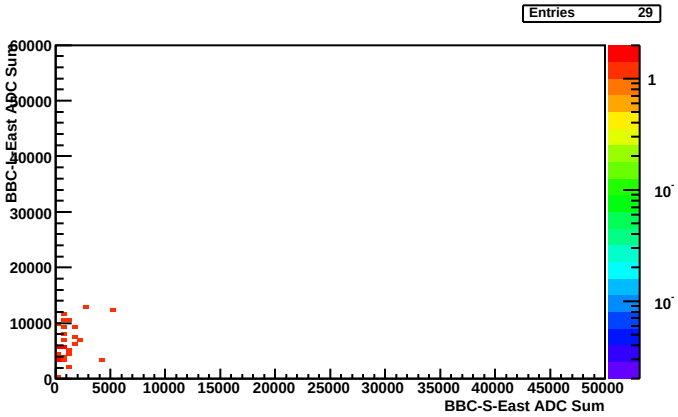

Entries 29
TOF Mult
BBC-L-West ADC Sum

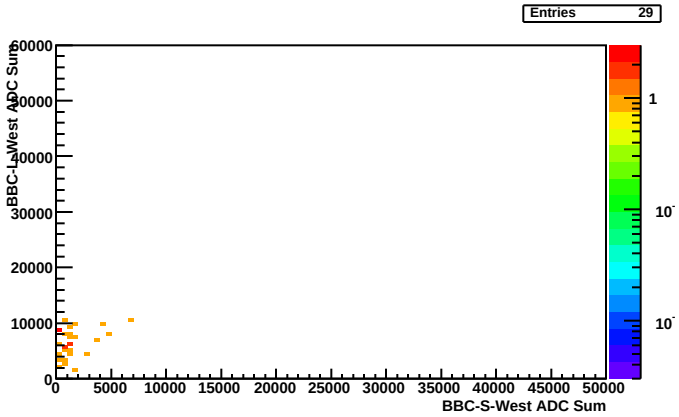

Entries 29
TOF Mult
BBC-S-East ADC Sum

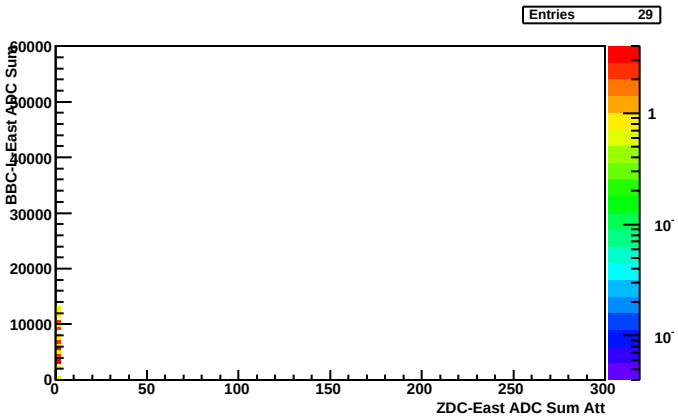

Entries 29
TOF Mult
BBC-S-West ADC Sum

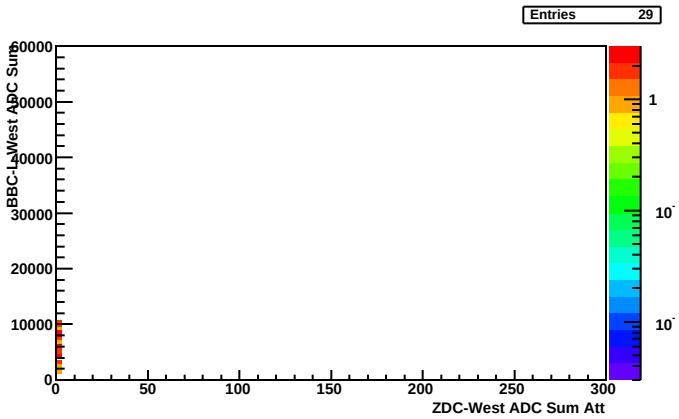

Entries 29
TOF Mult
ZDC-East ADC Sum Att

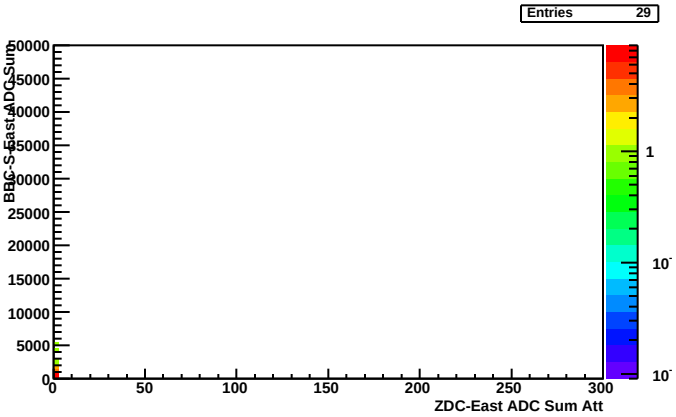

Entries 29
TOF Mult
ZDC-West ADC Sum Att

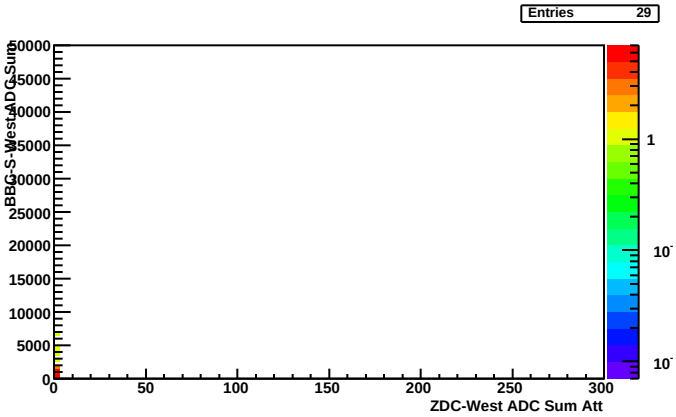

Entries 29
BBC-L-East ADC Sum
BBC-S-East ADC Sum

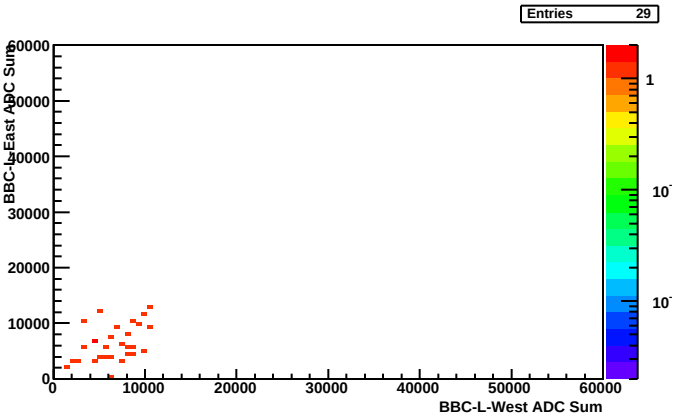

Entries 29
BBC-L-West ADC Sum
BBC-S-West ADC Sum

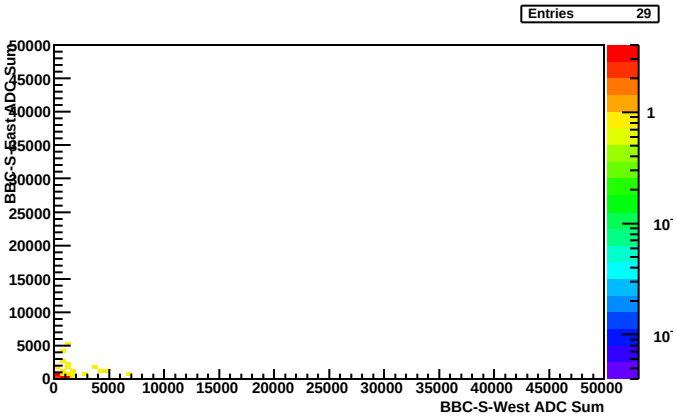

Entries 29
BBC-L-East ADC Sum
ZDC-East ADC Sum Att

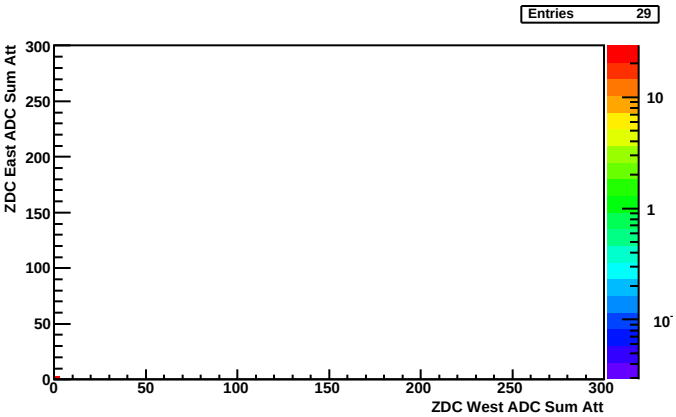

Entries 29
BBC-L-West ADC Sum
ZDC-West ADC Sum Att

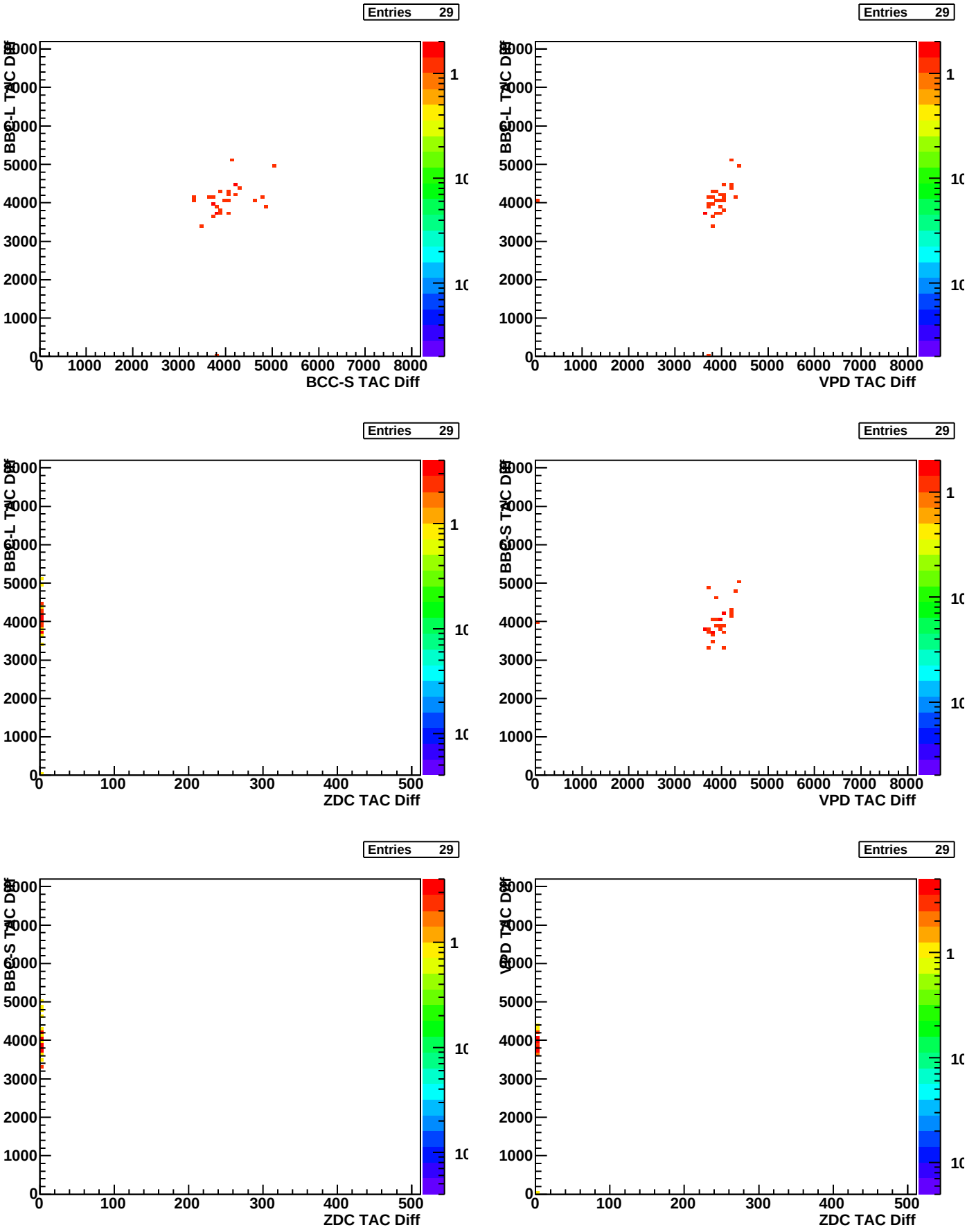

Entries 29
BBC-S-East ADC Sum
ZDC-East ADC Sum Att

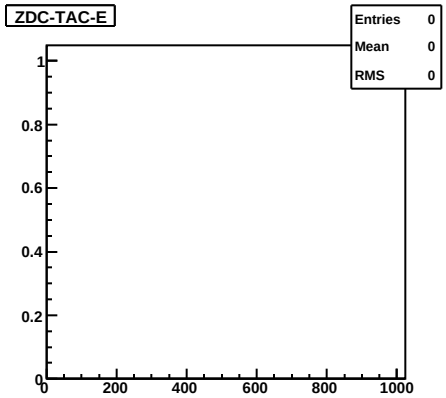

Entries 29
BBC-S-West ADC Sum
ZDC-West ADC Sum Att

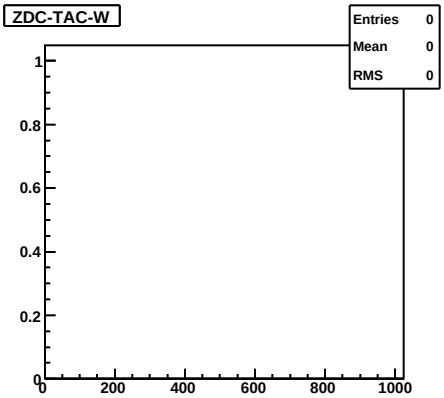

Entries 29
BBC-L-East ADC Sum
BBC-L-West ADC Sum

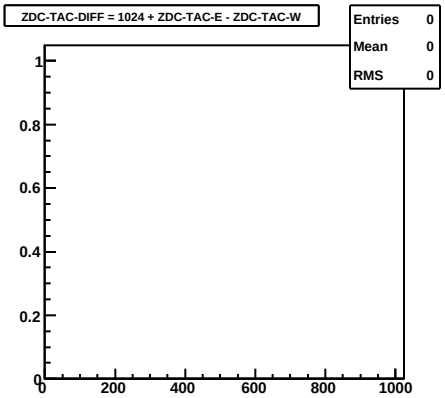

Entries 29
BBC-S-East ADC Sum
BBC-S-West ADC Sum

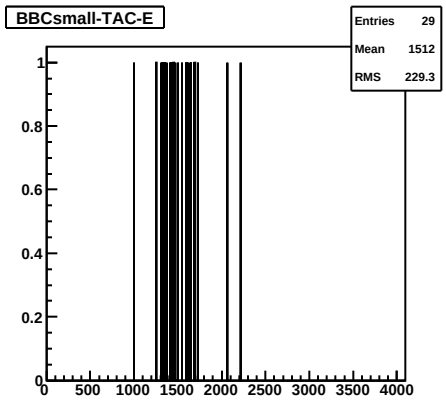

Entries 29
ZDC East ADC Sum Att
ZDC West ADC Sum Att

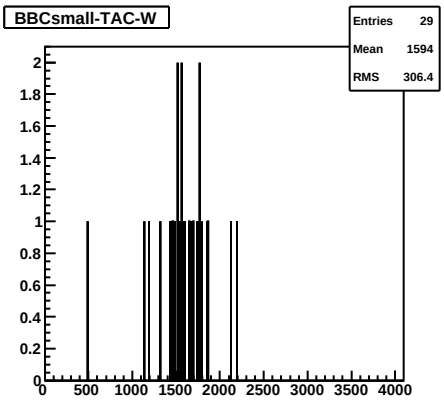

Entries 29
BBC-L TAC Diff
BCC-S TAC Diff
Entries 29
BBC-L TAC Diff
VPD TAC Diff
Entries 29
BBC-L TAC Diff
ZDC TAC Diff
Entries 29
BBC-S TAC Diff
VPD TAC Diff
Entries 29
BBC-S TAC Diff
ZDC TAC Diff
Entries 29
VPD TAC Diff
ZDC TAC Diff

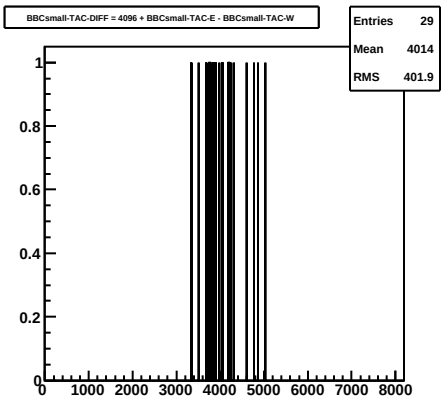

ZDC-TAC-E
Entries 0
Mean 0
RMS 0

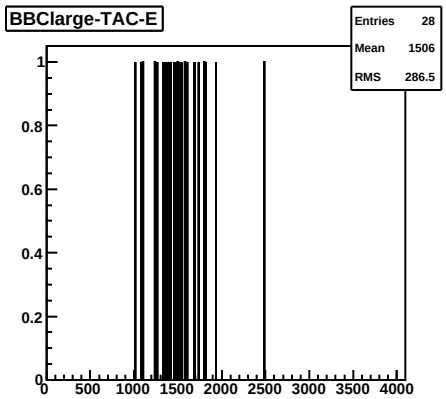

ZDC-TAC-W
Entries 0
Mean 0
RMS 0

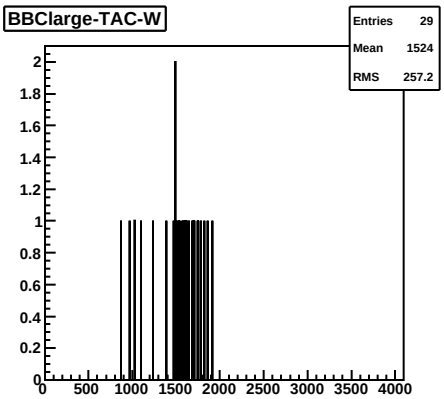

ZDC-TAC-DIFF = 1024 + ZDC-TAC-E - ZDC-TAC-W
Entries 0
Mean 0
RMS 0

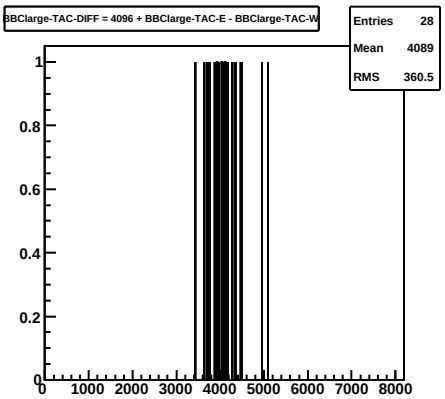

BBCsmall-TAC-E
Entries 29
Mean 1512
RMS 229.3

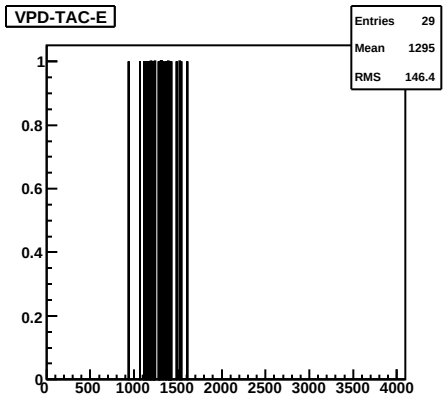

BBCsmall-TAC-W
Entries 29
Mean 1594
RMS 306.4

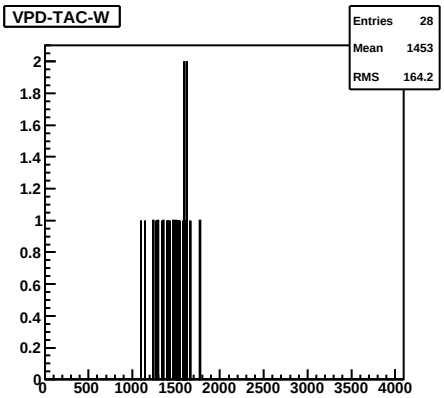

BBCsmall-TAC-DIFF = 4096 + BBCsmall-TAC-E - BBCsmall-TAC-W
Entries 29
Mean 4014
RMS 401.9

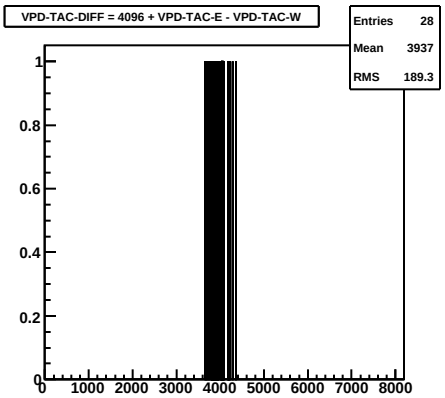

BBClarge-TAC-E
Entries 28
Mean 1506
RMS 286.5

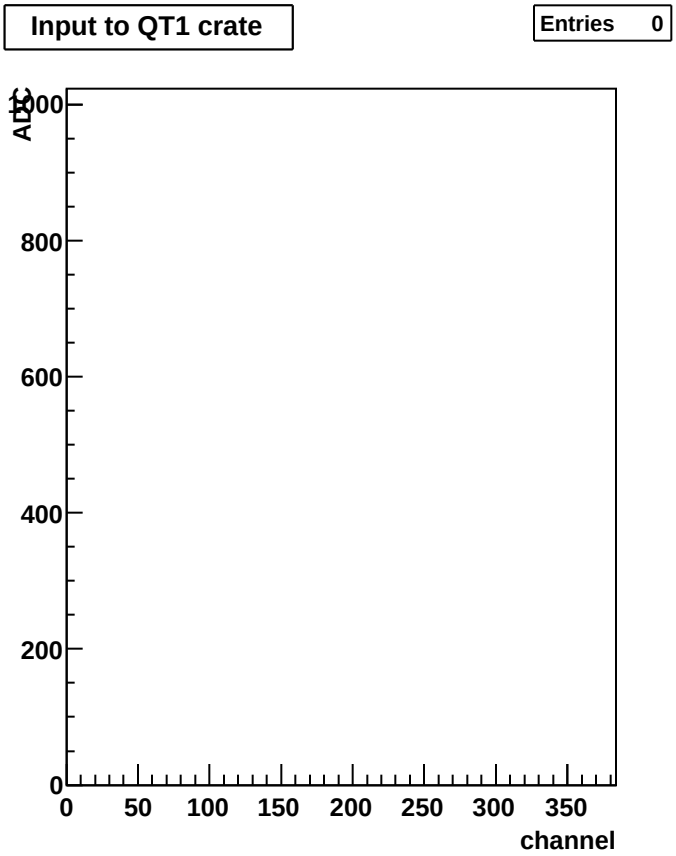

BBClarge-TAC-W
Entries 29
Mean 1524
RMS 257.2

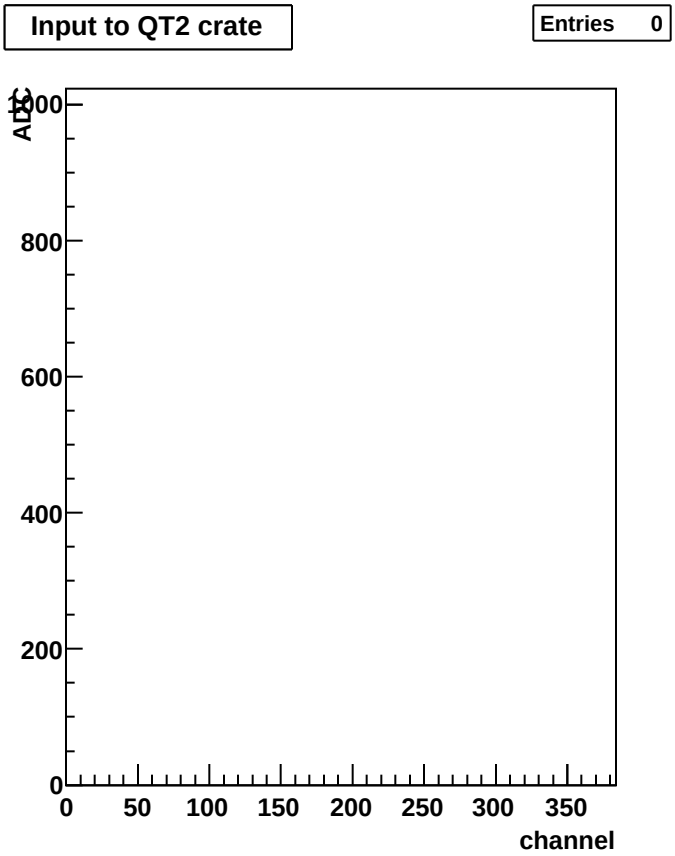

BBClarge-TAC-DIFF = 4096 + BBClarge-TAC-E - BBClarge-TAC-W
Entries 28
Mean 4089
RMS 360.5

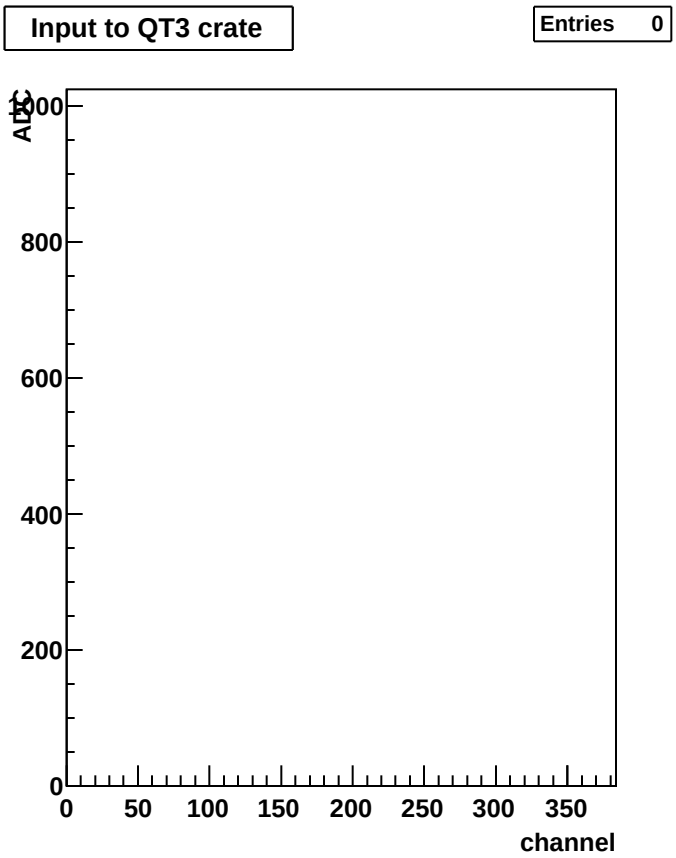

VPD-TAC-E
Entries 29
Mean 1295
RMS 146.4

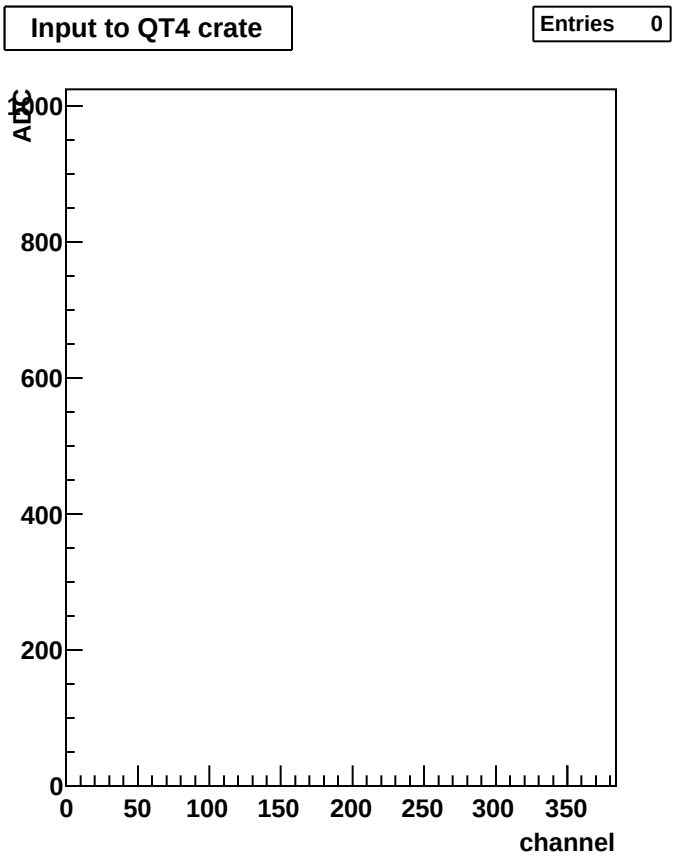

VPD-TAC-W
Entries 28
Mean 1453
RMS 164.2

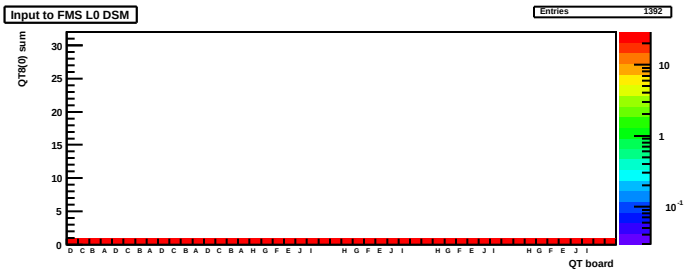

VPD-TAC-DIFF = 4096 + VPD-TAC-E - VPD-TAC-W
Entries 28
Mean 3937
RMS 189.3

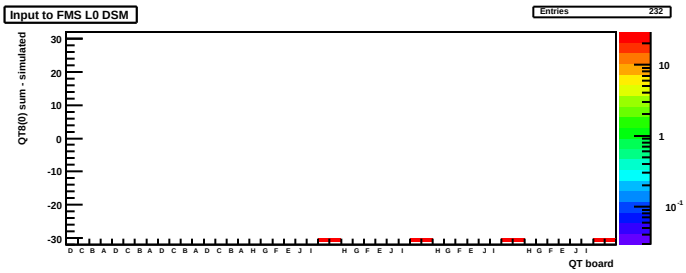

Input to QT1 crate
Entries 0
ADC
1000
800
600
400
200
0
0 50 100 150 200 250 300 350
channel

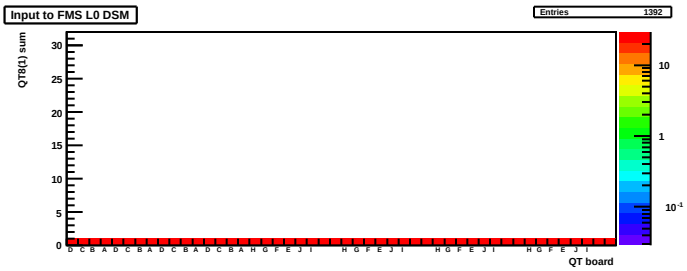

Input to QT2 crate
Entries 0
ADC
1000
800
600
400
200
0
0 50 100 150 200 250 300 350
channel

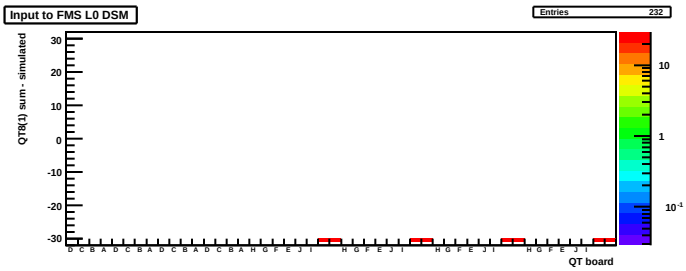

Input to QT3 crate
Entries 0
ADC
1000
800
600
400
200
0
0 50 100 150 200 250 300 350
channel

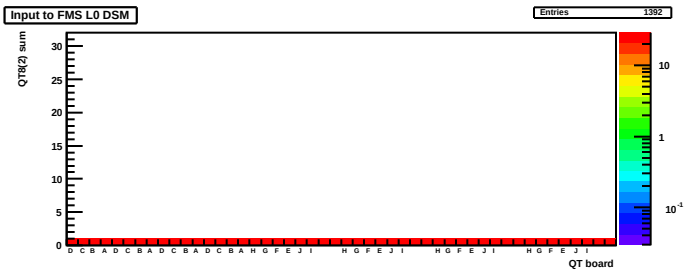

Input to QT4 crate
Entries 0
ADC
1000
800
600
400
200
0
0 50 100 150 200 250 300 350
channel

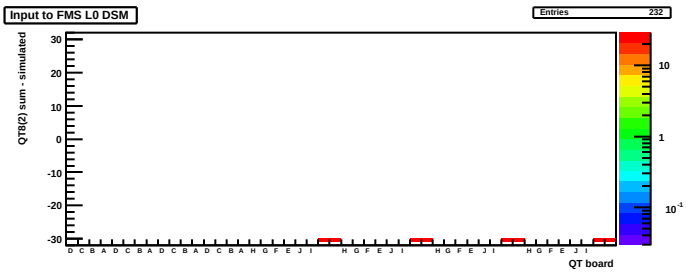

Input to FMS L0 DSM
Entries 1392
QT8(0) sum
QT board

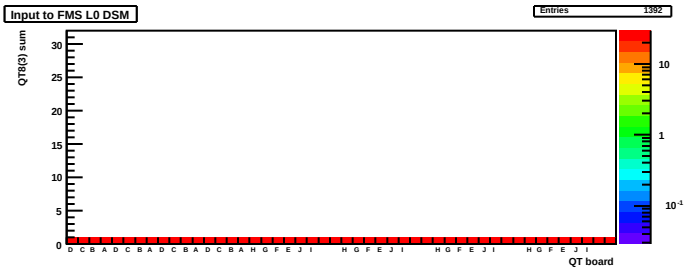

Input to FMS L0 DSM
Entries 232
QT8(0) sum - simulated
QT board

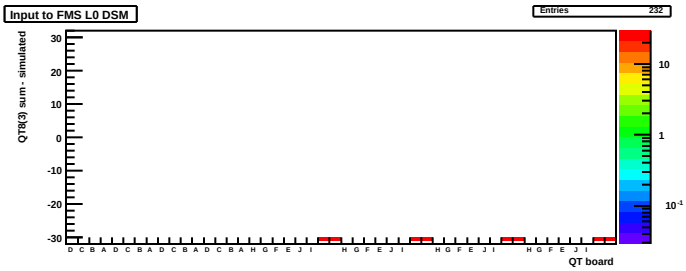

Input to FMS L0 DSM
Entries 1392
QT8(1) sum
QT board

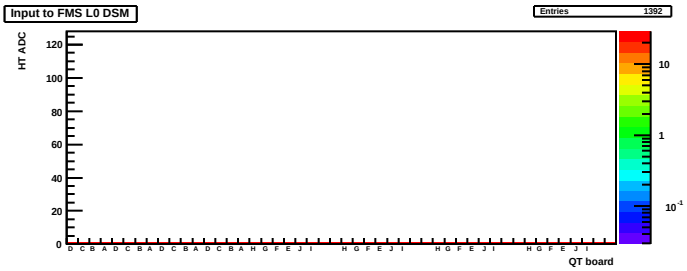

Input to FMS L0 DSM
Entries 232
QT8(1) sum - simulated
QT board

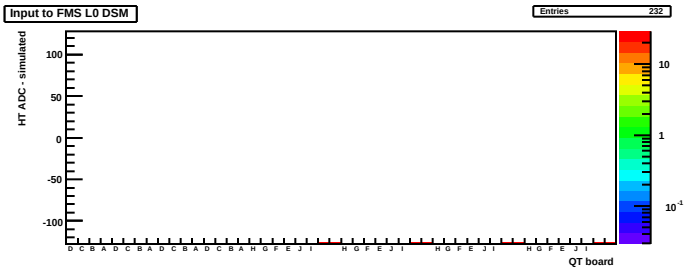

Input to FMS L0 DSM
Entries 1392
QT8(2) sum
QT board

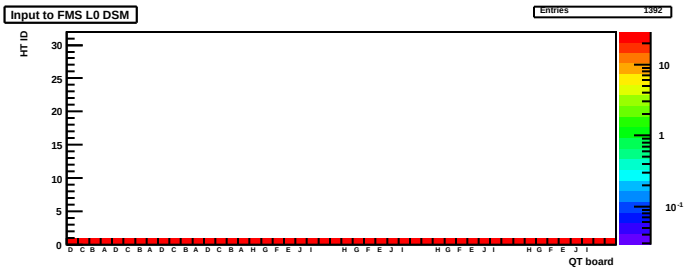

Input to FMS L0 DSM
Entries 232
QT8(2) sum - simulated
QT board

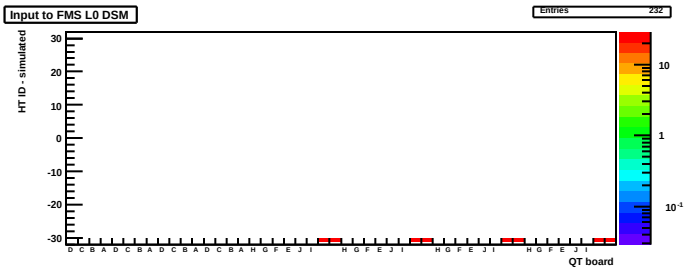

Input to FMS L0 DSM
Entries 1392
QT8(3) sum
QT board

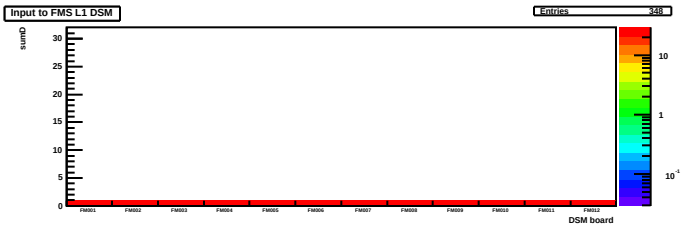

Input to FMS L0 DSM
Entries 232
QT8(3) sum - simulated
QT board

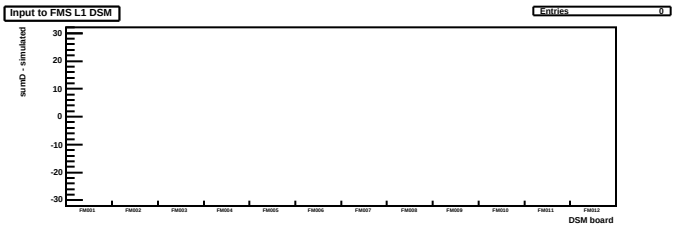

Input to FMS L0 DSM
Entries 1392
HT ADC
QT board

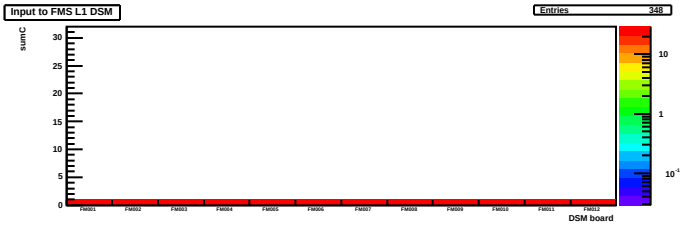

Input to FMS L0 DSM
Entries 232
HT ADC - simulated
QT board

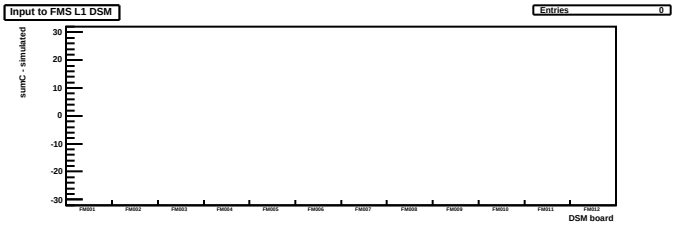

Input to FMS L0 DSM
Entries 1392
HT ID
QT board

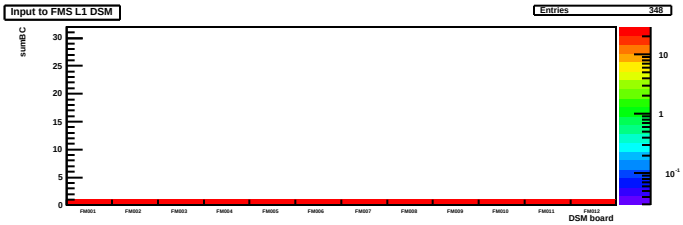

Input to FMS L0 DSM
Entries 232
HT ID - simulated
QT board

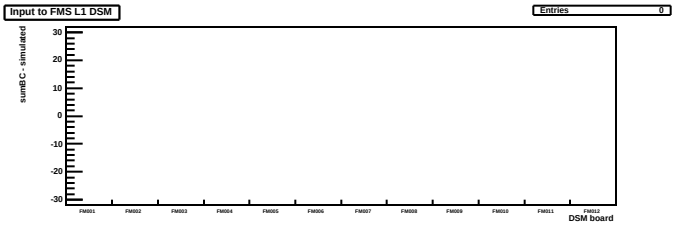

Input to FMS L1 DSM
Entries 348
sumD
DSM board

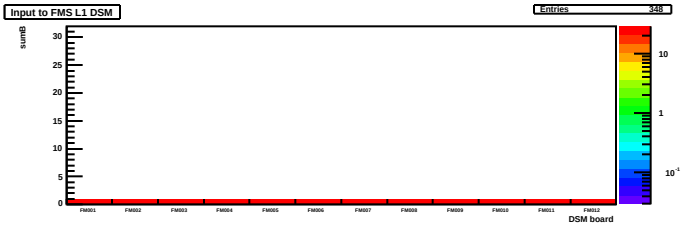

Input to FMS L1 DSM
Entries 0
sumD - simulated
DSM board

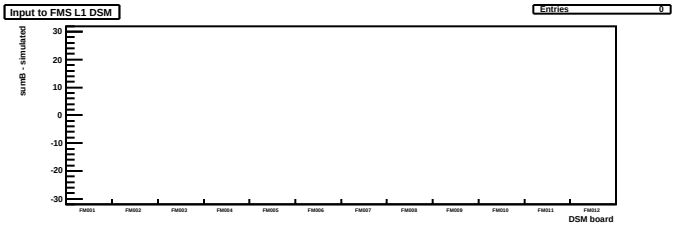

Input to FMS L1 DSM
Entries 348
sumC
DSM board

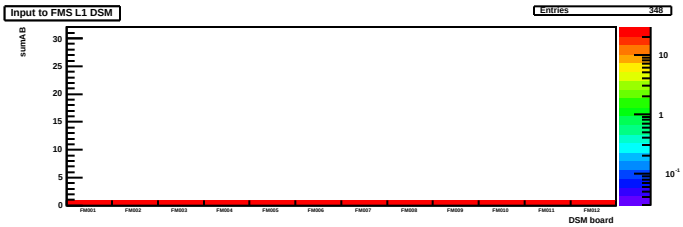

Input to FMS L1 DSM
Entries 0
sumC - simulated
DSM board

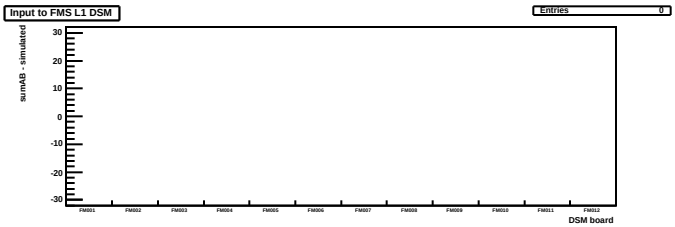

Input to FMS L1 DSM
Entries 348
sumBC
DSM board

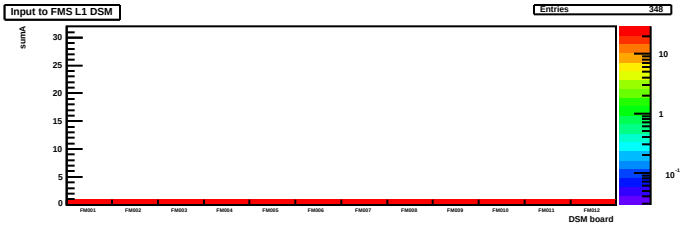

Input to FMS L1 DSM
Entries 0
sumBC - simulated
DSM board

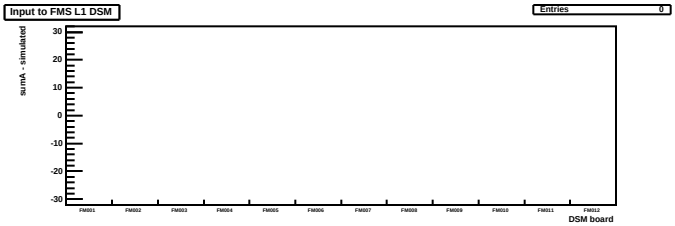

Input to FMS L1 DSM
Entries 348
sumB
DSM board

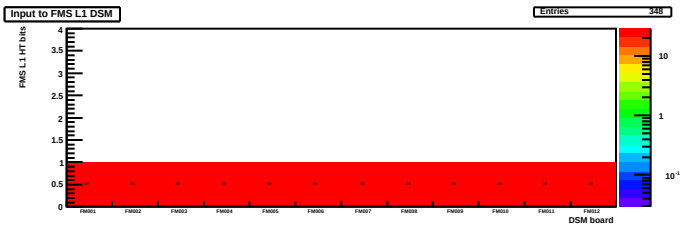

Input to FMS L1 DSM
Entries 0
sumB - simulated
DSM board

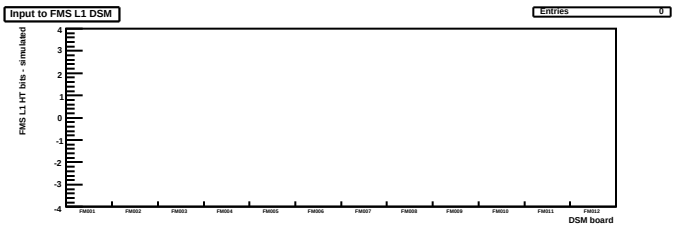

Input to FMS L1 DSM
Entries 348
sumAB
DSM board

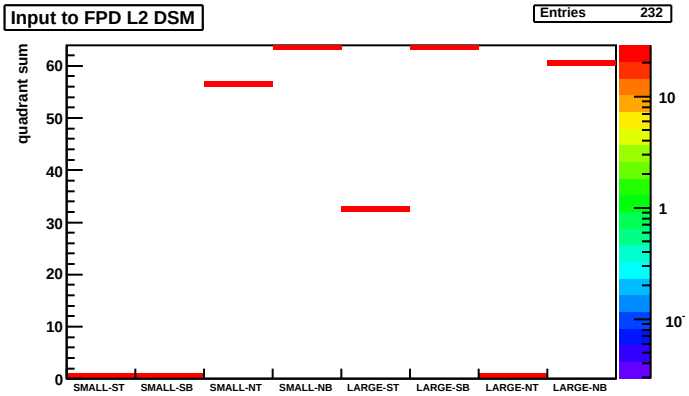

Input to FMS L1 DSM
Entries 0
sumAB - simulated
DSM board

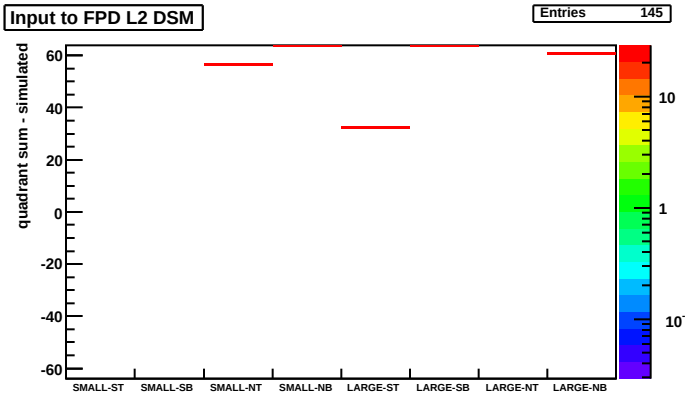

Input to FMS L1 DSM
Entries 348
sumA
DSM board

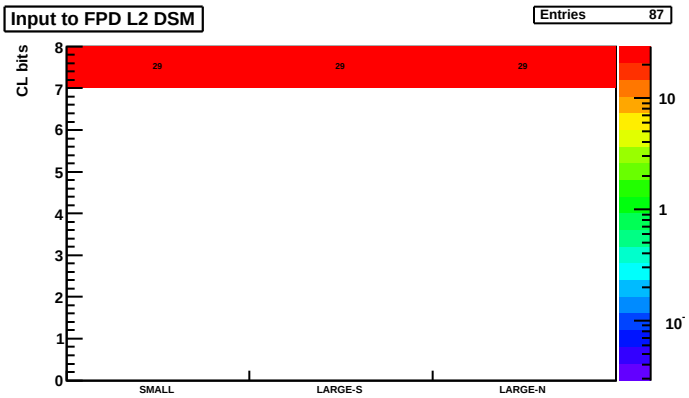

Input to FMS L1 DSM
Entries 0
sumA - simulated
DSM board

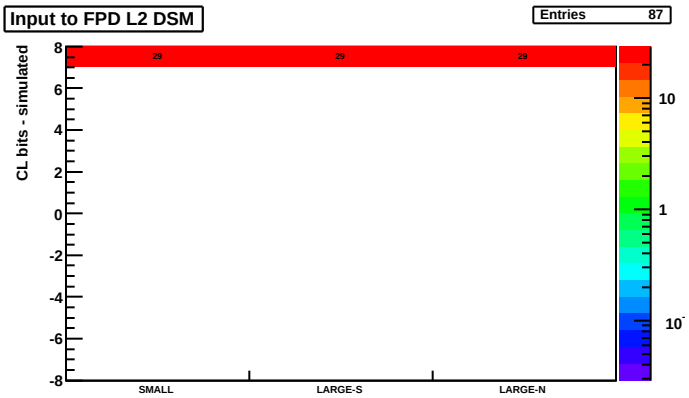

Input to FMS L1 DSM
Entries 348
FMS L1 HT bits
DSM board

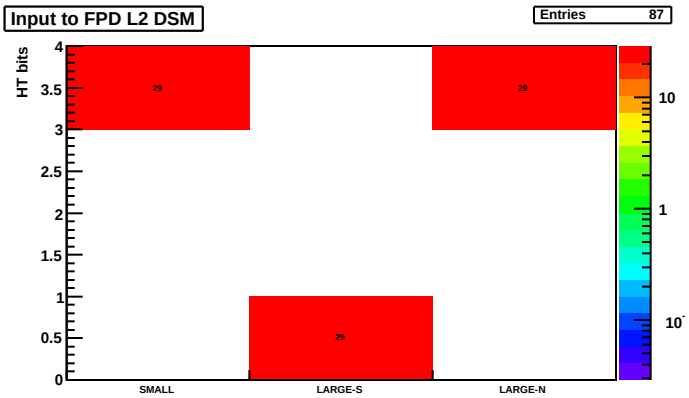

Input to FMS L1 DSM
Entries 0
FMS L1 HT bits - simulated
DSM board

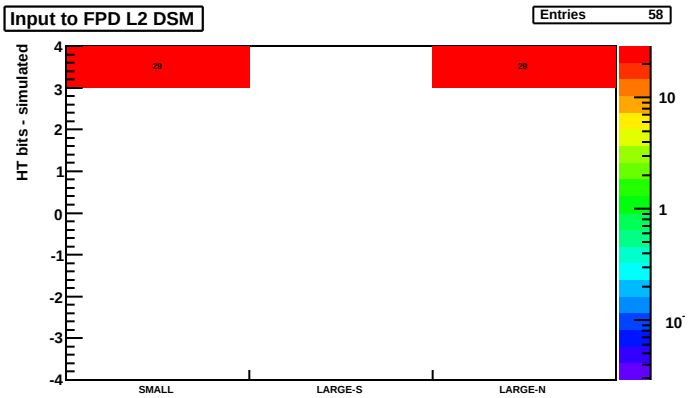

Input to FPD L2 DSM
Entries 232
quadrant sum
SMALL-ST
SMALL-SB
SMALL-NT
SMALL-NB
LARGE-ST
LARGE-SB
LARGE-NT
LARGE-NB

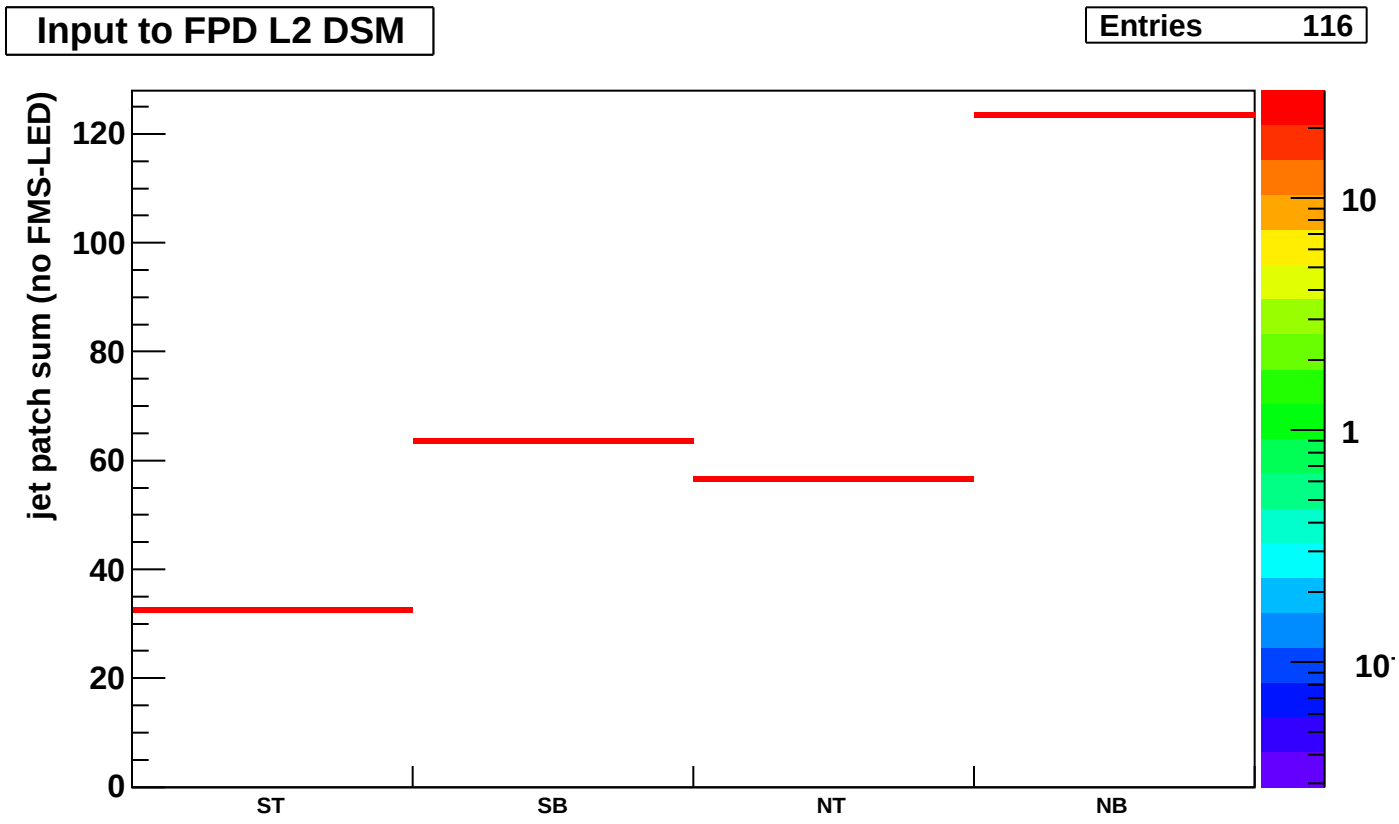

Input to FPD L2 DSM
Entries 145
quadrant sum - simulated
SMALL-ST
SMALL-SB
SMALL-NT
SMALL-NB
LARGE-ST
LARGE-SB
LARGE-NT
LARGE-NB

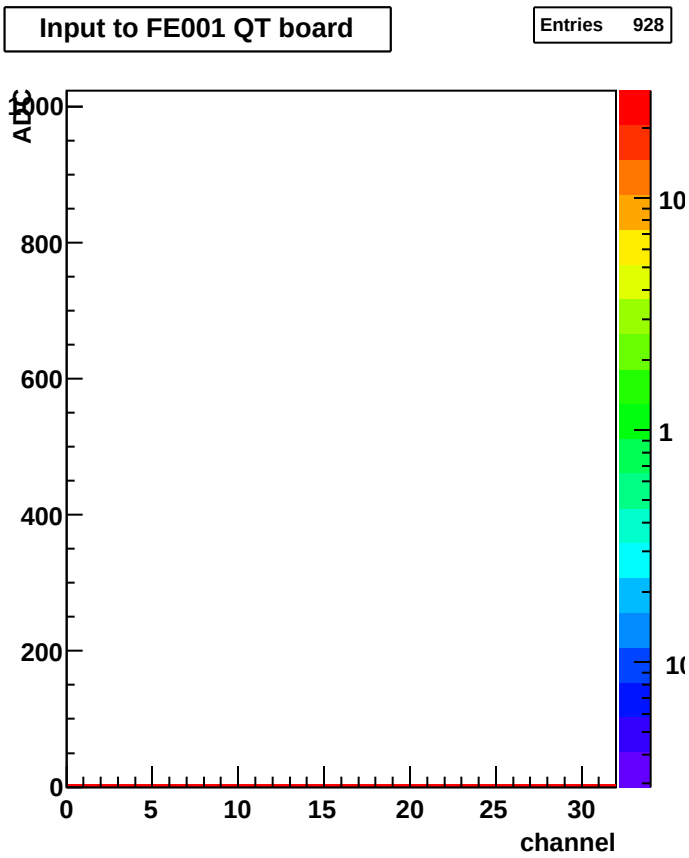

Input to FPD L2 DSM
Entries 87
CL bits
SMALL
LARGE-S
LARGE-N

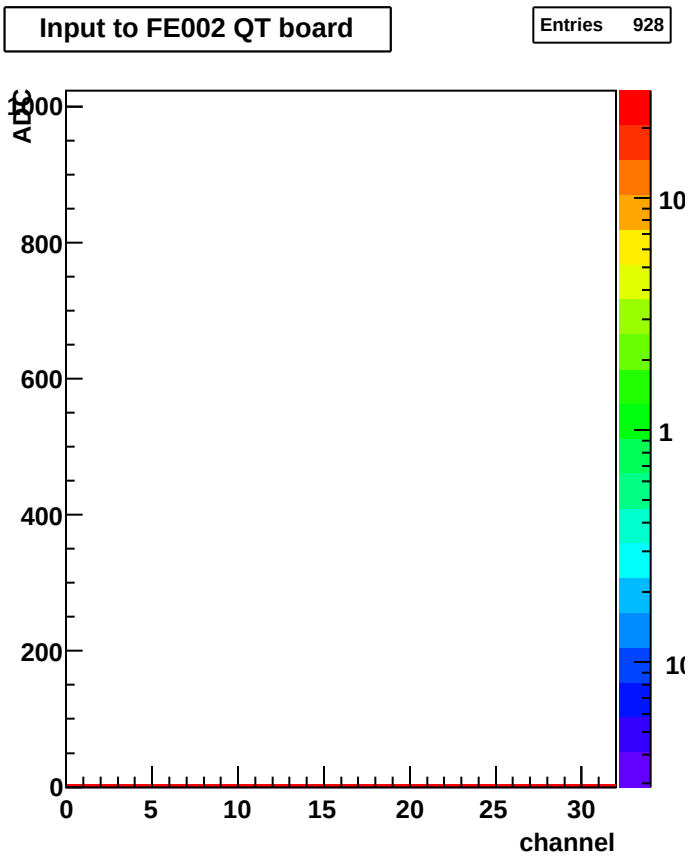

Input to FPD L2 DSM
Entries 87
CL bits - simulated
SMALL
LARGE-S
LARGE-N

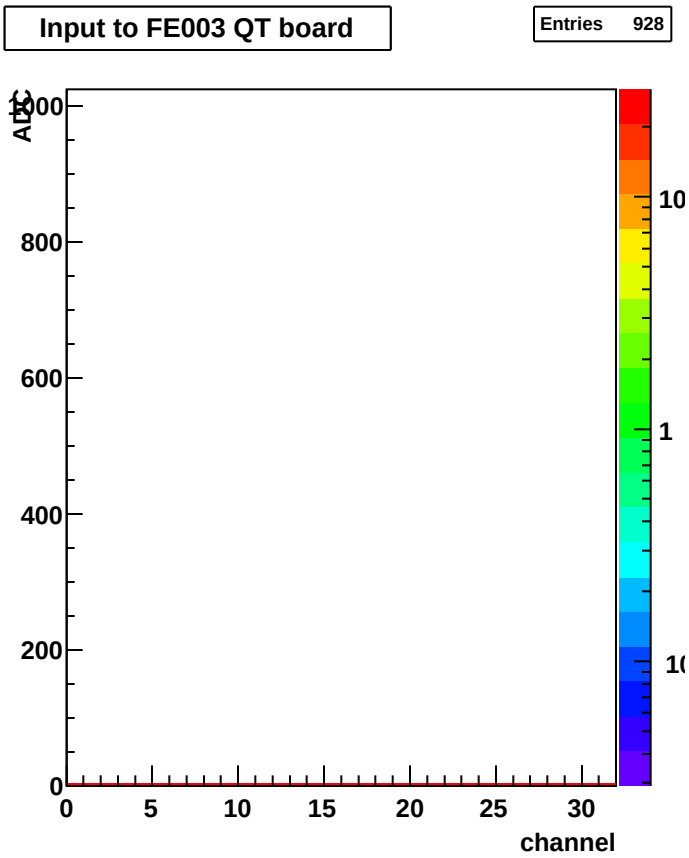

Input to FPD L2 DSM
Entries 87
HT bits
SMALL
LARGE-S
LARGE-N

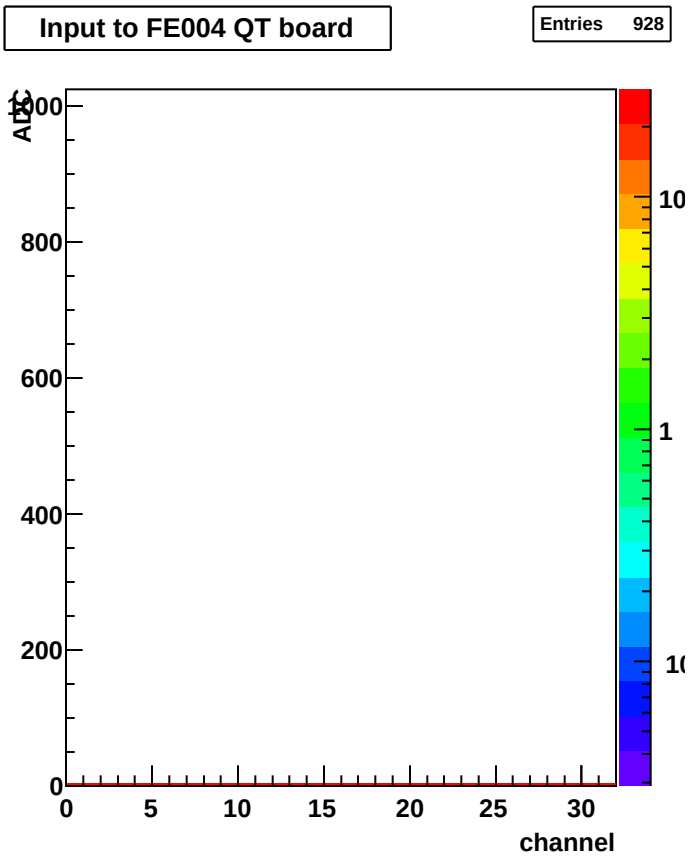

Input to FPD L2 DSM
Entries 58
HT bits - simulated
SMALL
LARGE-S
LARGE-N

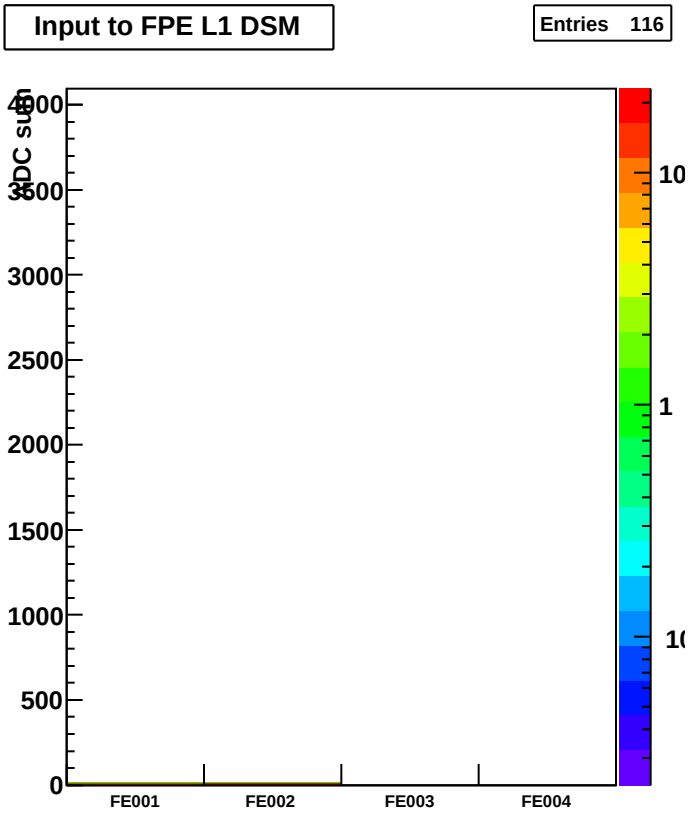

Input to FPD L2 DSM
Entries 116
jet patch sum (no FMS-LED)
0
20
40
60
80
100
120
ST
SB
NT
NB
10
1
10

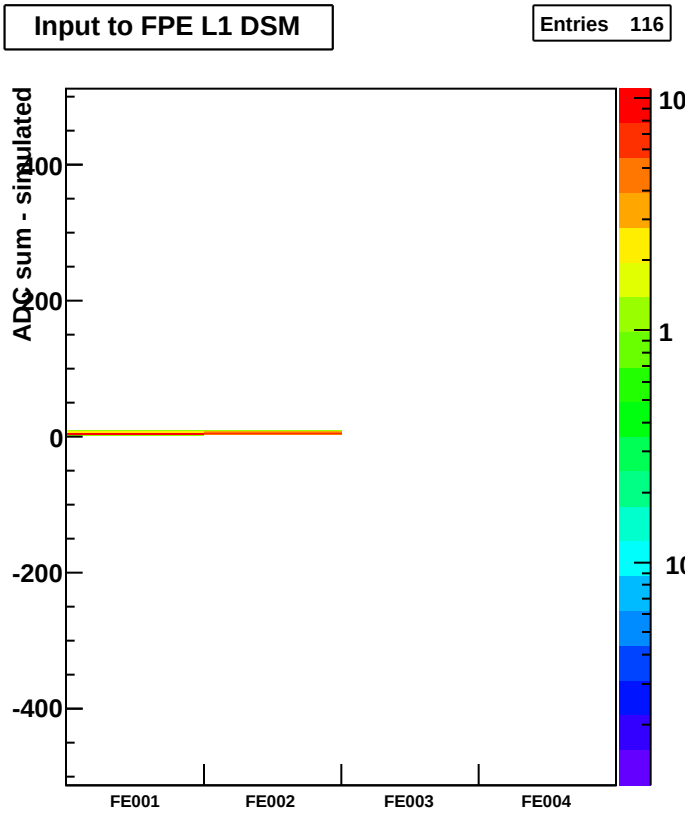

Input to FE001 QT board
Entries 928
ADC
channel


Input to FE002 QT board
Entries 928
ADC
channel

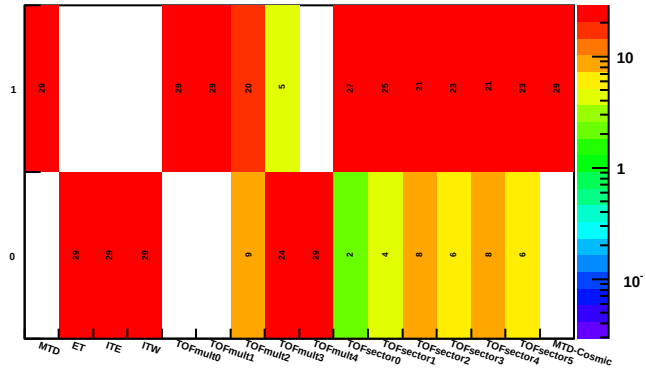

Input to FE003 QT board
Entries 928
ADC
channel


Input to FE004 QT board
Entries 928
ADC
channel

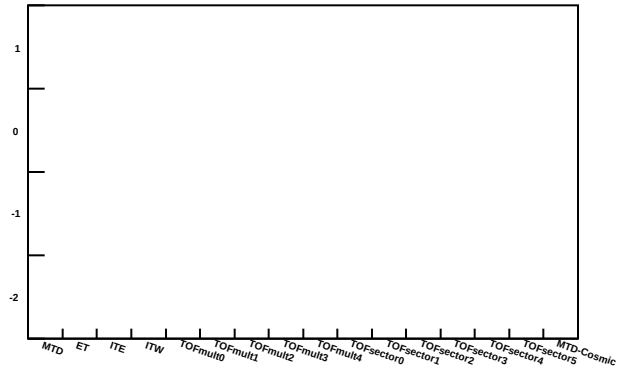

Input to FPE L1 DSM
Entries 116
ADC sum
4000
3500
3000
2500
2000
1500
1000
500
0
FE001
FE002
FE003
FE004
10
1
10


Input to FPE L1 DSM
Entries 116
ADC sum - simulated
0
-200
-400
FE001
FE002
FE003
FE004
10
1
10

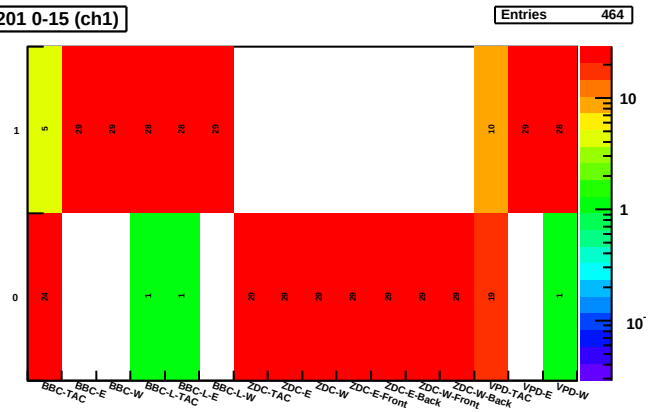
TF201 0-15 (ch0)



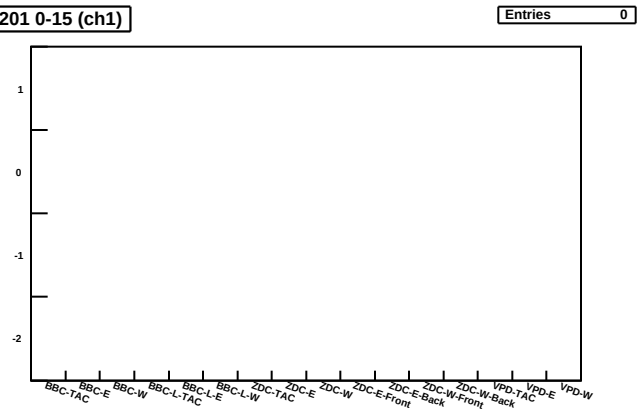
TF201 0-15 (ch0)



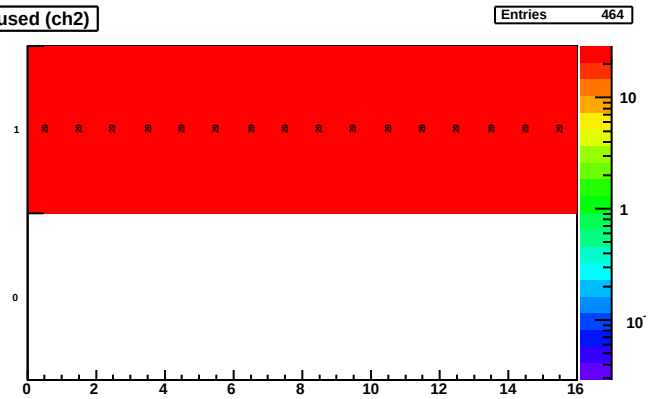
VT201 0-15 (ch1)

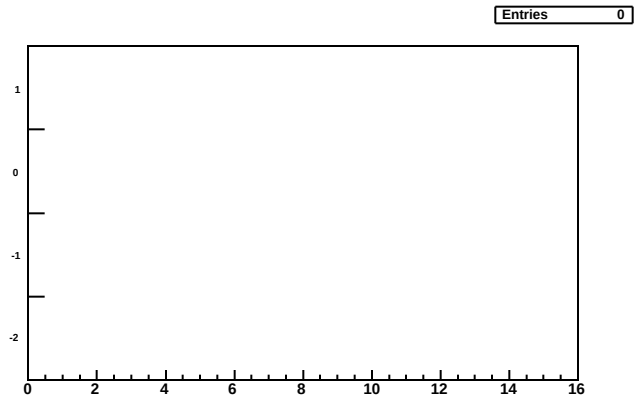


VT201 0-15 (ch1)

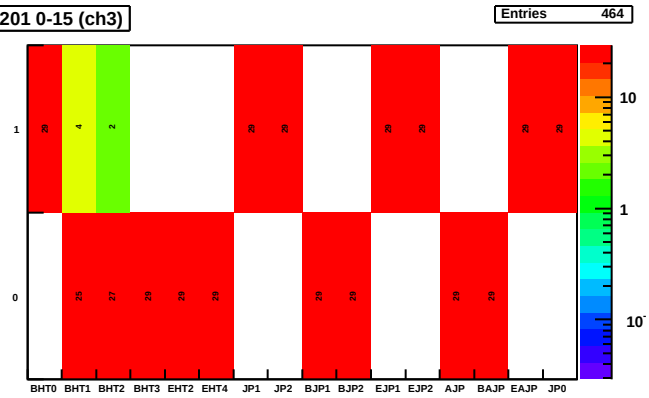


Unused (ch2)

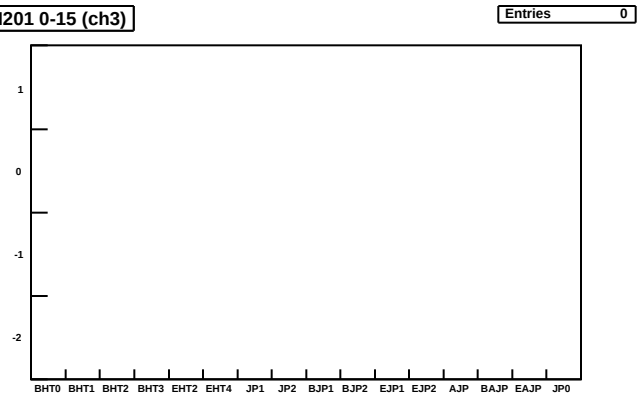




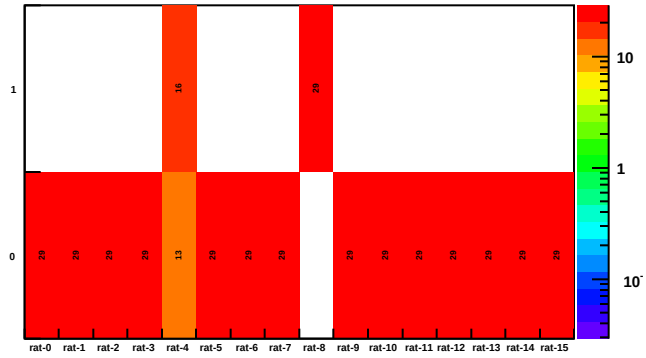
EM201 0-15 (ch3)

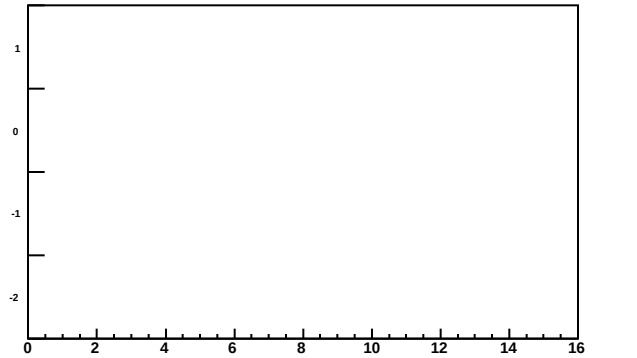


EM201 0-15 (ch3)

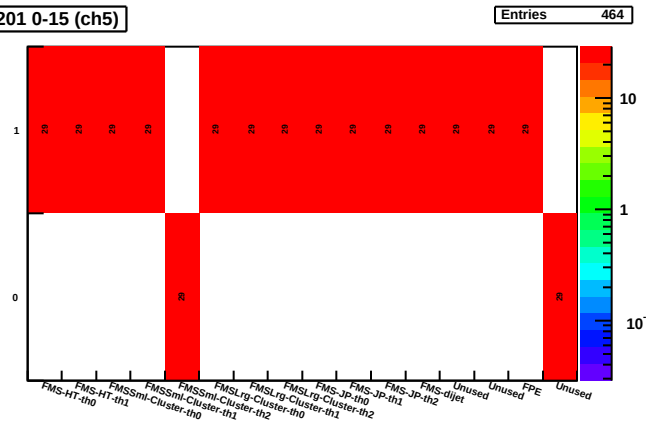


RAT board (ch4)

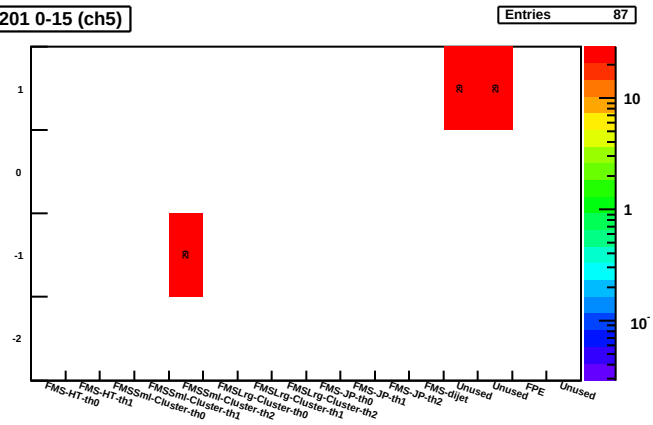




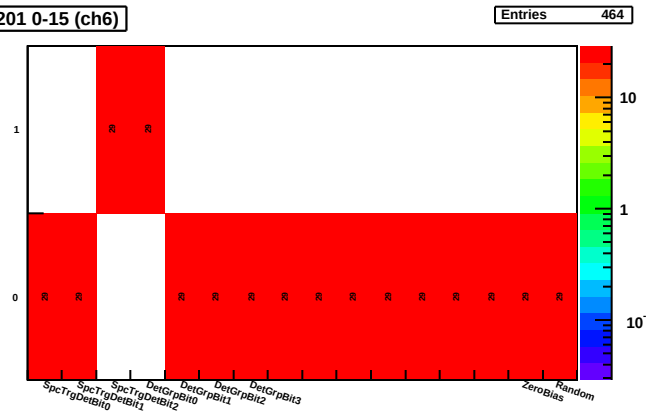
FP201 0-15 (ch5)

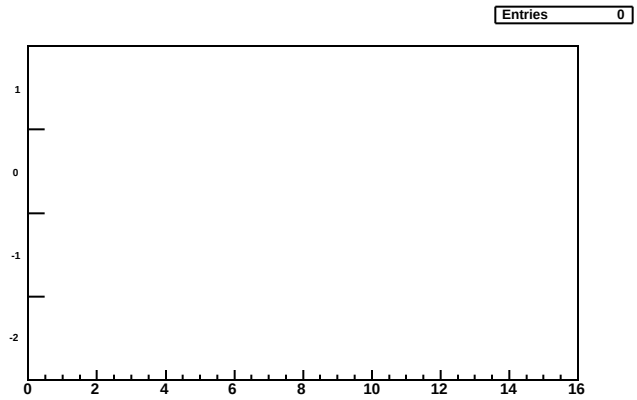
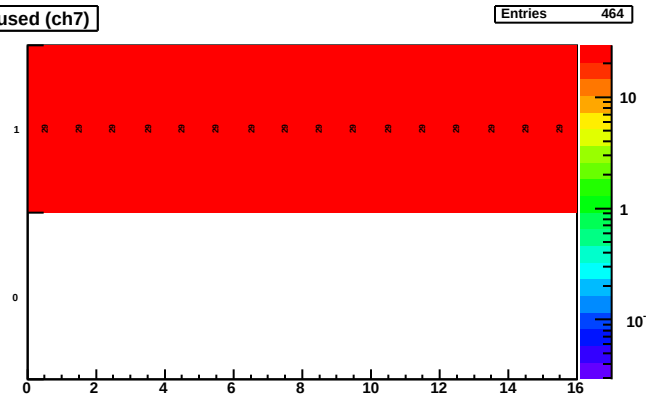
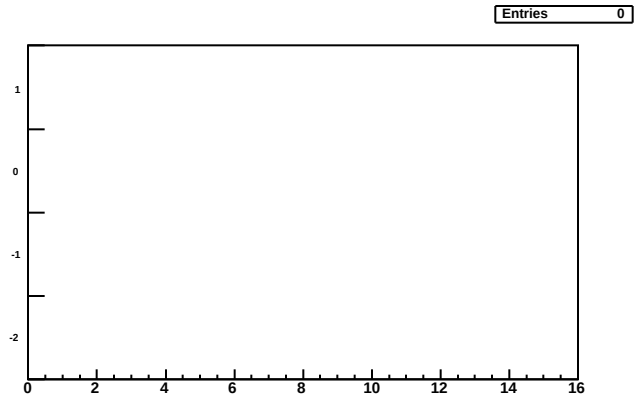


FP201 0-15 (ch5)



ST201 0-15 (ch6)





Unused (ch7)