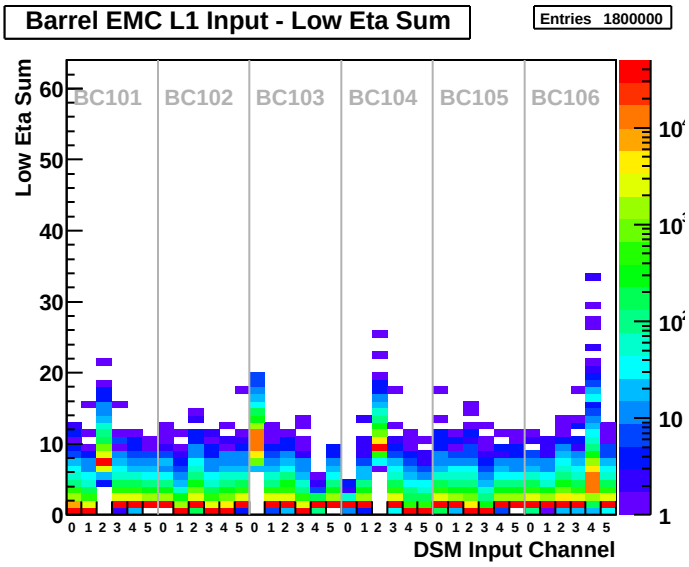
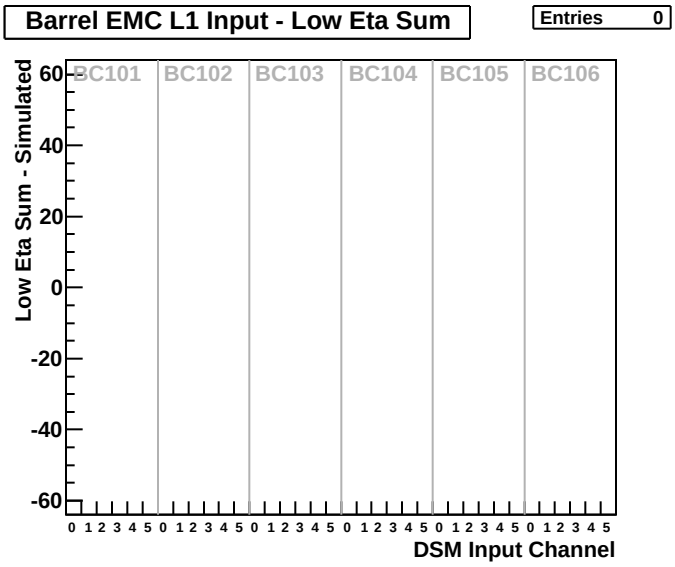
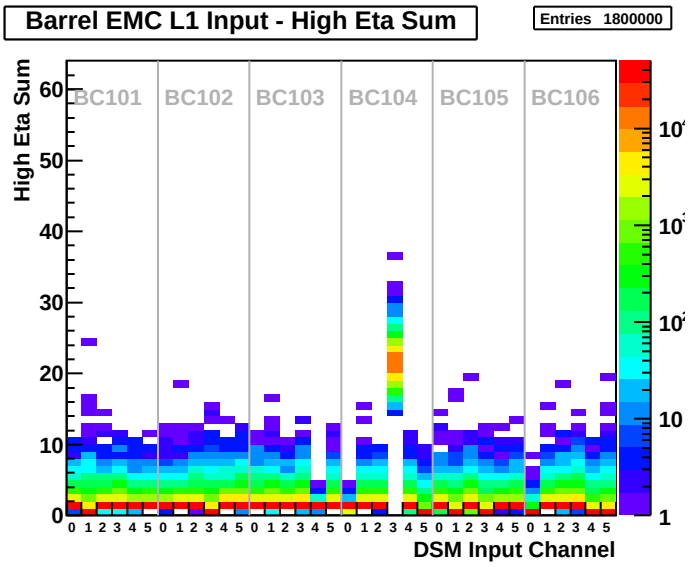
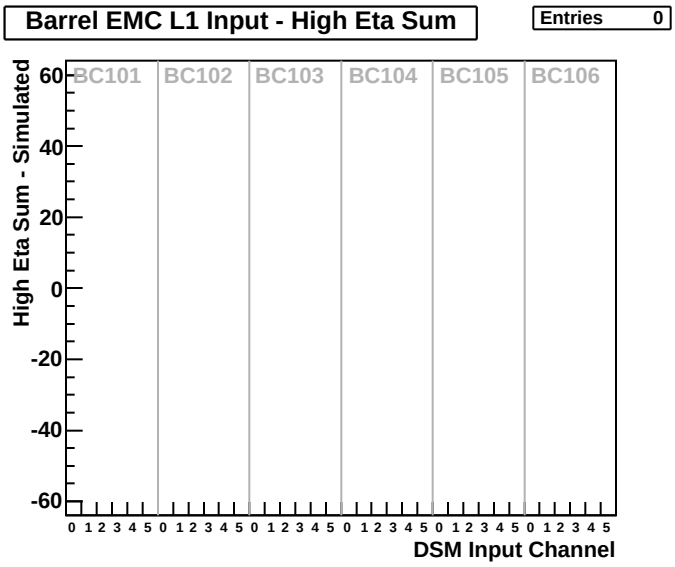
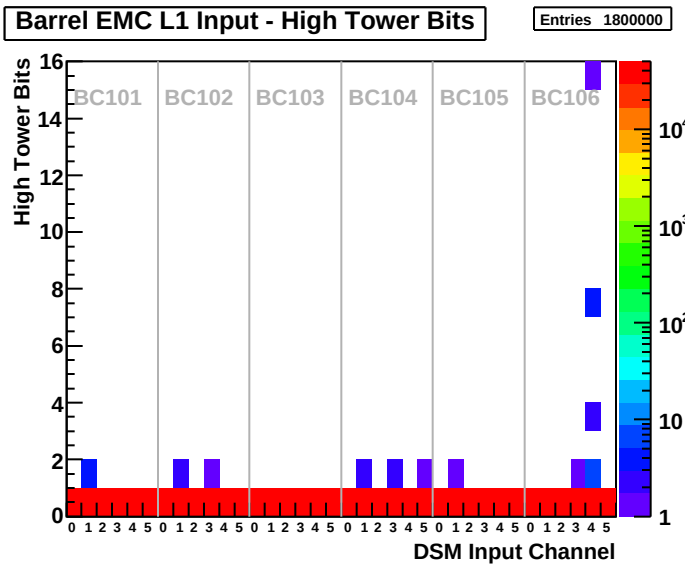
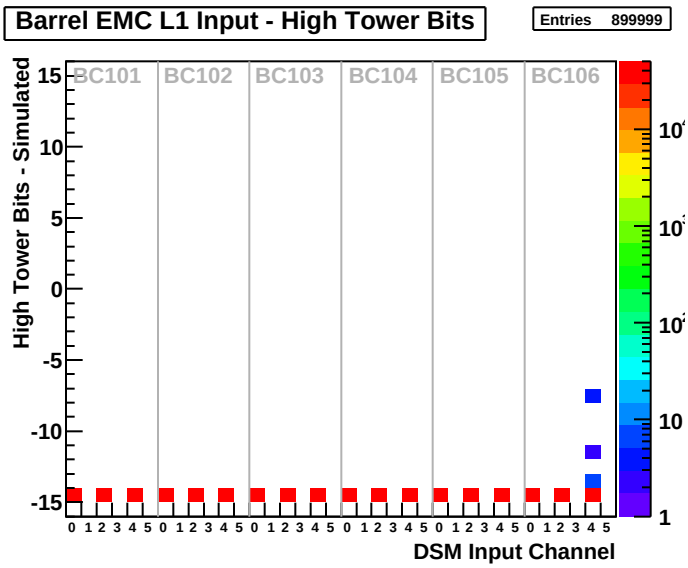

Barrel EMC L1 Input - Low Eta Sum
Entries 1800000
Low Eta Sum
BC101
BC102
BC103
BC104
BC105
BC106
DSM Input Channel

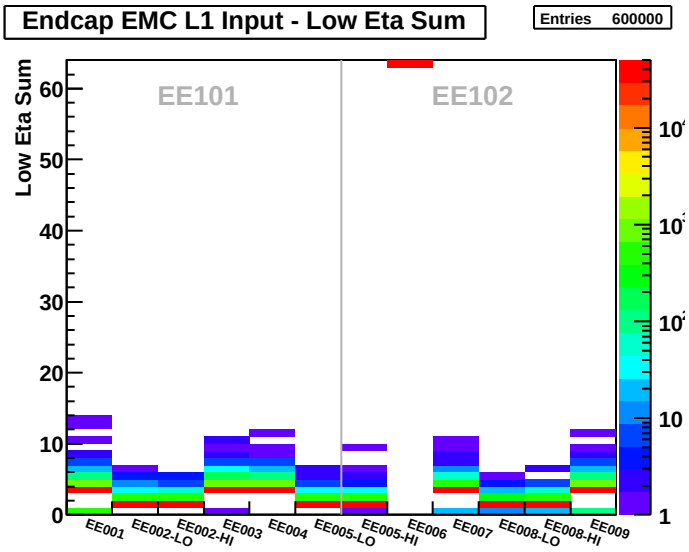

Barrel EMC L1 Input - Low Eta Sum
Entries 0
Low Eta Sum - Simulated
BC101
BC102
BC103
BC104
BC105
BC106
DSM Input Channel

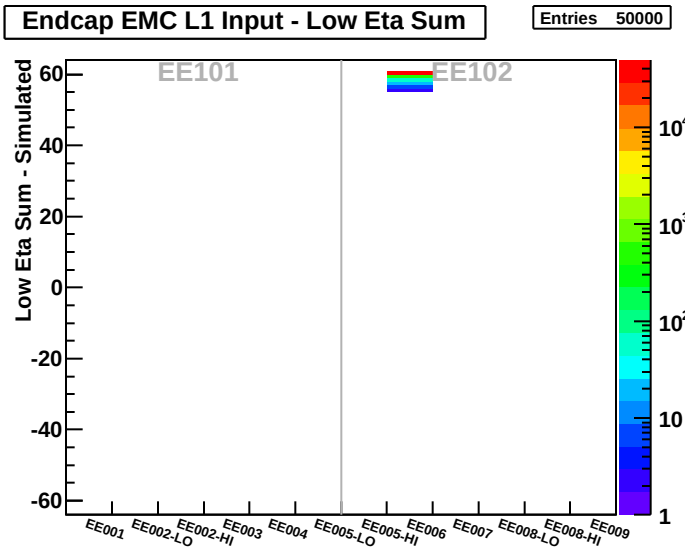

Barrel EMC L1 Input - High Eta Sum
Entries 1800000
High Eta Sum
BC101
BC102
BC103
BC104
BC105
BC106
DSM Input Channel

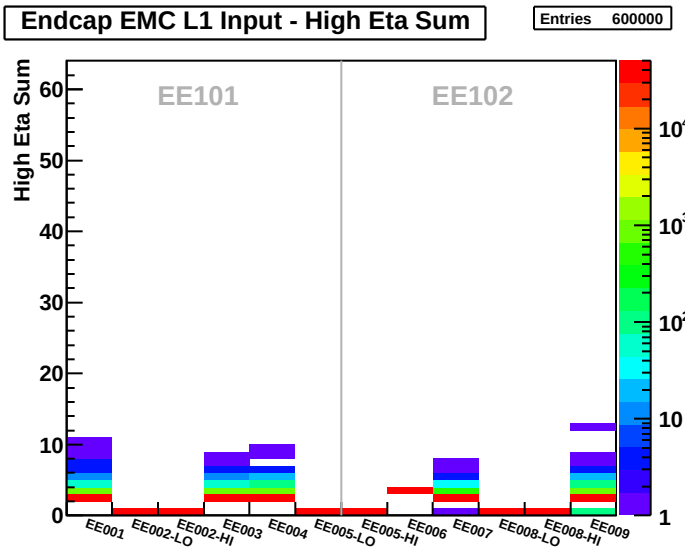

Barrel EMC L1 Input - High Eta Sum
Entries 0
High Eta Sum - Simulated
BC101
BC102
BC103
BC104
BC105
BC106
DSM Input Channel

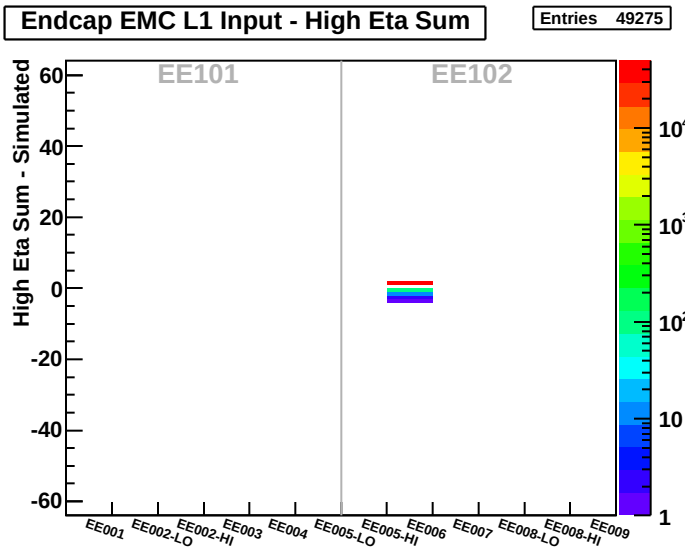

Barrel EMC L1 Input - High Tower Bits
Entries 1800000
High Tower Bits
BC101
BC102
BC103
BC104
BC105
BC106
DSM Input Channel

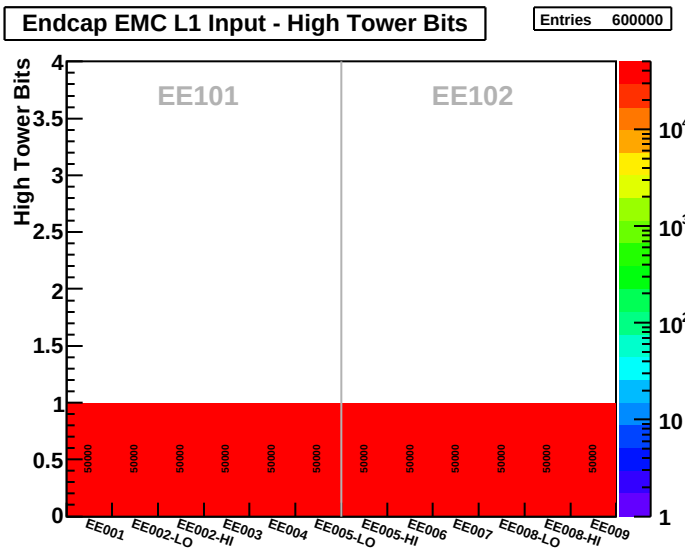

Barrel EMC L1 Input - High Tower Bits
Entries 899999
High Tower Bits - Simulated
BC101
BC102
BC103
BC104
BC105
BC106
DSM Input Channel

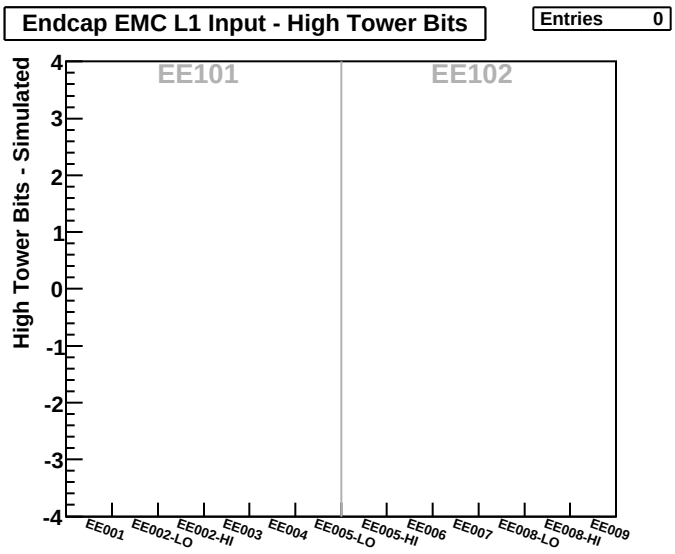

Endcap EMC L1 Input - Low Eta Sum
Entries 600000
Low Eta Sum
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

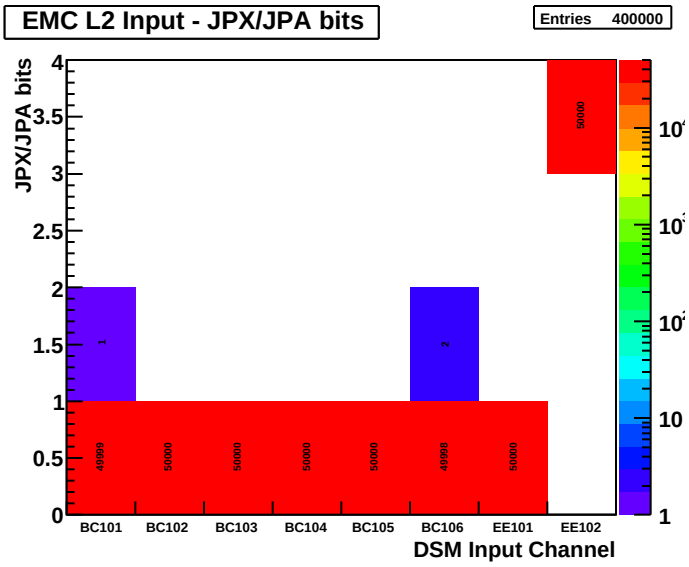

Endcap EMC L1 Input - Low Eta Sum
Entries 50000
Low Eta Sum - Simulated
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

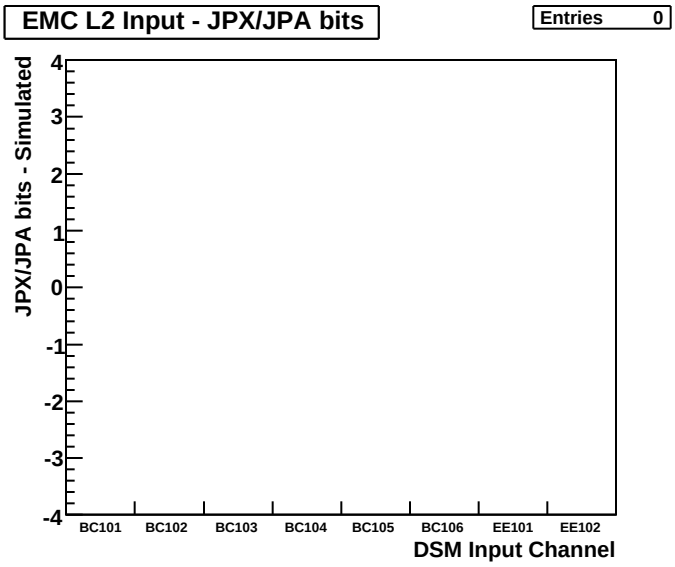

Endcap EMC L1 Input - High Eta Sum
Entries 600000
High Eta Sum
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

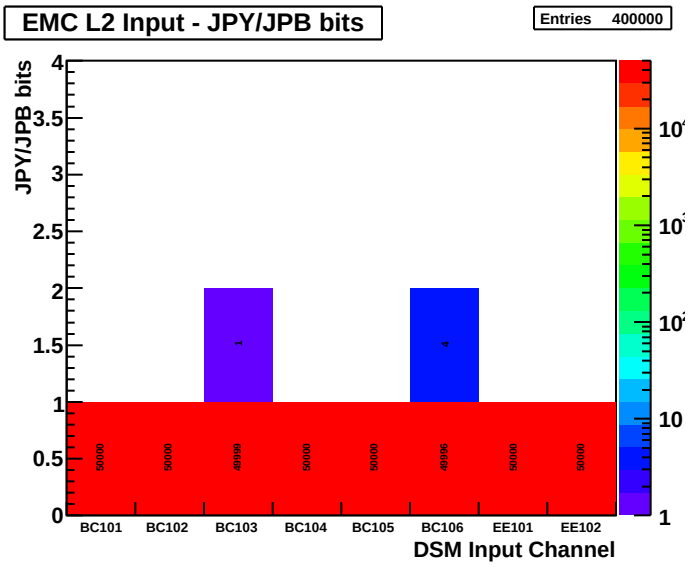

Endcap EMC L1 Input - High Eta Sum
Entries 49275
High Eta Sum - Simulated
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

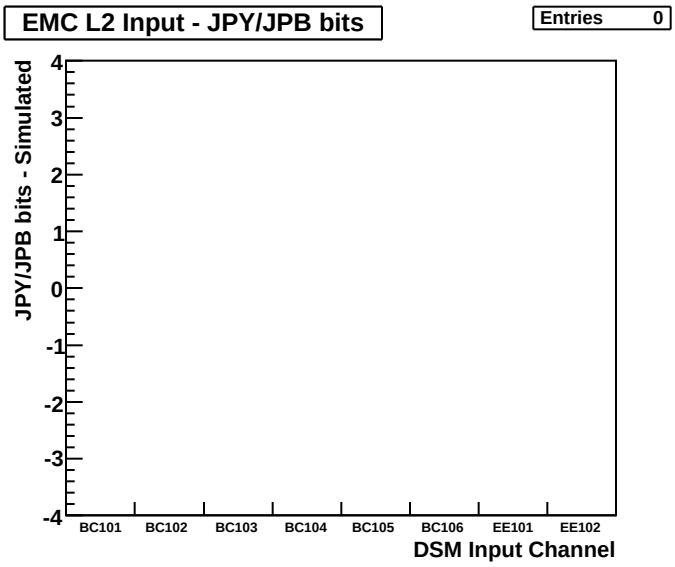

Endcap EMC L1 Input - High Tower Bits
Entries 600000
High Tower Bits
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

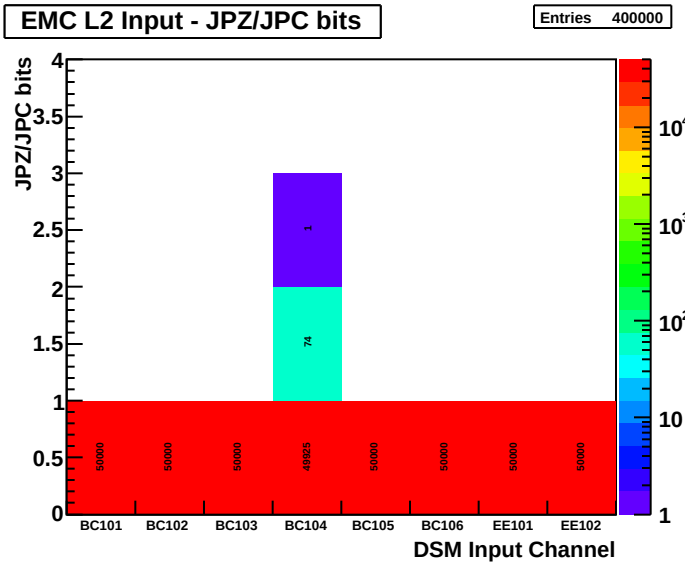

Endcap EMC L1 Input - High Tower Bits
Entries 0
High Tower Bits - Simulated
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

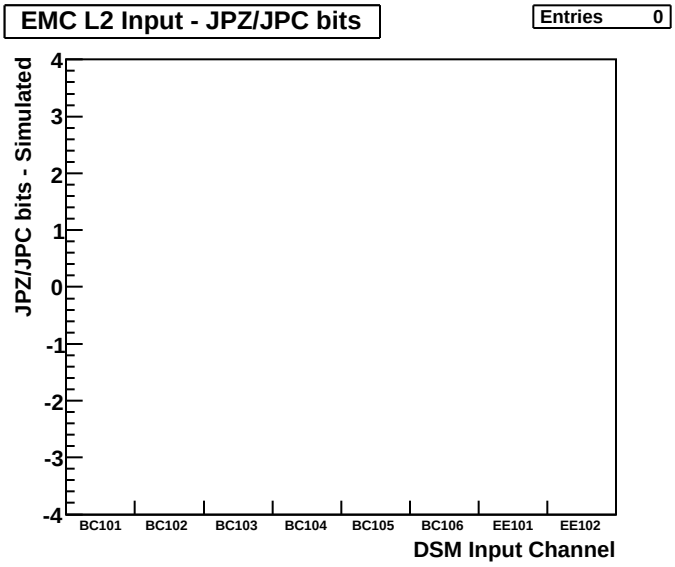

EMC L2 Input - JPX/JPA bits
Entries 400000
JPX/JPA bits
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102
49999 50000 50000 50000 50000 49998 50000
1 2
50000

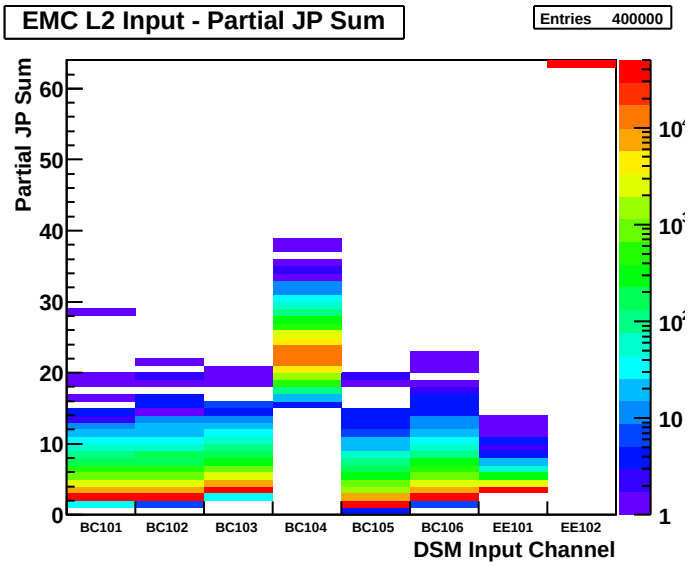

EMC L2 Input - JPX/JPA bits
Entries 0
JPX/JPA bits - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

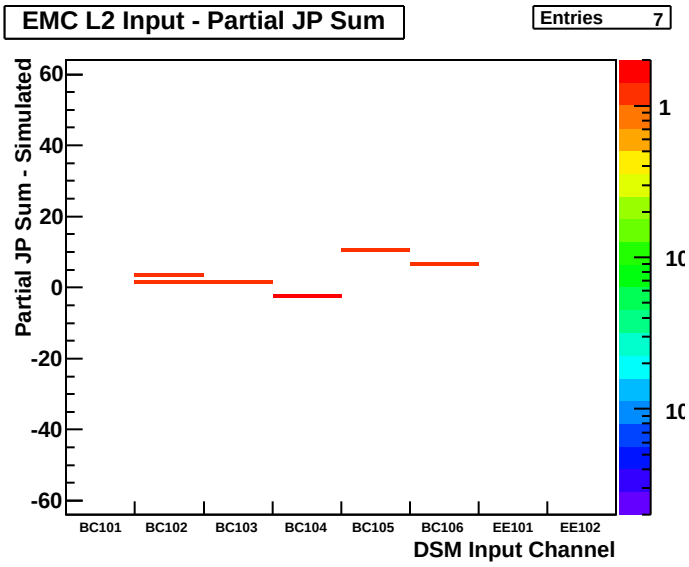

EMC L2 Input - JPY/JPB bits
Entries 400000
JPY/JPB bits
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102
50000 50000 49999 50000 50000 49996 50000 50000
1 4

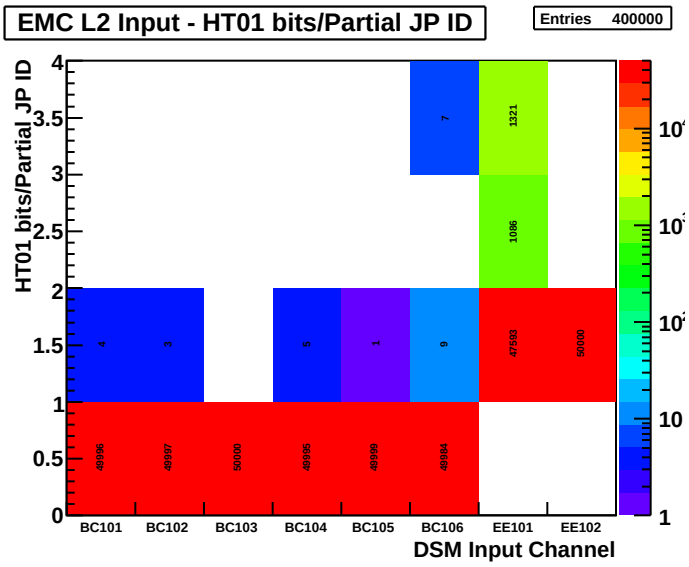

EMC L2 Input - JPY/JPB bits
Entries 0
JPY/JPB bits - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

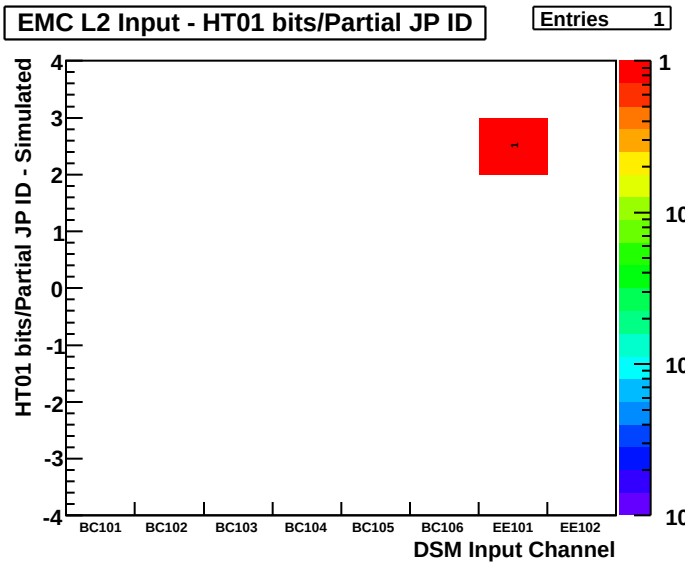

EMC L2 Input - JPZ/JPC bits
Entries 400000
JPZ/JPC bits
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102
50000 50000 50000 49925 50000 50000 50000 50000
1 74

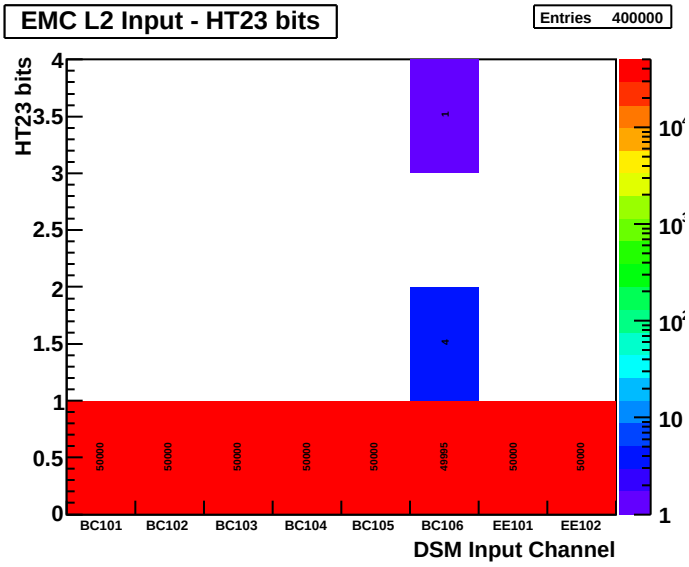

EMC L2 Input - JPZ/JPC bits
Entries 0
JPZ/JPC bits - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

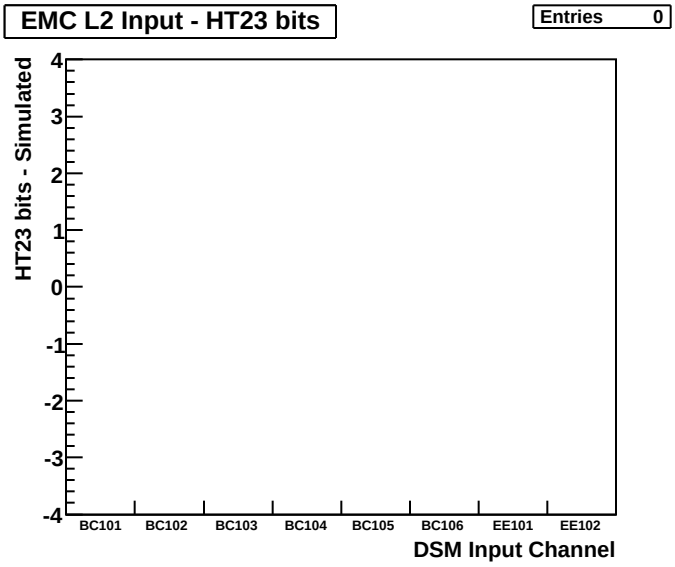

EMC L2 Input - Partial JP Sum
Entries 400000
Partial JP Sum
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

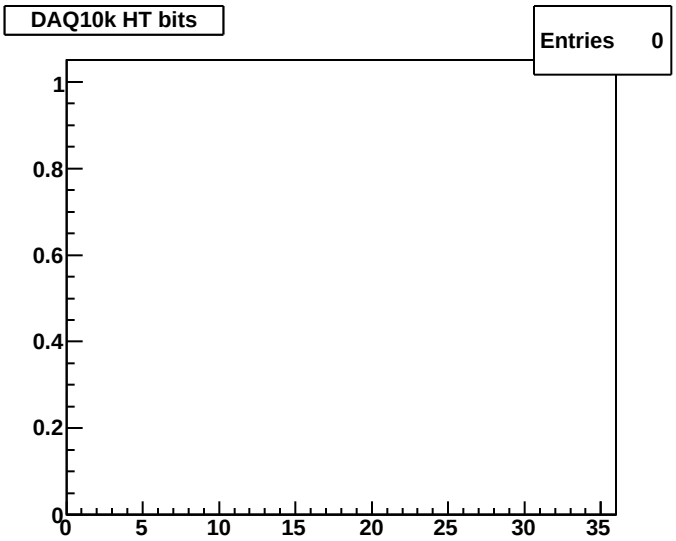

EMC L2 Input - Partial JP Sum
Entries 7
Partial JP Sum - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

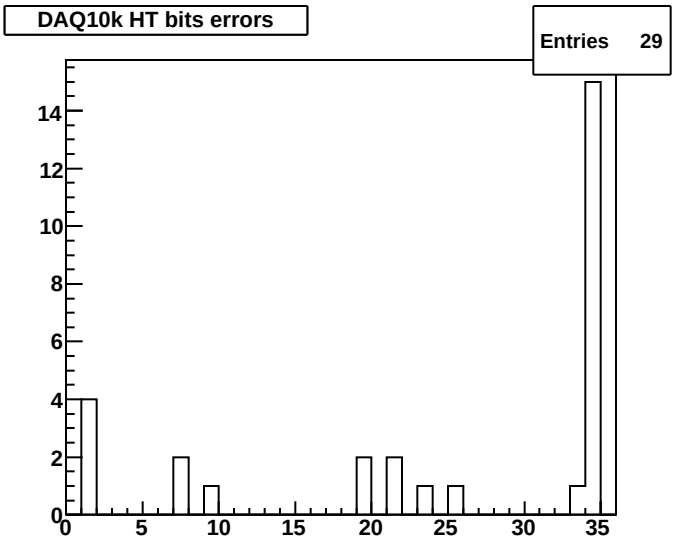

EMC L2 Input - HT01 bits/Partial JP ID
Entries 400000
HT01 bits/Partial JP ID
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

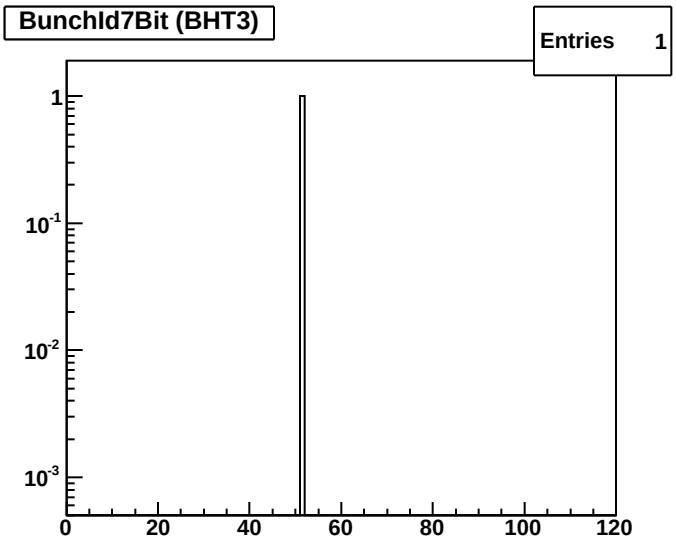

EMC L2 Input - HT01 bits/Partial JP ID
Entries 1
HT01 bits/Partial JP ID - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

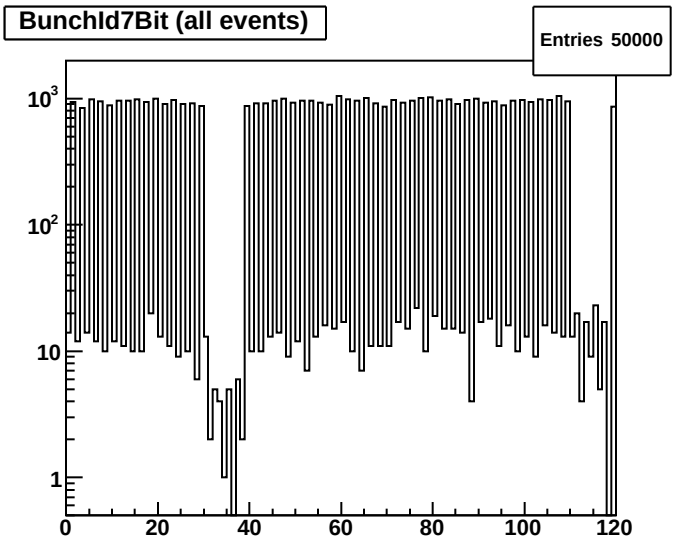

EMC L2 Input - HT23 bits
Entries 400000
HT23 bits
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

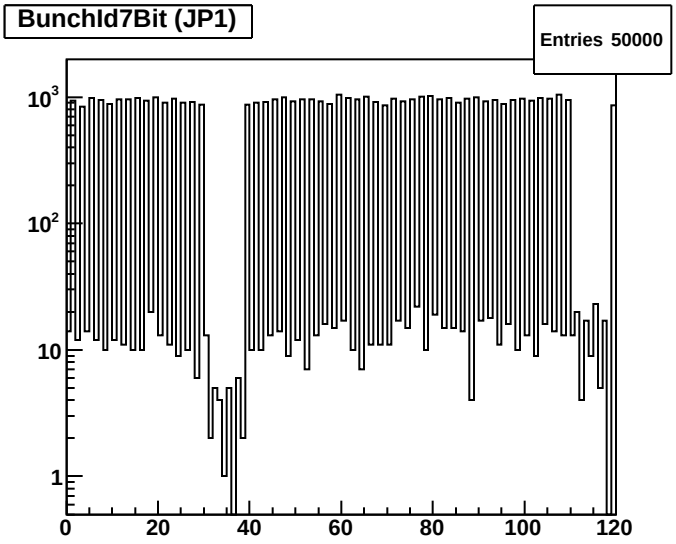

EMC L2 Input - HT23 bits
Entries 0
HT23 bits - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

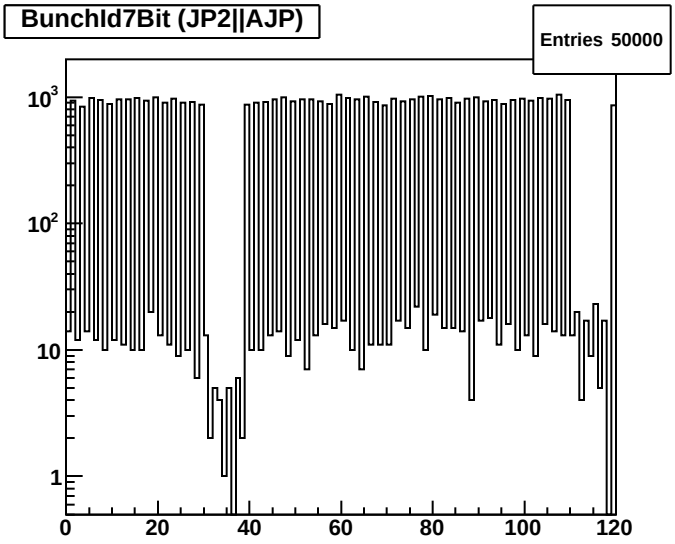

DAQ10k HT bits
Entries 0

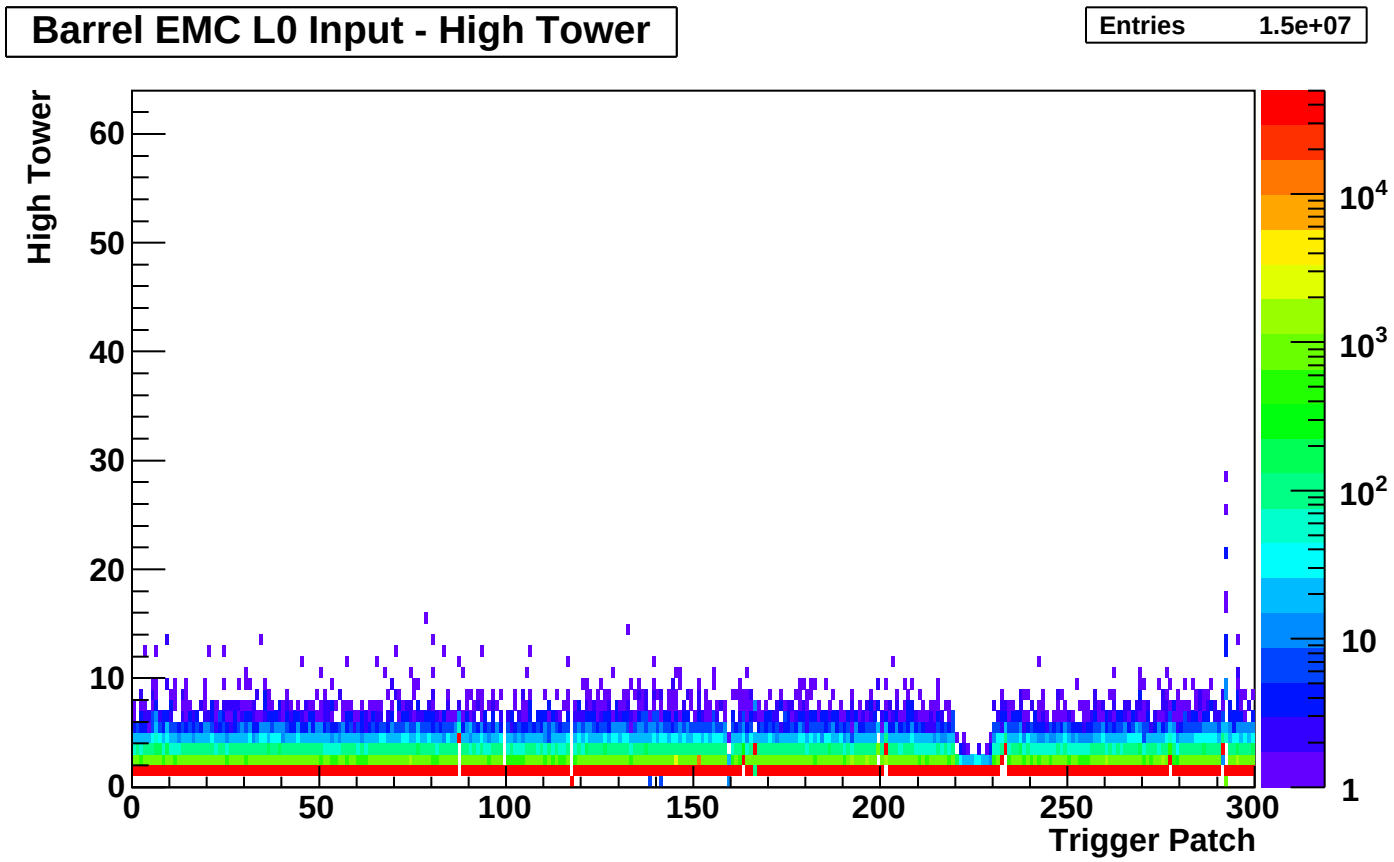

DAQ10k HT bits errors
Entries 29

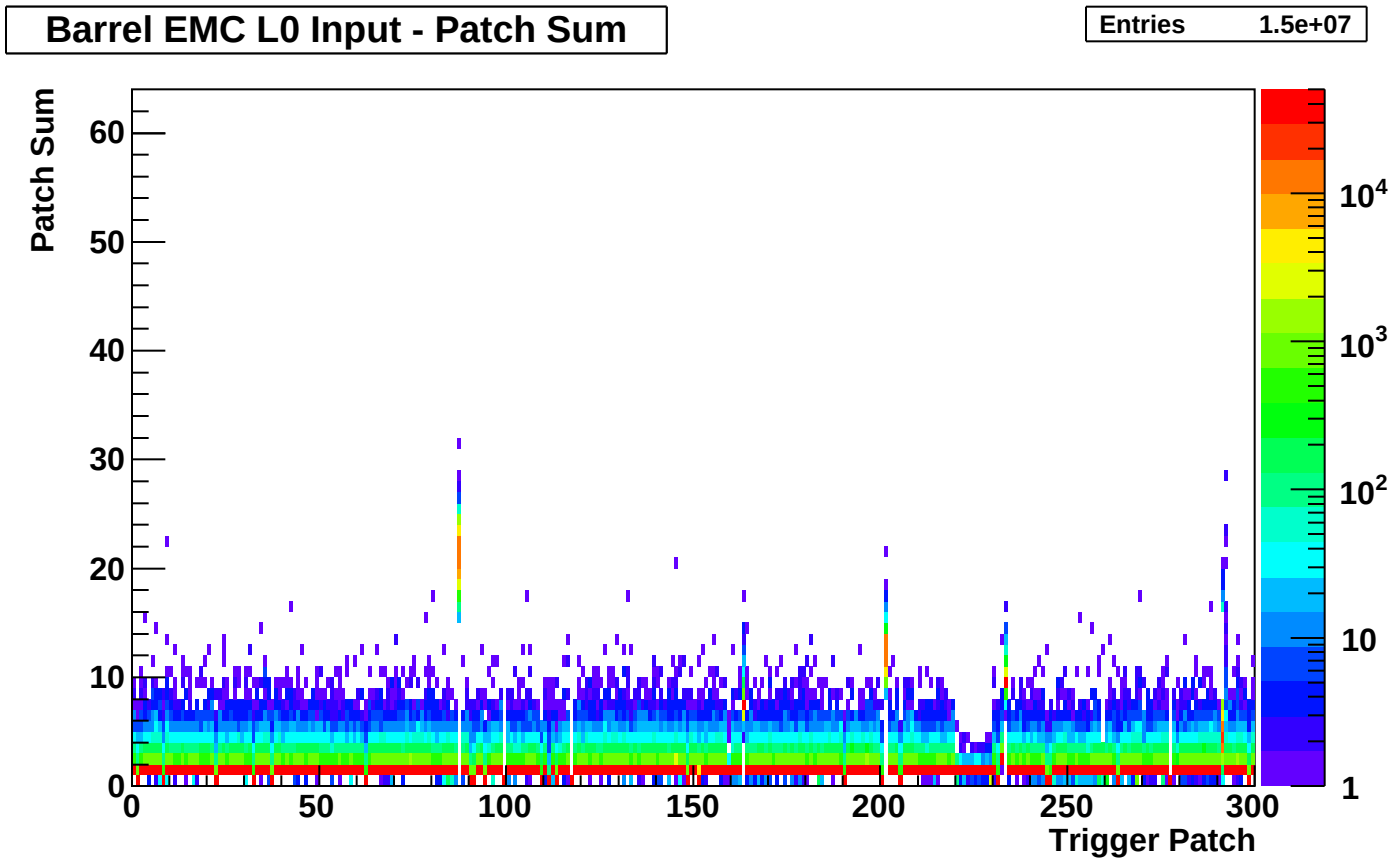

BunchId7Bit (BHT3)
Entries 1

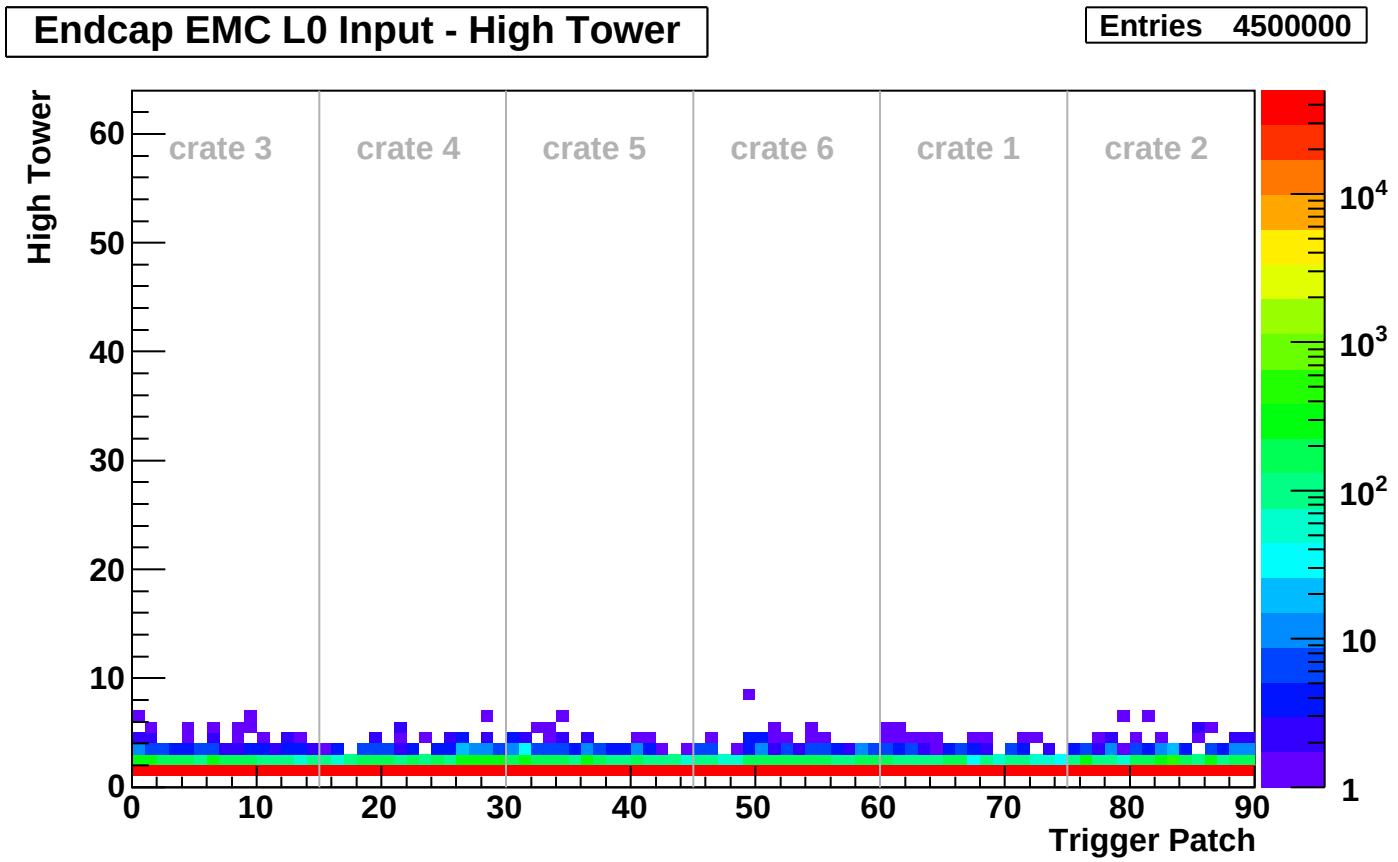

BunchId7Bit (all events)
Entries 50000

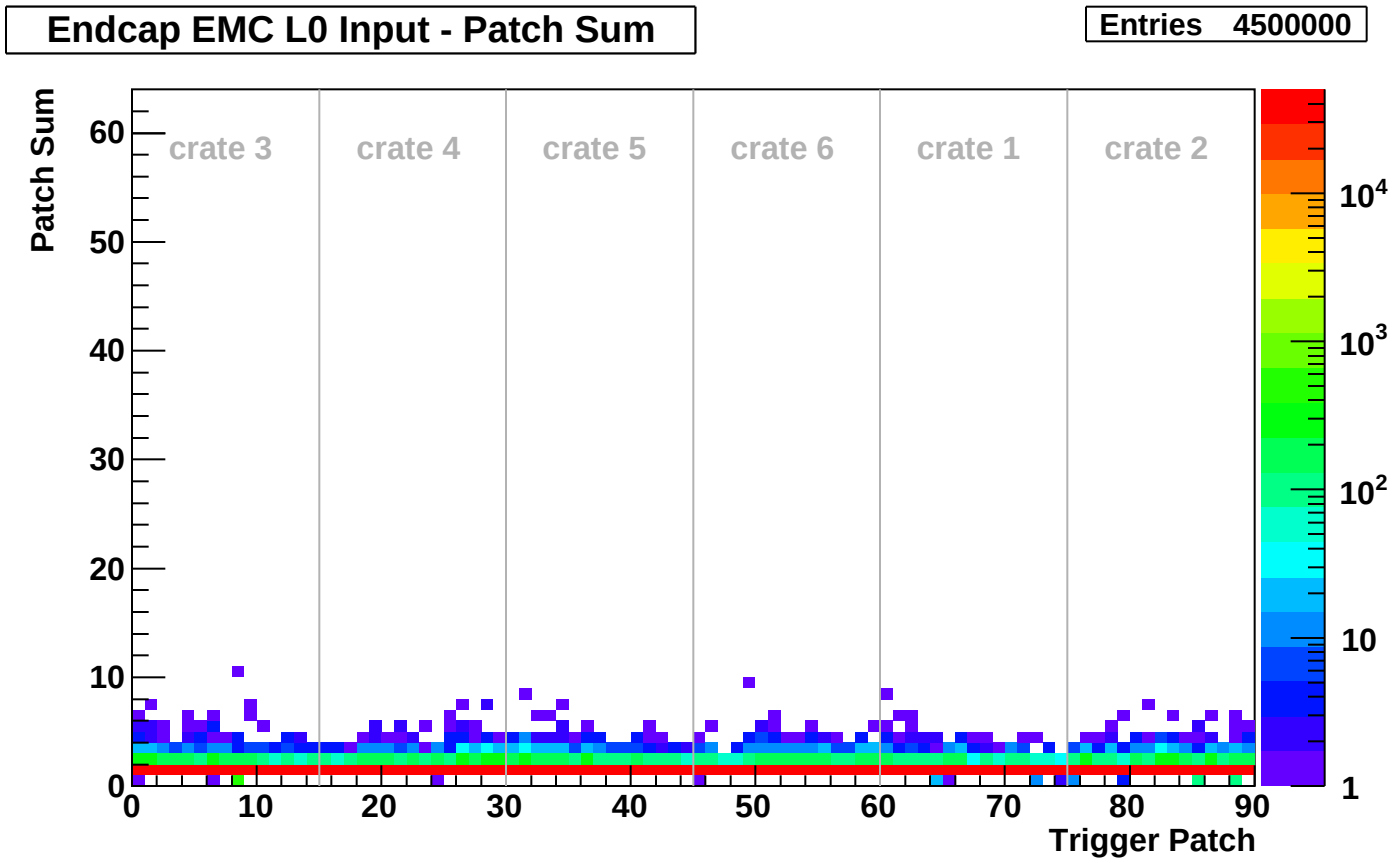

BunchId7Bit (JP1)
Entries 50000

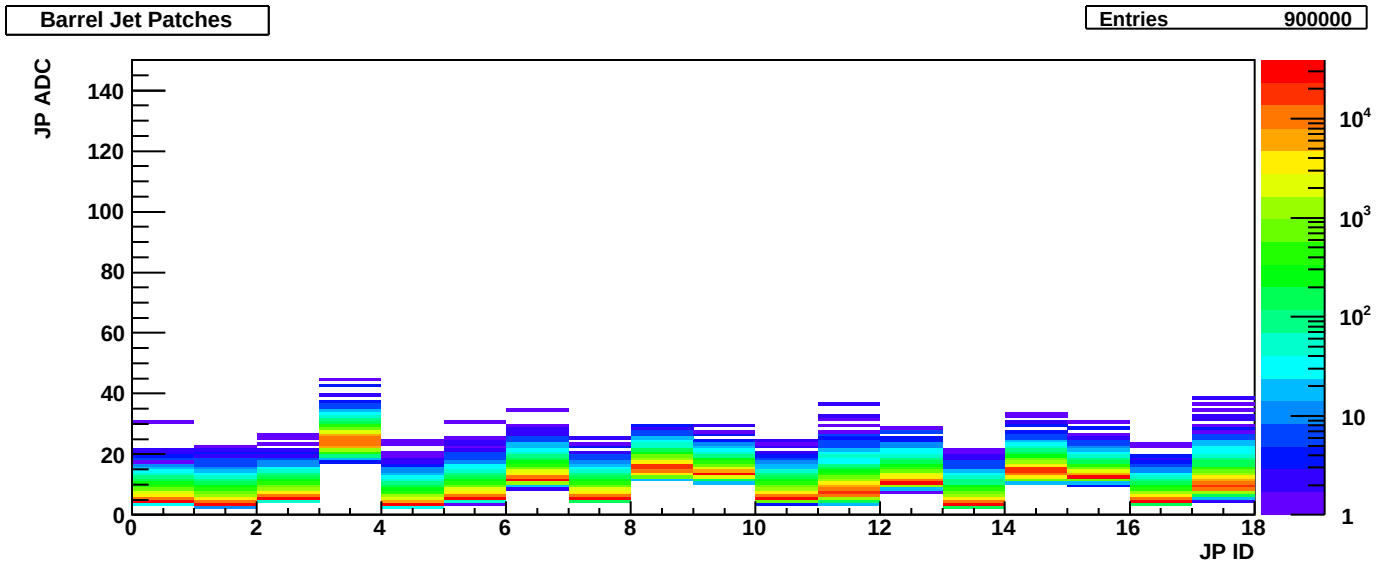

BunchId7Bit (JP2||AJP)
Entries 50000

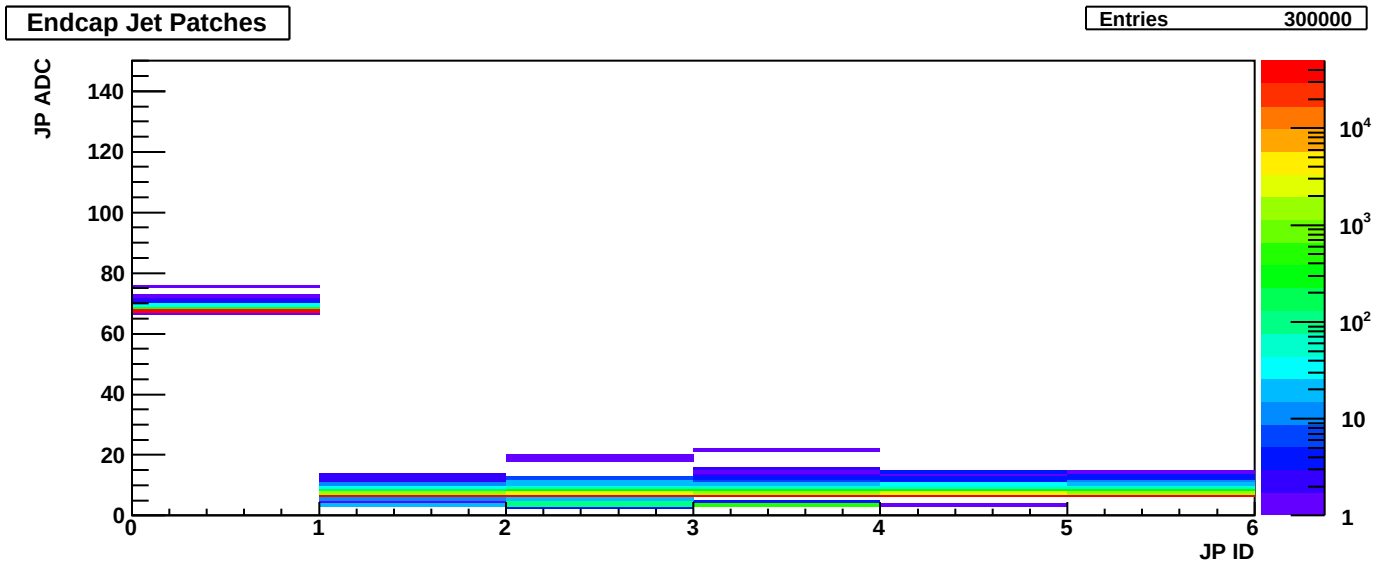

Barrel EMC L0 Input - High Tower
Entries 1.5e+07
High Tower
Trigger Patch
0
10
20
30
40
50
60
0
50
100
150
200
250
300
1
10
$10^2$
$10^3$
$10^4$

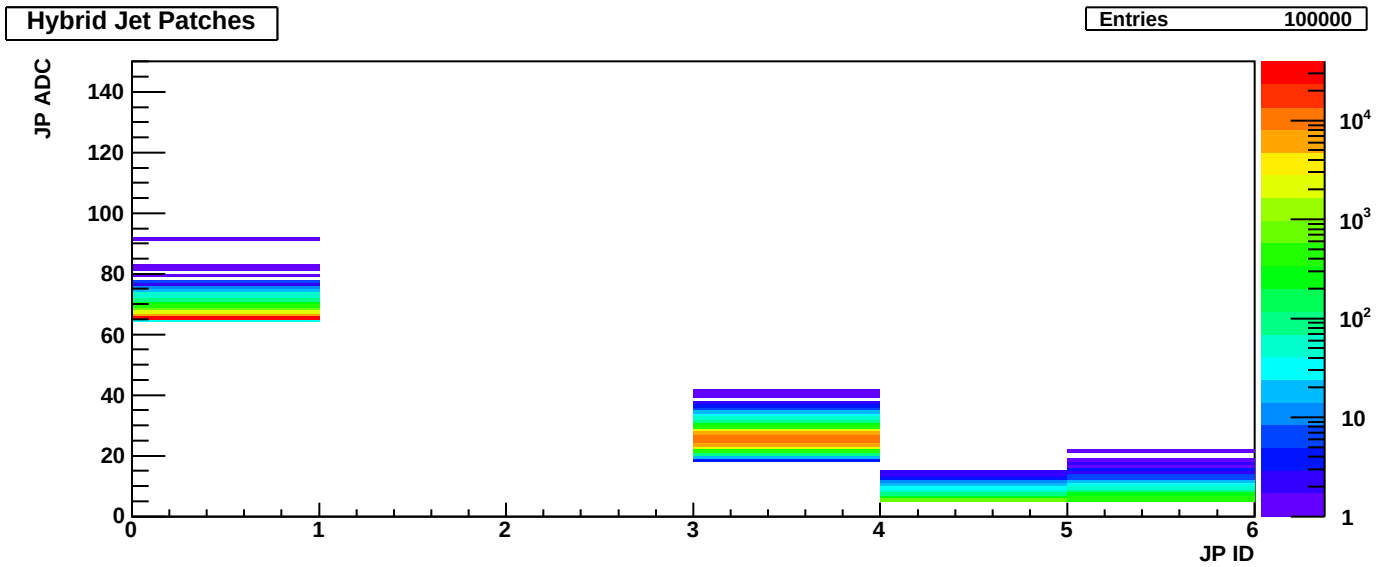

Barrel EMC L0 Input - Patch Sum
Entries 1.5e+07
Patch Sum
Trigger Patch
0
10
20
30
40
50
60
0
50
100
150
200
250
300
1
10
$10^2$
$10^3$
$10^4$

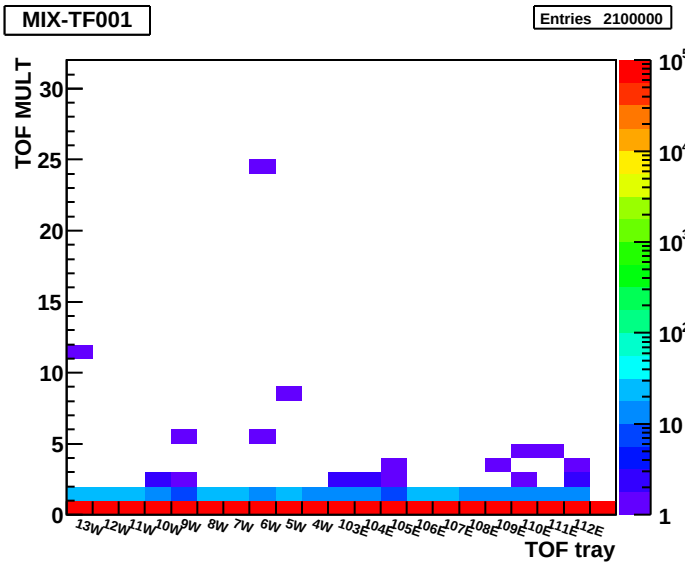

Endcap EMC L0 Input - High Tower
Entries 4500000
High Tower
crate 3
crate 4
crate 5
crate 6
crate 1
crate 2
Trigger Patch

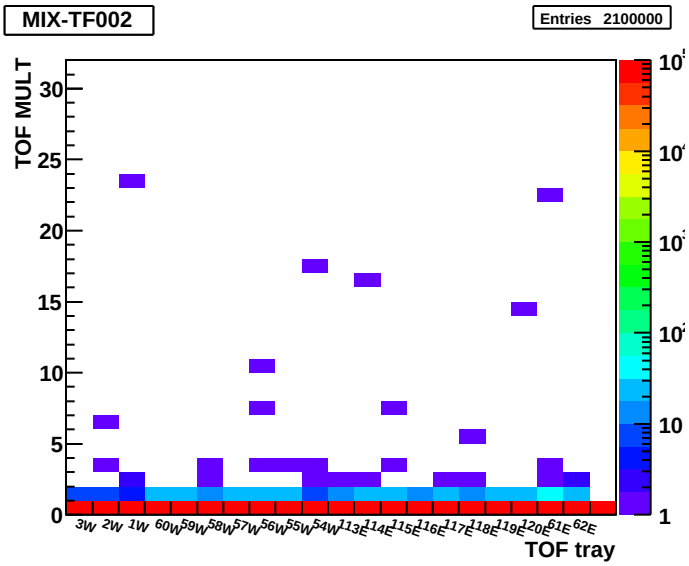

Endcap EMC L0 Input - Patch Sum
Entries 4500000
Patch Sum
crate 3
crate 4
crate 5
crate 6
crate 1
crate 2
Trigger Patch

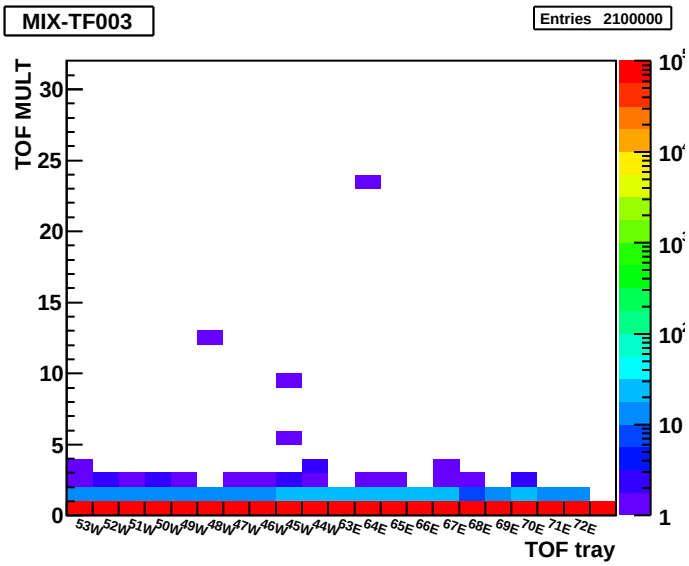

Barrel Jet Patches
Entries 900000
JP ADC
JP ID

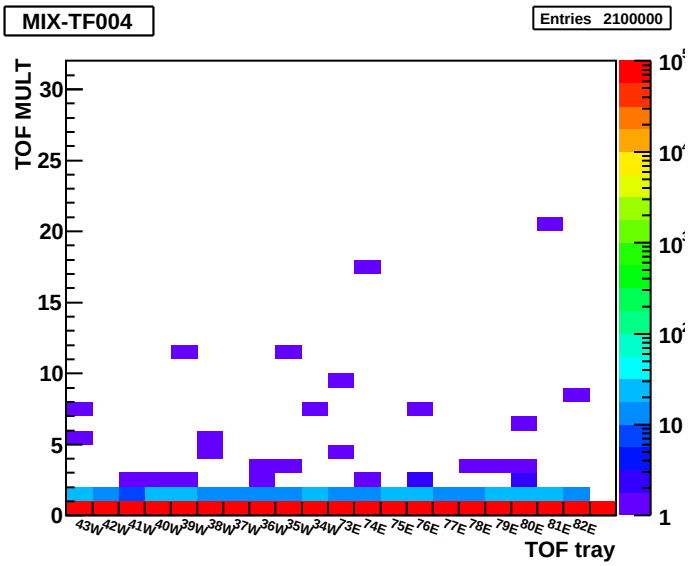

Endcap Jet Patches
Entries 300000
JP ADC
JP ID

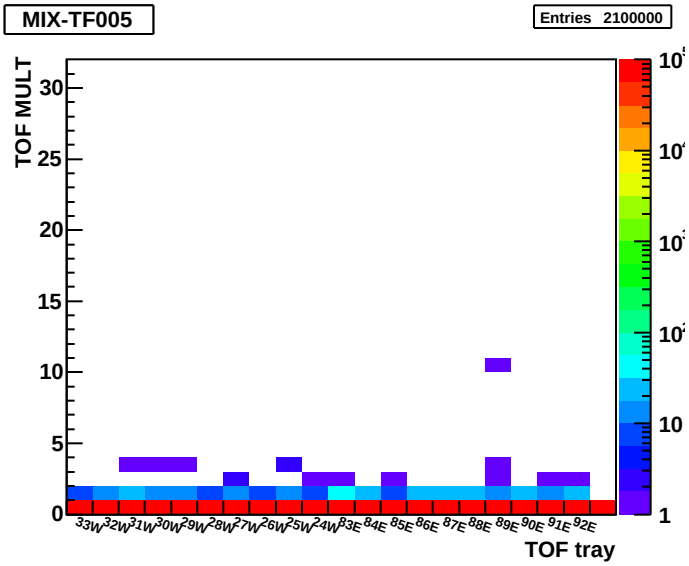

Hybrid Jet Patches
Entries 100000
JP ADC
JP ID

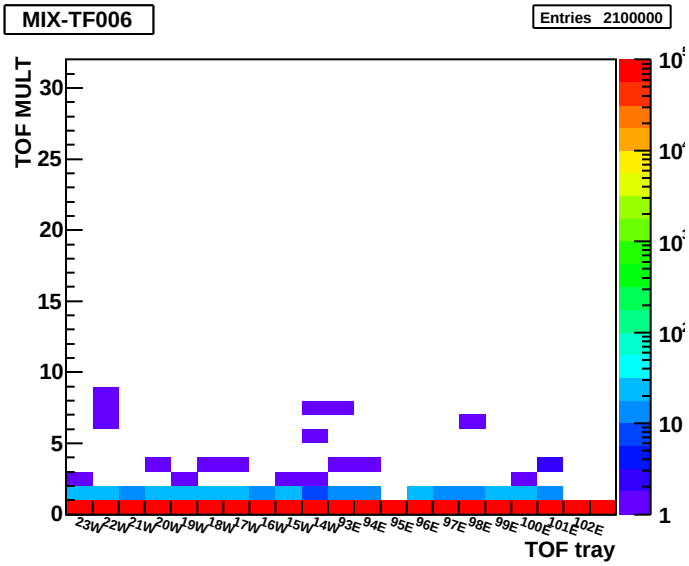

MIX-TF001
Entries 2100000
TOF MULT
TOF tray

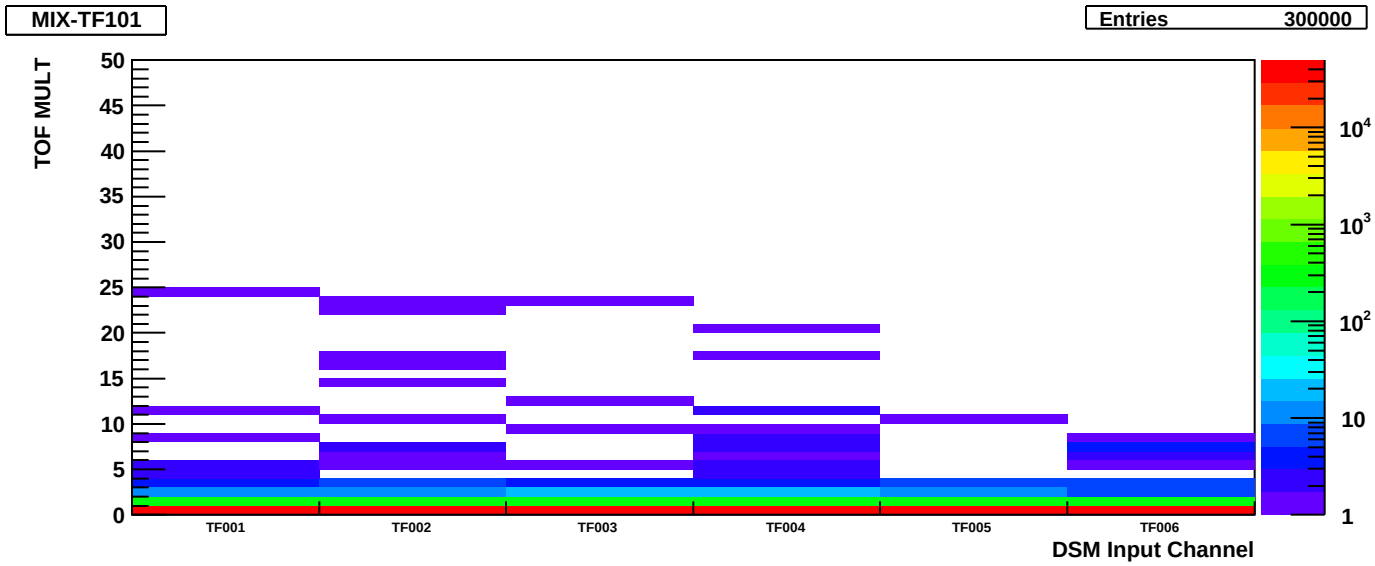

MIX-TF002
Entries 2100000
TOF MULT
TOF tray

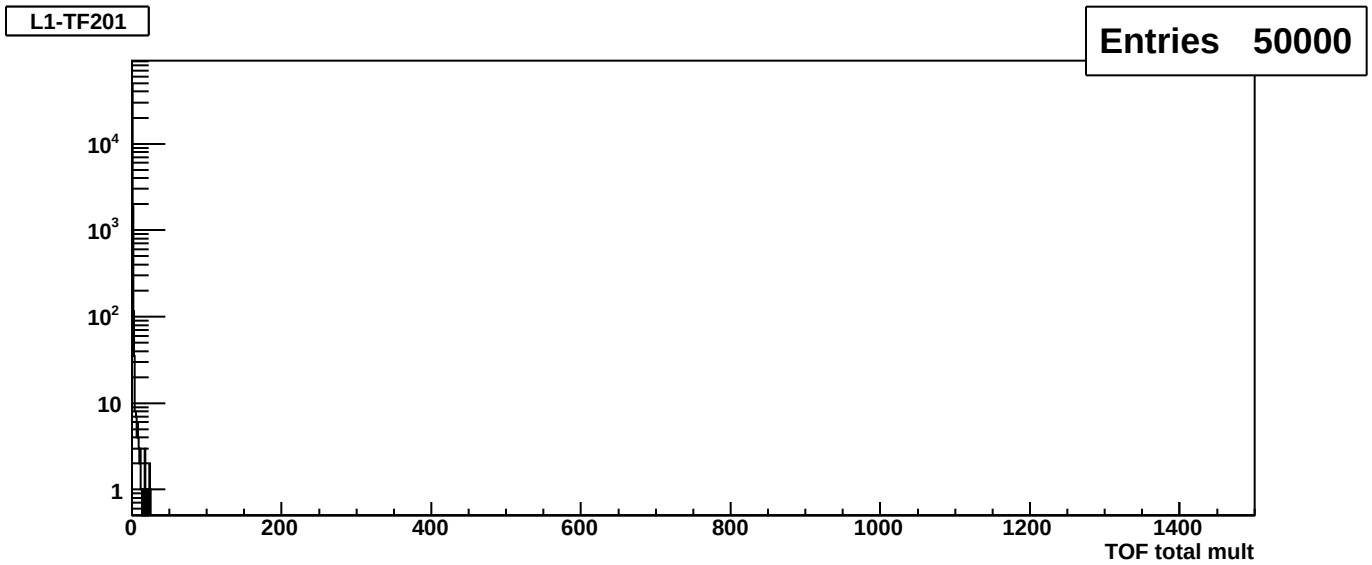

MIX-TF003
Entries 2100000
TOF MULT
TOF tray

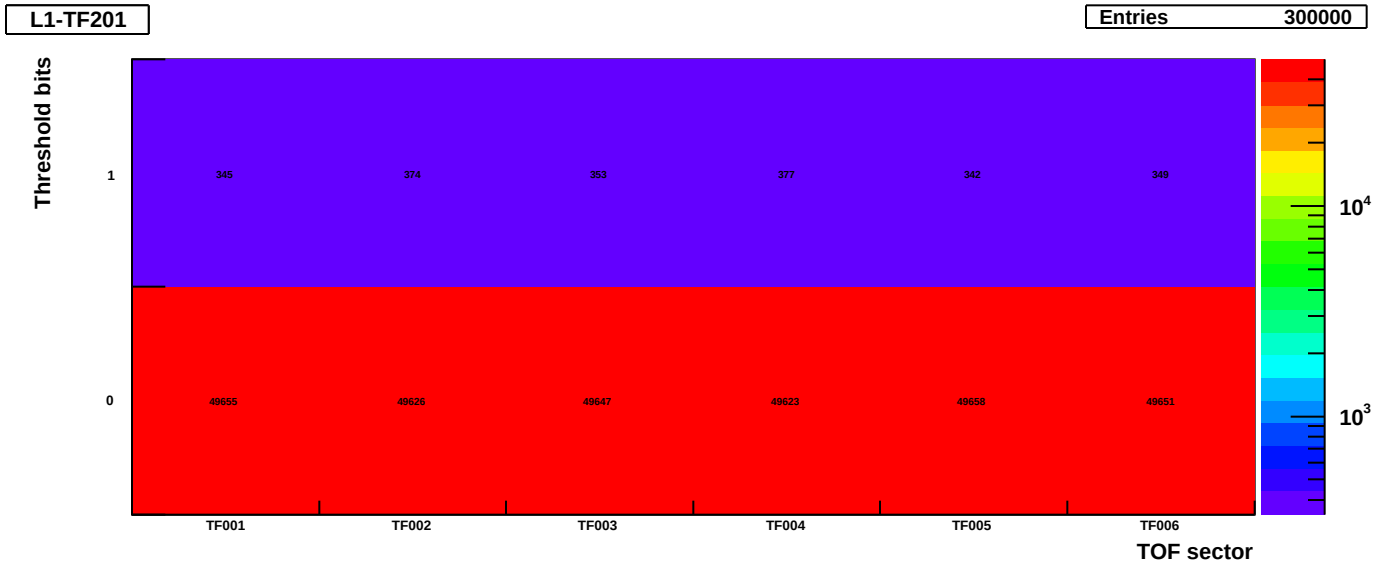

MIX-TF004
Entries 2100000
TOF MULT
TOF tray

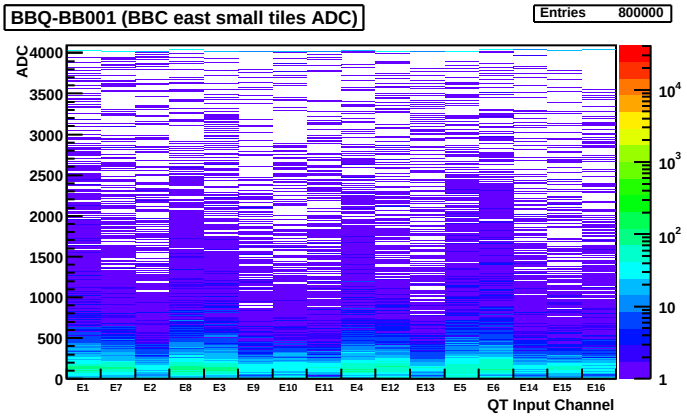

MIX-TF005
Entries 2100000
TOF MULT
TOF tray

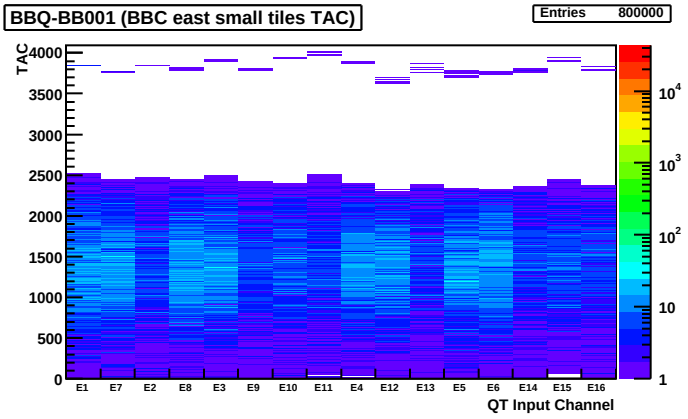

MIX-TF006
Entries 2100000
TOF MULT
TOF tray

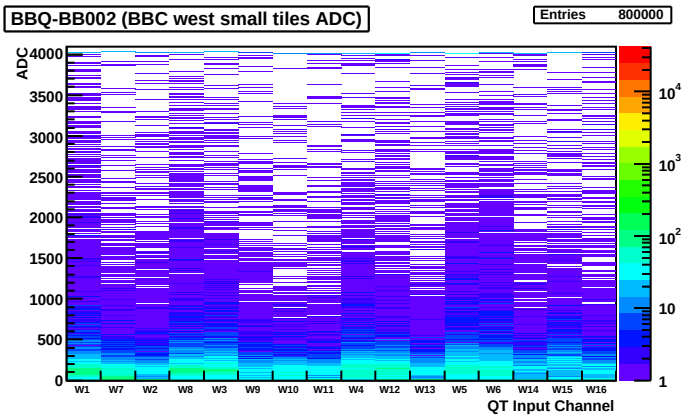

MIX-TF101
Entries 300000
TOF MULT
50
45
40
35
30
25
20
15
10
5
0
TF001
TF002
TF003
TF004
TF005
TF006
DSM Input Channel
$10^4$
$10^3$
$10^2$
10
1

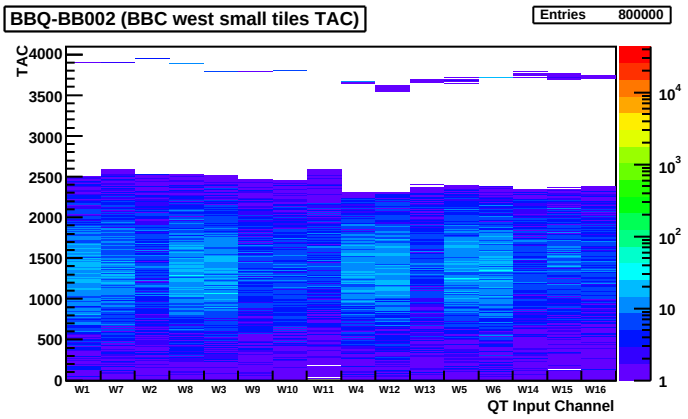

L1-TF201
Entries 50000
$10^4$
$10^3$
$10^2$
10
1
0
200
400
600
800
1000
1200
1400
TOF total mult

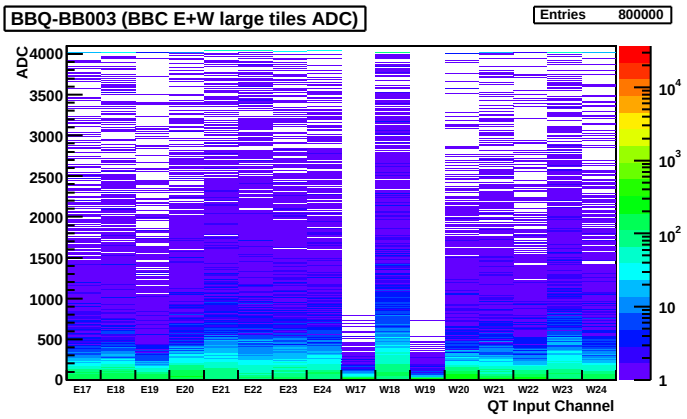

L1-TF201
Entries 300000
Threshold bits
1
0
345
374
353
377
342
349
49655
49626
49647
49623
49658
49651
TF001
TF002
TF003
TF004
TF005
TF006
TOF sector
$10^4$
$10^3$

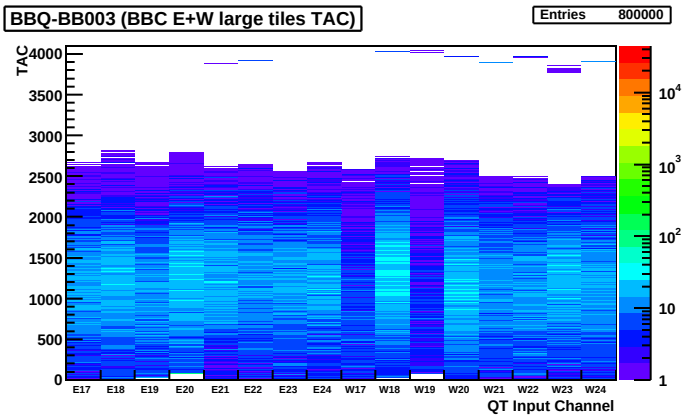

BBQ-BB001 (BBC east small tiles ADC)
Entries 800000
ADC
QT Input Channel

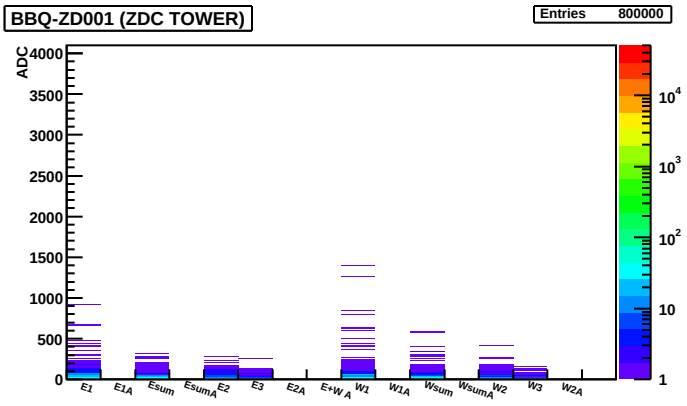

BBQ-BB001 (BBC east small tiles TAC)
Entries 800000
TAC
QT Input Channel

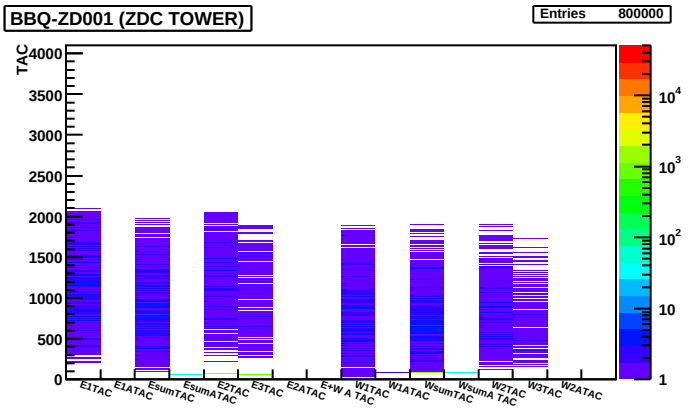

BBQ-BB002 (BBC west small tiles ADC)
Entries 800000
ADC
QT Input Channel

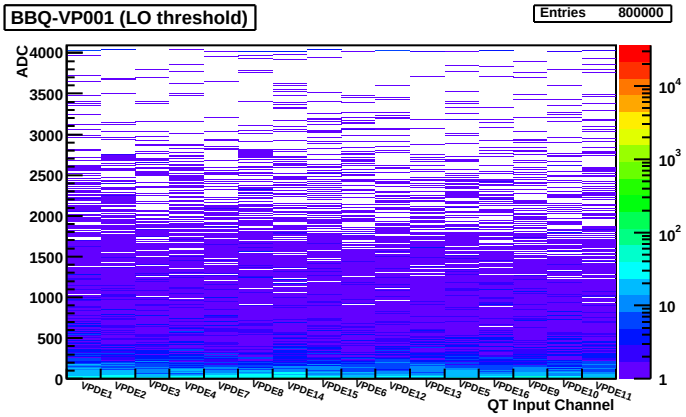

BBQ-BB002 (BBC west small tiles TAC)
Entries 800000
TAC
QT Input Channel

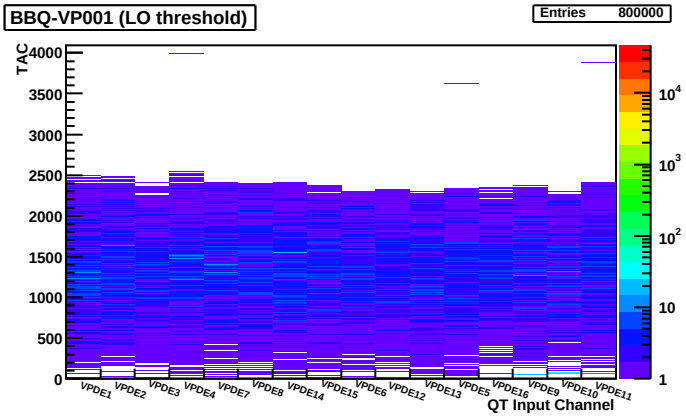

BBQ-BB003 (BBC E+W large tiles ADC)
Entries 800000
ADC
QT Input Channel

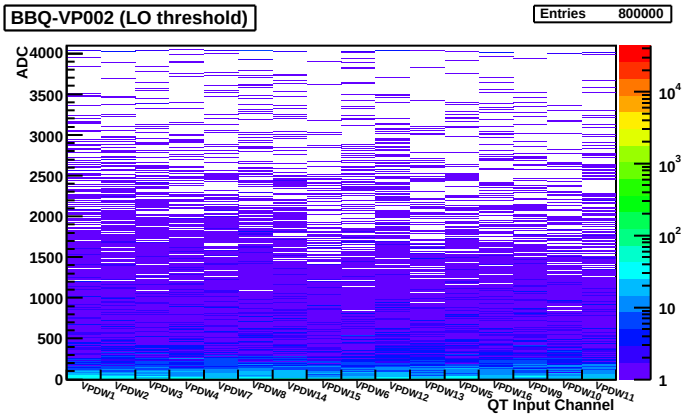

BBQ-BB003 (BBC E+W large tiles TAC)
Entries 800000
TAC
QT Input Channel

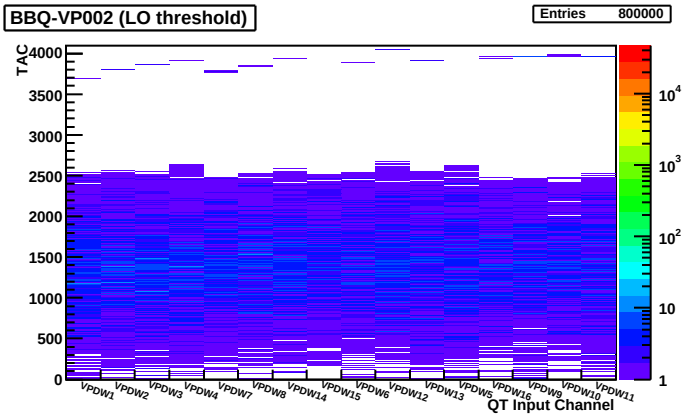

BBQ-ZD001 (ZDC TOWER)
Entries 800000
ADC

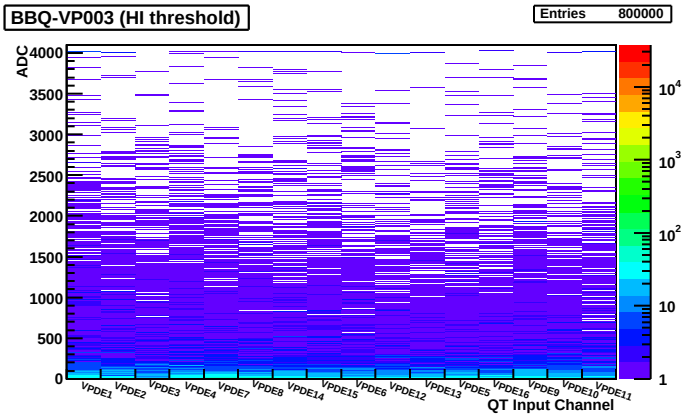

BBQ-ZD001 (ZDC TOWER)
Entries 800000
TAC

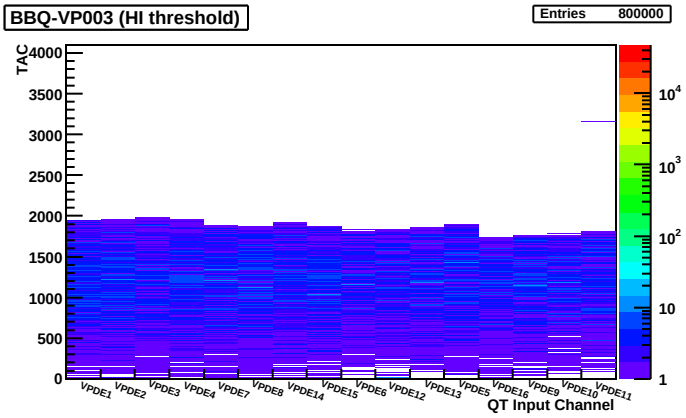

BBQ-VP001 (LO threshold)
Entries 800000
ADC
QT Input Channel

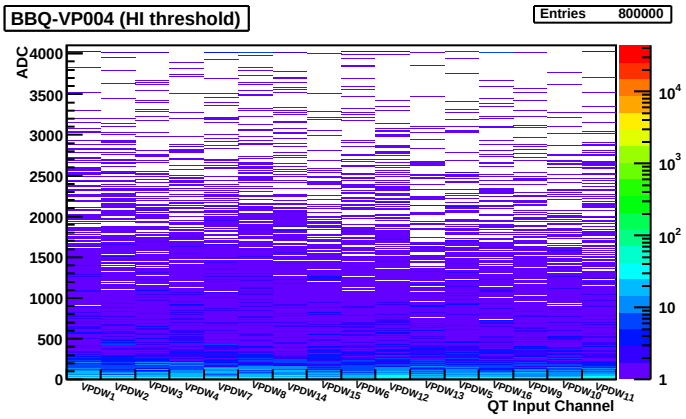

BBQ-VP001 (LO threshold)
Entries 800000
TAC
QT Input Channel

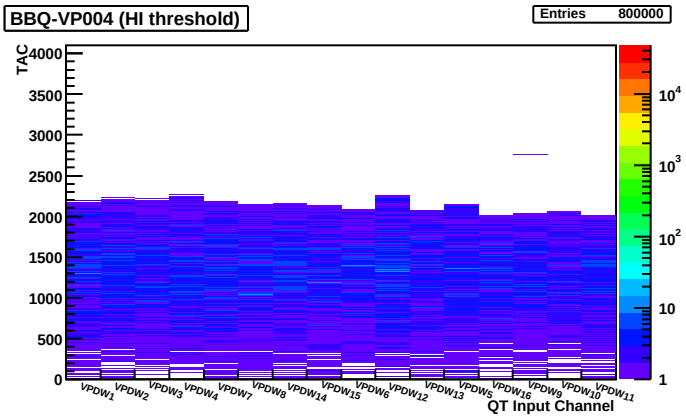

BBQ-VP002 (LO threshold)
Entries 800000
ADC
QT Input Channel

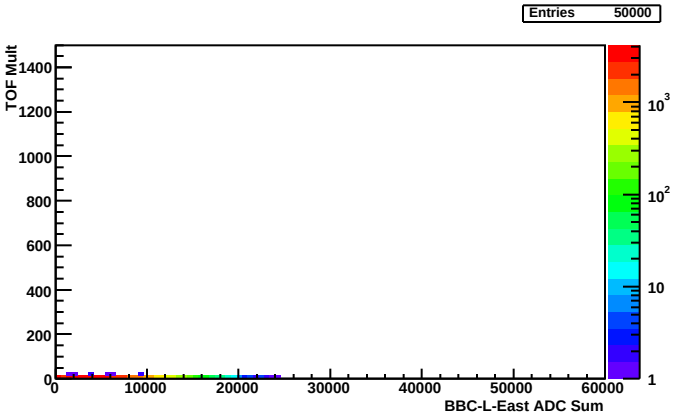

BBQ-VP002 (LO threshold)
Entries 800000
TAC
QT Input Channel

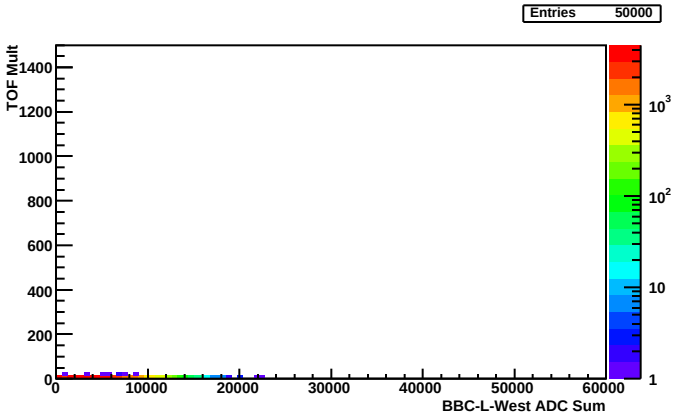

BBQ-VP003 (HI threshold)
Entries 800000
ADC
QT Input Channel

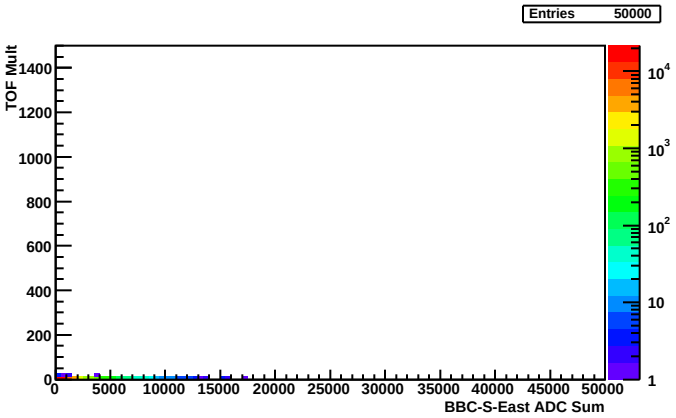

BBQ-VP003 (HI threshold)
Entries 800000
TAC
QT Input Channel

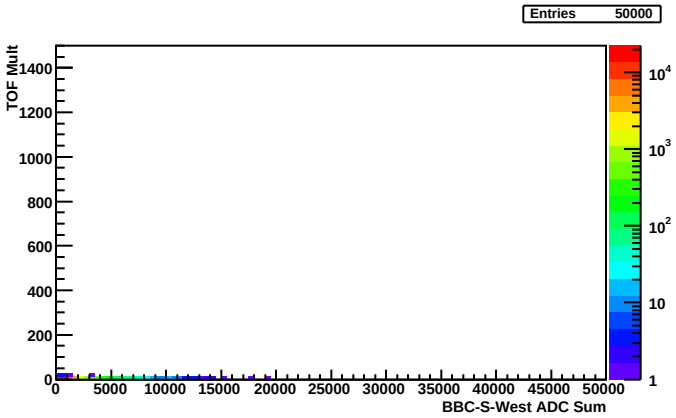

BBQ-VP004 (HI threshold)
Entries 800000
ADC
QT Input Channel

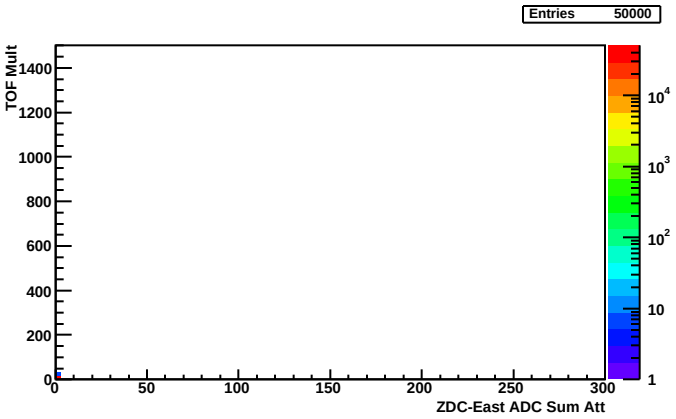

BBQ-VP004 (HI threshold)
Entries 800000
TAC
QT Input Channel

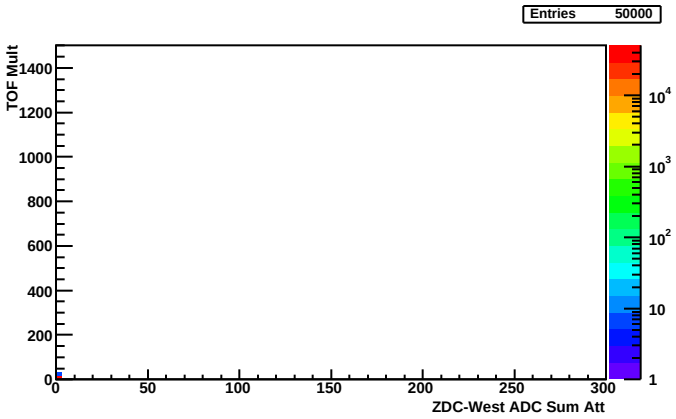

Entries 50000
TOF Mult
BBC-L-East ADC Sum

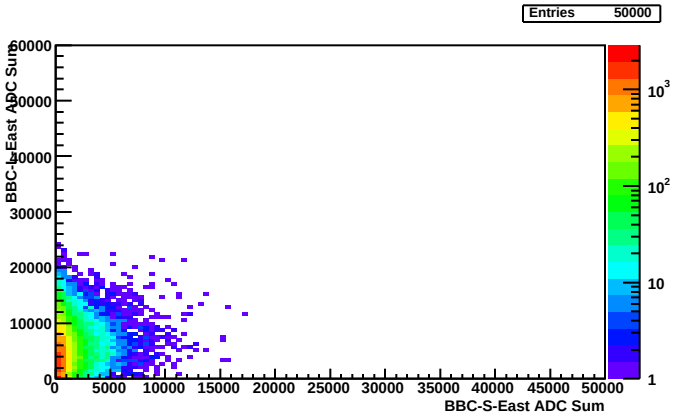

Entries 50000
TOF Mult
BBC-L-West ADC Sum

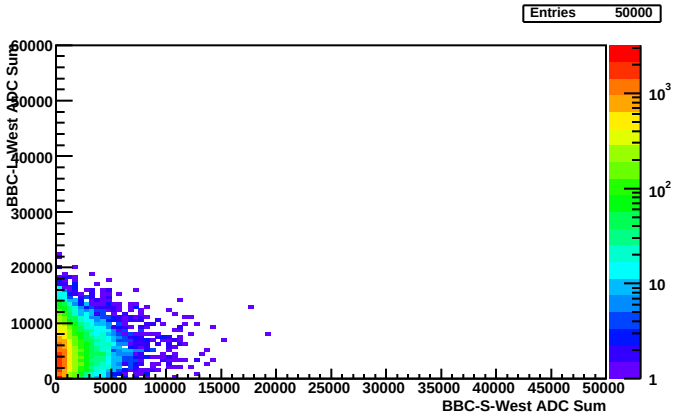

Entries 50000
TOF Mult
BBC-S-East ADC Sum

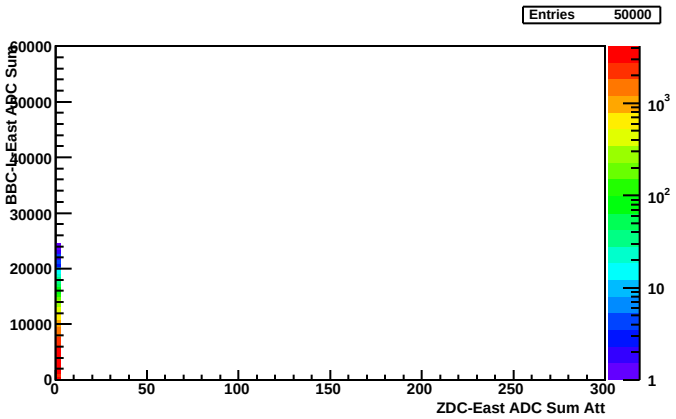

Entries 50000
TOF Mult
BBC-S-West ADC Sum

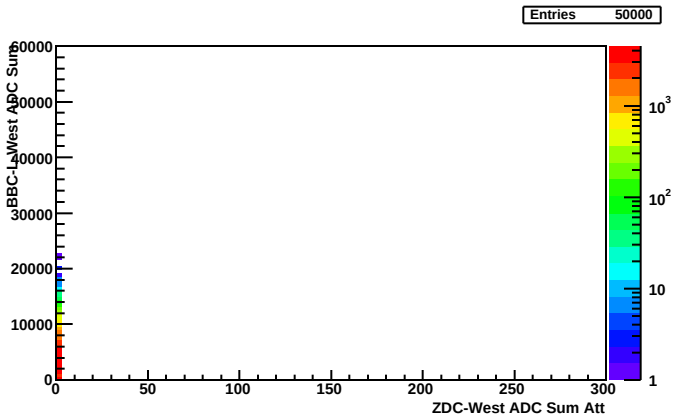

Entries 50000
TOF Mult
ZDC-East ADC Sum Att

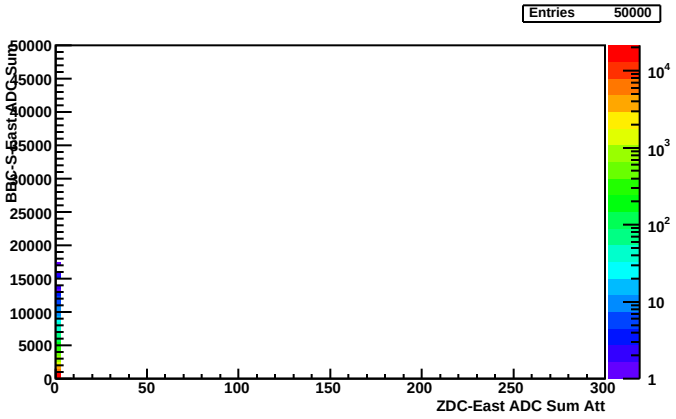

Entries 50000
TOF Mult
ZDC-West ADC Sum Att

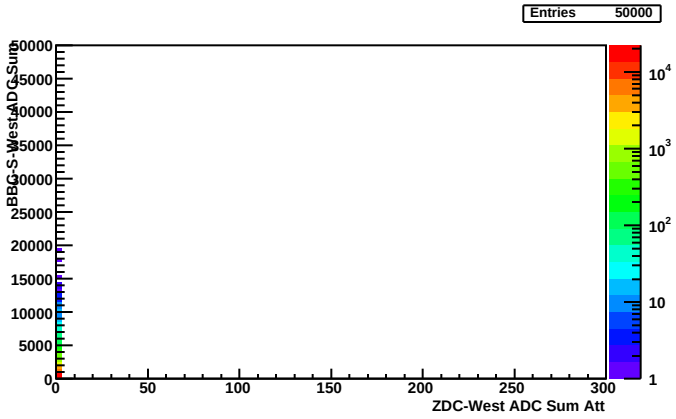

Entries 50000
BBC-L-East ADC Sum
BBC-S-East ADC Sum

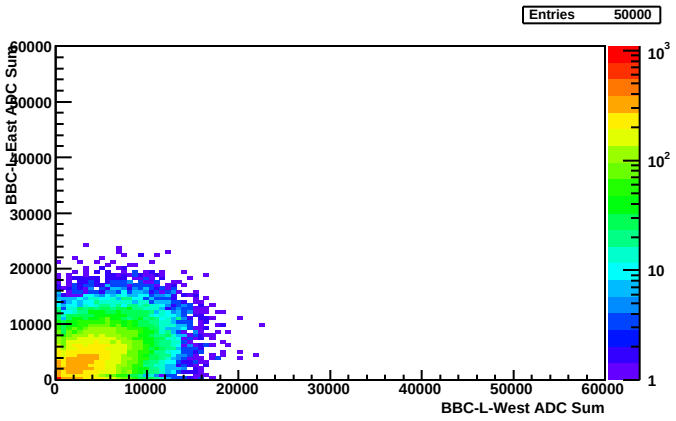

Entries 50000
BBC-L-West ADC Sum
BBC-S-West ADC Sum

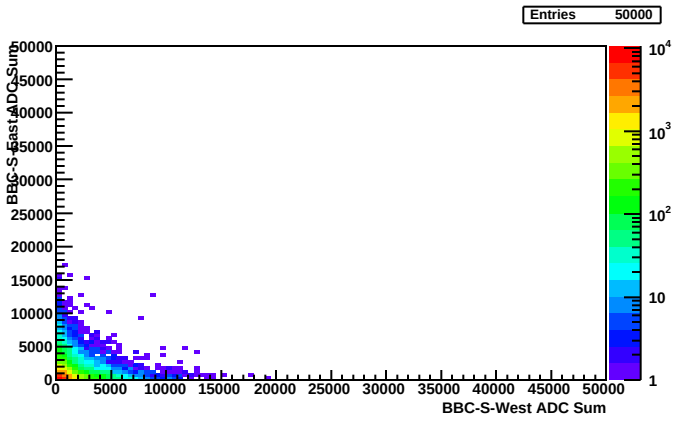

Entries 50000
BBC-L-East ADC Sum
ZDC-East ADC Sum Att

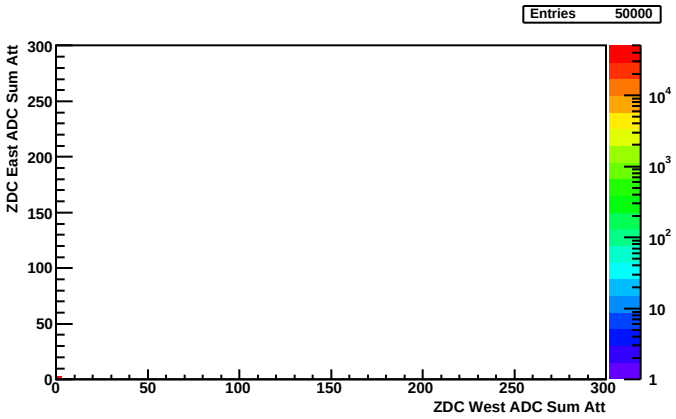

Entries 50000
BBC-L-West ADC Sum
ZDC-West ADC Sum Att

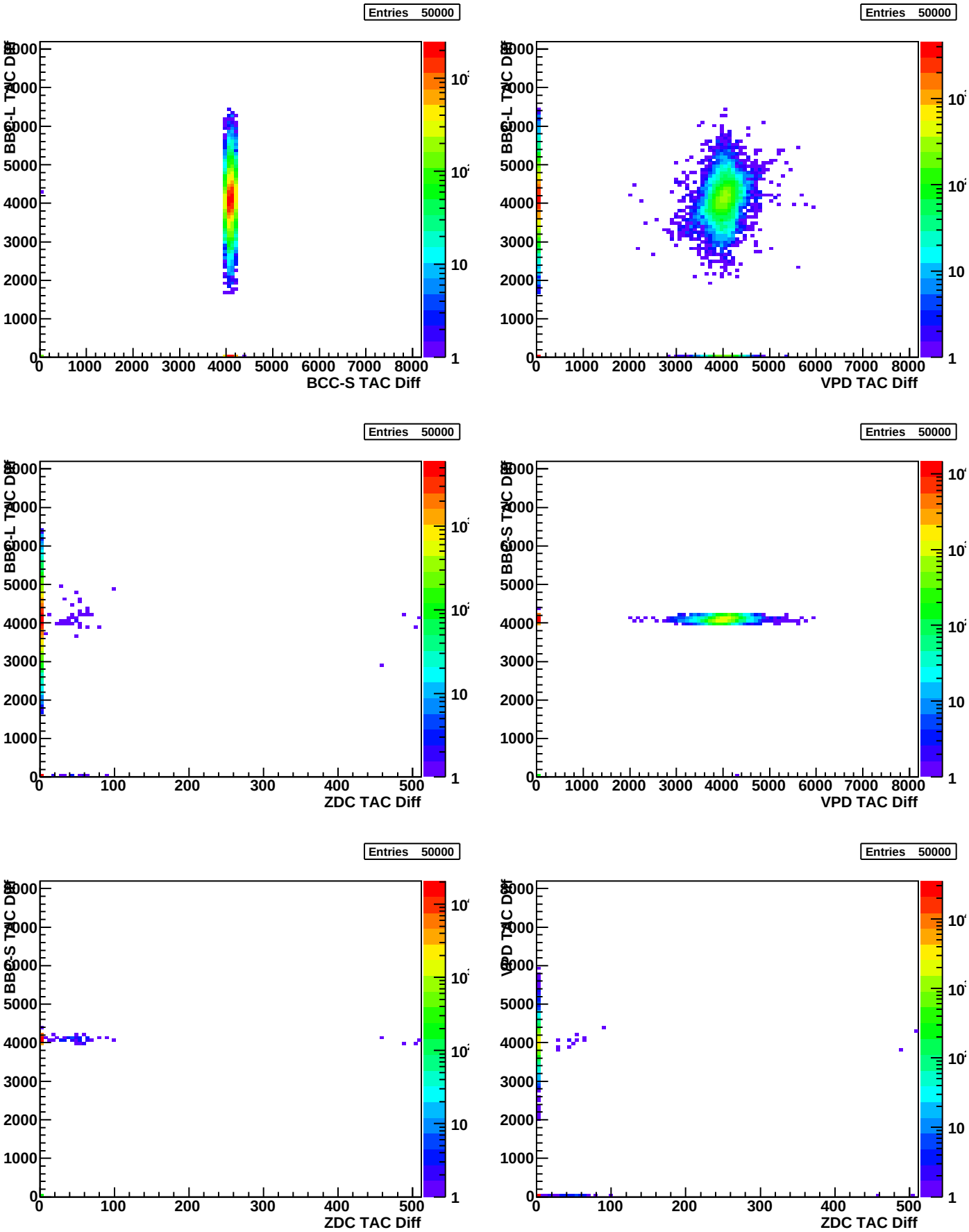

Entries 50000
BBC-S-East ADC Sum
ZDC-East ADC Sum Att

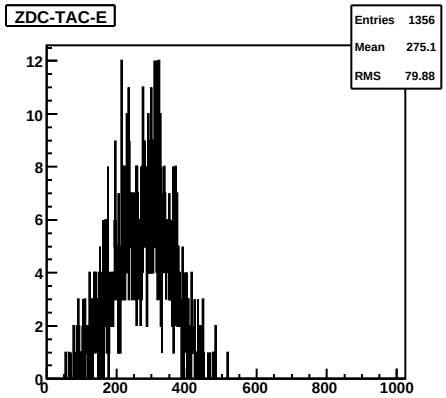

Entries 50000
BBC-S-West ADC Sum
ZDC-West ADC Sum Att

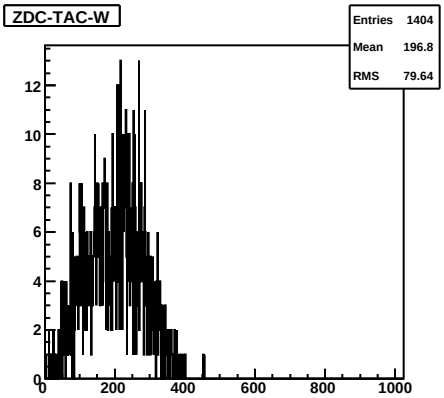

Entries 50000
BBC-L-East ADC Sum
BBC-L-West ADC Sum

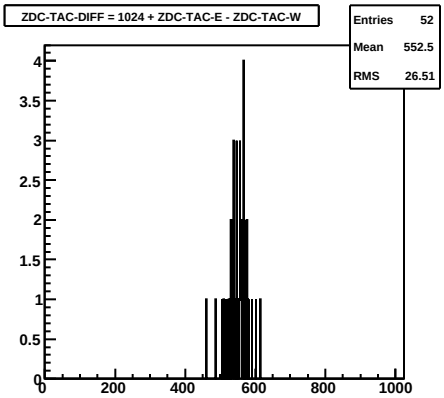

Entries 50000
BBC-S-East ADC Sum
BBC-S-West ADC Sum

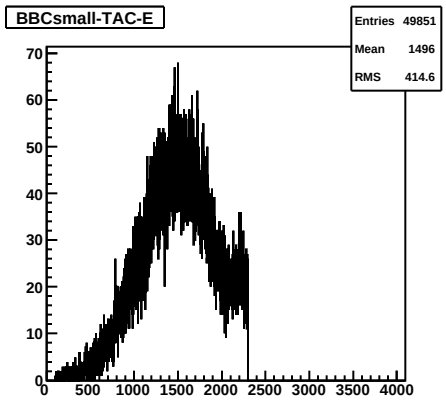

Entries 50000
ZDC East ADC Sum Att
ZDC West ADC Sum Att

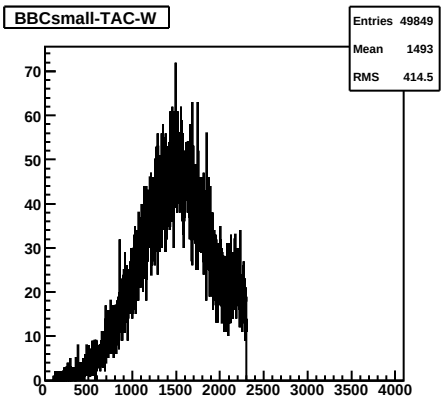

Entries 50000
BBC-L TAC Diff
BCC-S TAC Diff
Entries 50000
BBC-L TAC Diff
VPD TAC Diff
Entries 50000
BBC-L TAC Diff
ZDC TAC Diff
Entries 50000
BBC-S TAC Diff
VPD TAC Diff
Entries 50000
BBC-S TAC Diff
ZDC TAC Diff
Entries 50000
VPD TAC Diff
ZDC TAC Diff

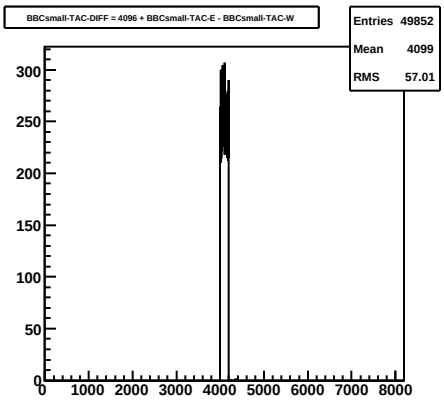

ZDC-TAC-E
Entries 1356
Mean 275.1
RMS 79.88

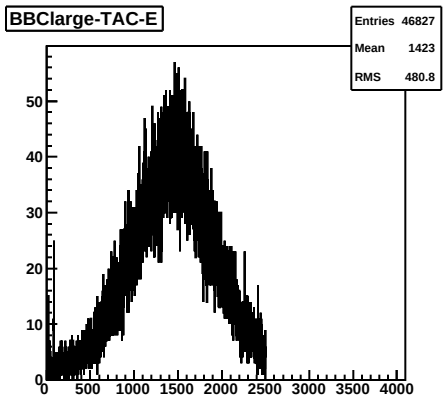

ZDC-TAC-W
Entries 1404
Mean 196.8
RMS 79.64

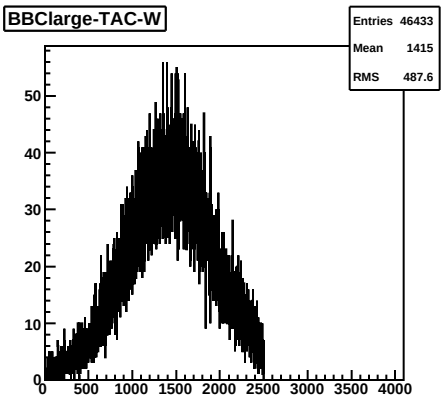

ZDC-TAC-DIFF = 1024 + ZDC-TAC-E - ZDC-TAC-W
Entries 52
Mean 552.5
RMS 26.51

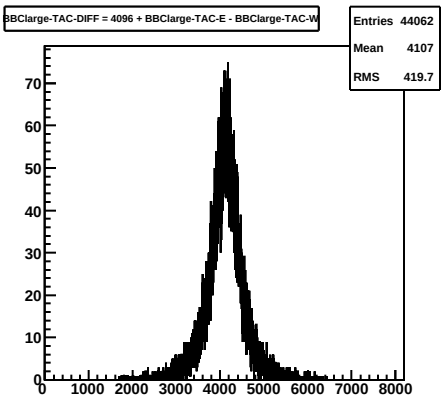

BBCsmall-TAC-E
Entries 49851
Mean 1496
RMS 414.6

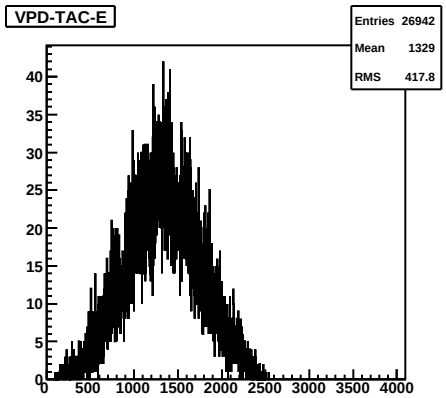

BBCsmall-TAC-W
Entries 49849
Mean 1493
RMS 414.5

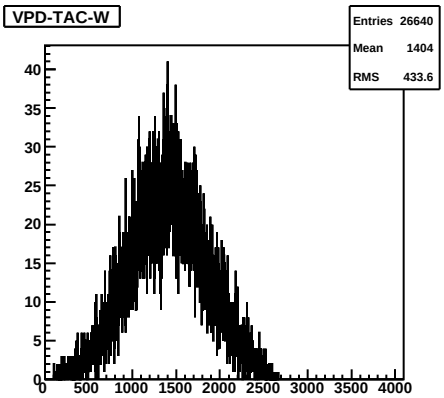

BBCsmall-TAC-DIFF = 4096 + BBCsmall-TAC-E - BBCsmall-TAC-W
Entries 49852
Mean 4099
RMS 57.01

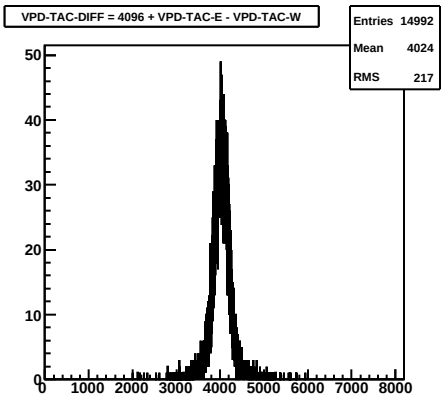

BBClarge-TAC-E
Entries 46827
Mean 1423
RMS 480.8

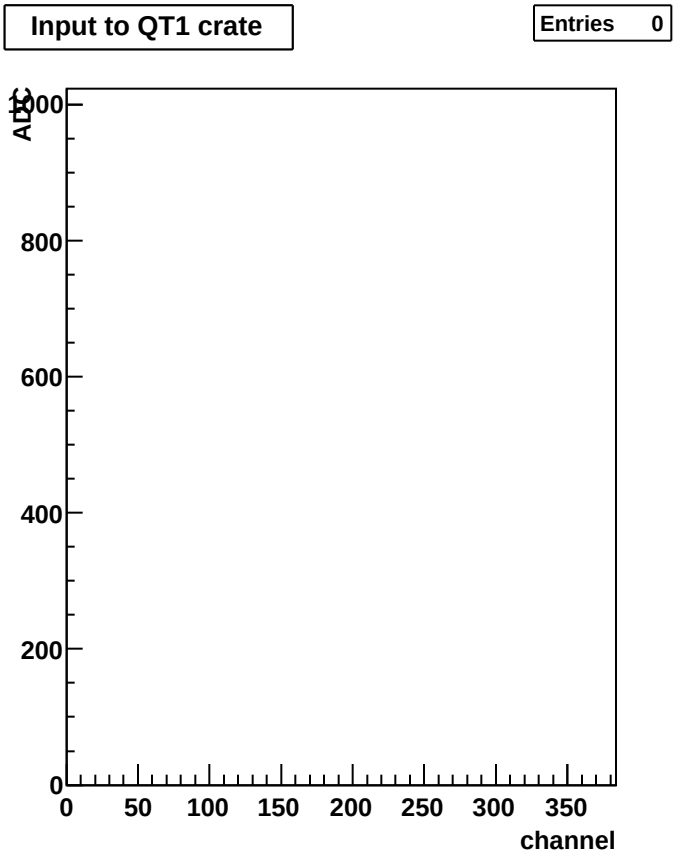

BBClarge-TAC-W
Entries 46433
Mean 1415
RMS 487.6

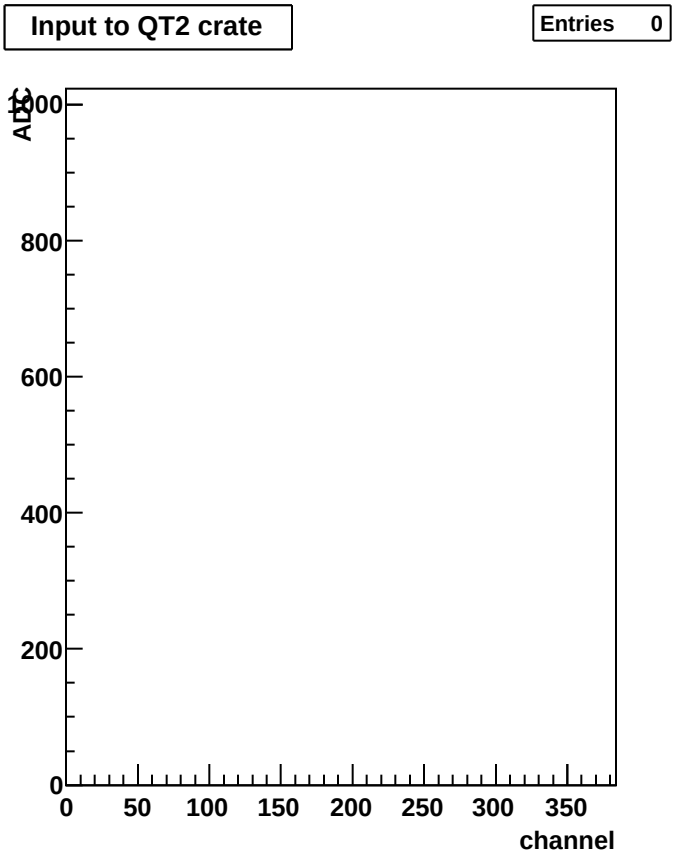

BBClarge-TAC-DIFF = 4096 + BBClarge-TAC-E - BBClarge-TAC-W
Entries 44062
Mean 4107
RMS 419.7

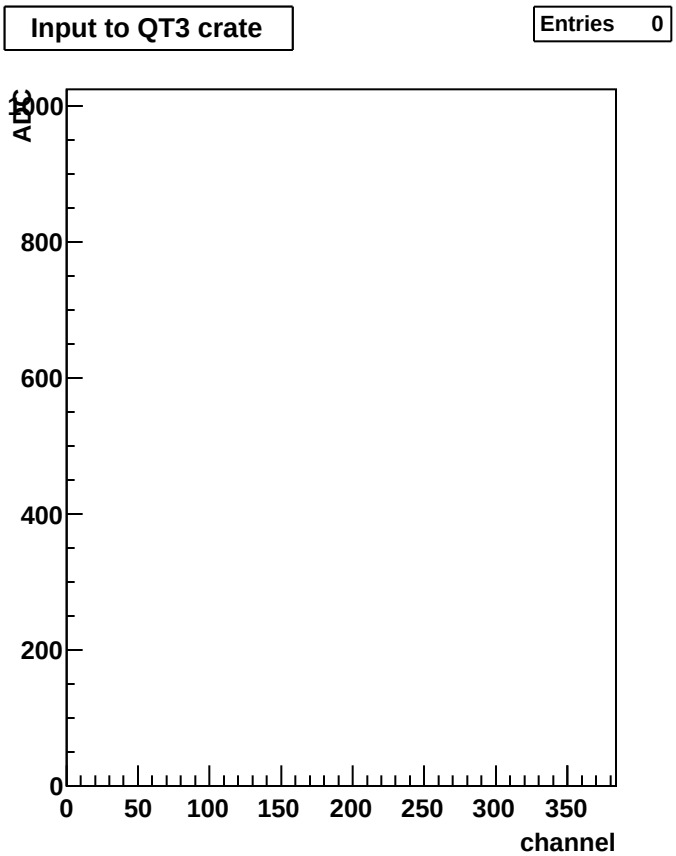

VPD-TAC-E
Entries 26942
Mean 1329
RMS 417.8

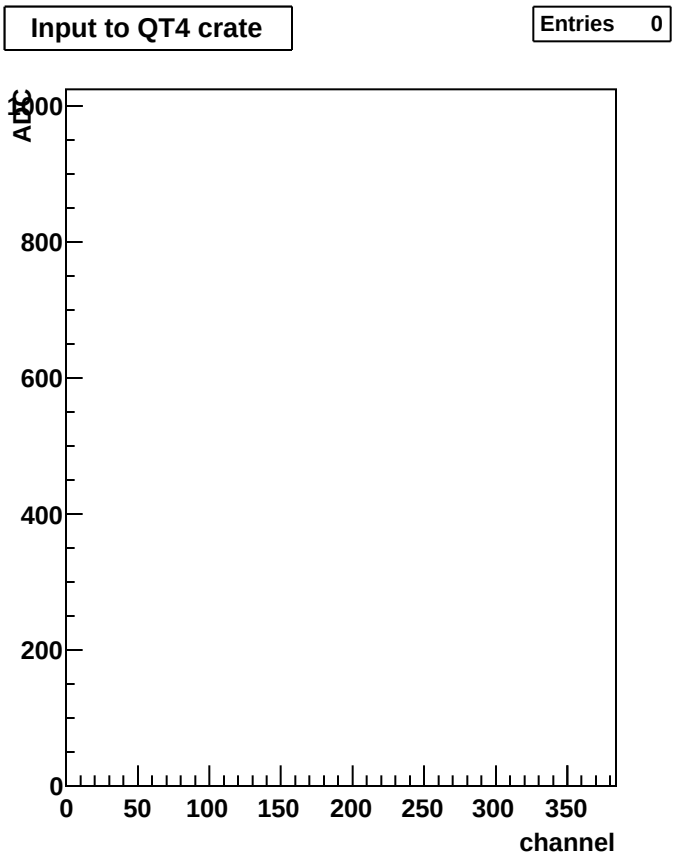

VPD-TAC-W
Entries 26640
Mean 1404
RMS 433.6

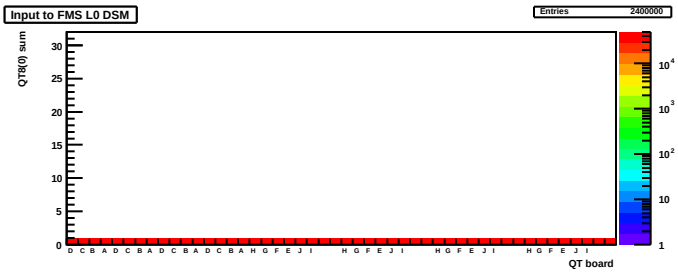

VPD-TAC-DIFF = 4096 + VPD-TAC-E - VPD-TAC-W
Entries 14992
Mean 4024
RMS 217

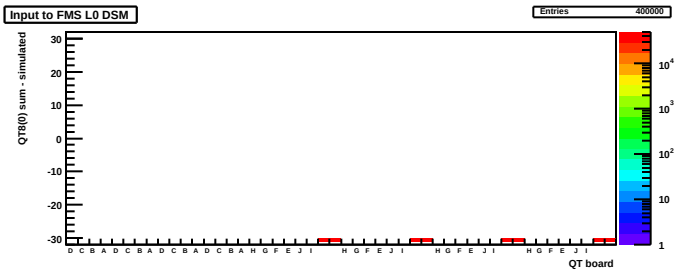

Input to QT1 crate
Entries 0
ADC
1000
800
600
400
200
0
0 50 100 150 200 250 300 350
channel

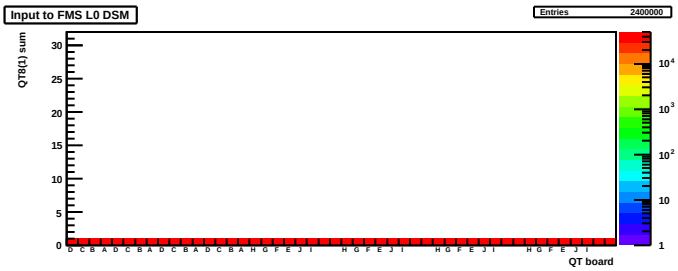

Input to QT2 crate
Entries 0
ADC
1000
800
600
400
200
0
0 50 100 150 200 250 300 350
channel

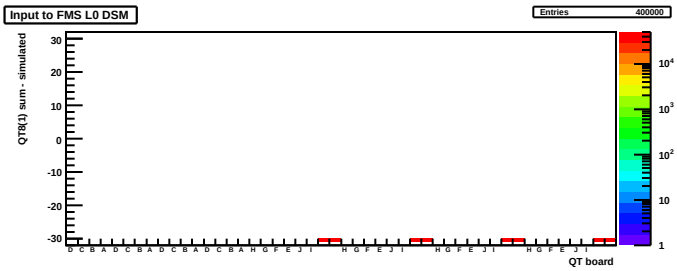

Input to QT3 crate
Entries 0
ADC
1000
800
600
400
200
0
0 50 100 150 200 250 300 350
channel

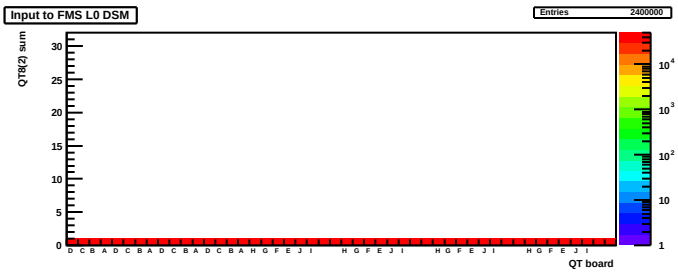

Input to QT4 crate
Entries 0
ADC
1000
800
600
400
200
0
0 50 100 150 200 250 300 350
channel

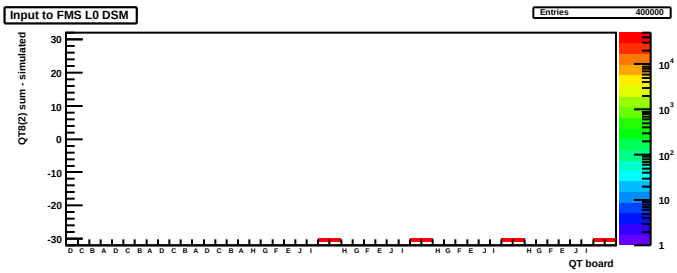

Input to FMS L0 DSM
Entries 2400000
QT8(0) sum
QT board

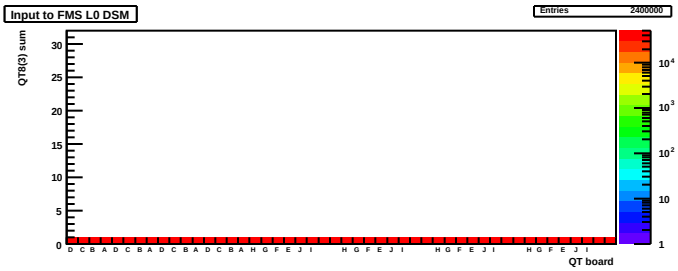

Input to FMS L0 DSM
Entries 400000
QT8(0) sum - simulated
QT board

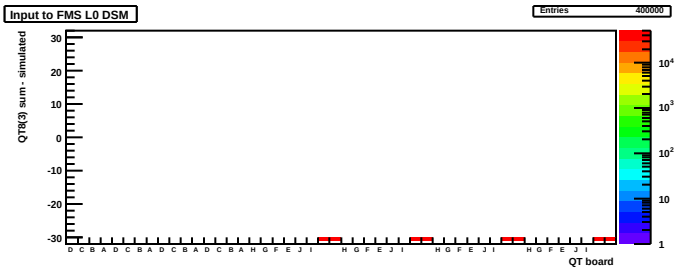

Input to FMS L0 DSM
Entries 2400000
QT8(1) sum
QT board

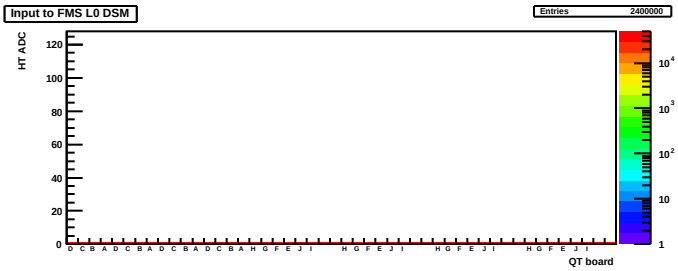

Input to FMS L0 DSM
Entries 400000
QT8(1) sum - simulated
QT board

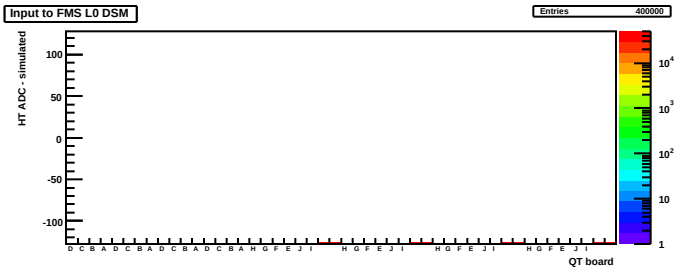

Input to FMS L0 DSM
Entries 2400000
QT8(2) sum
QT board

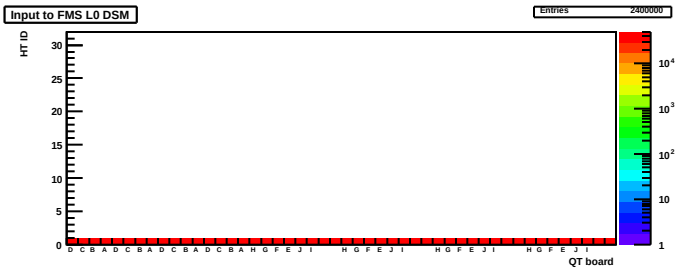

Input to FMS L0 DSM
Entries 400000
QT8(2) sum - simulated
QT board

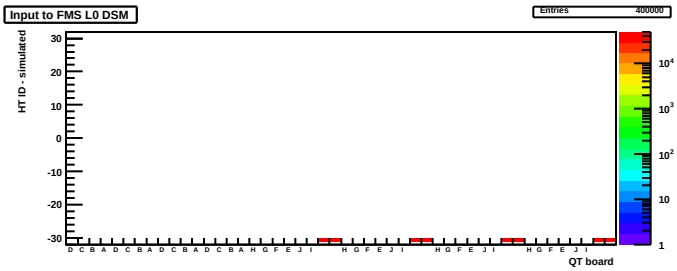

Input to FMS L0 DSM
Entries 2400000
QT8(3) sum
QT board

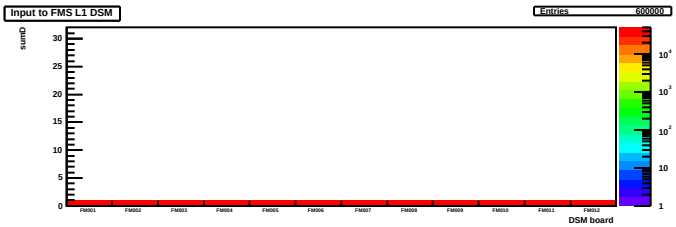

Input to FMS L0 DSM
Entries 400000
QT8(3) sum - simulated
QT board

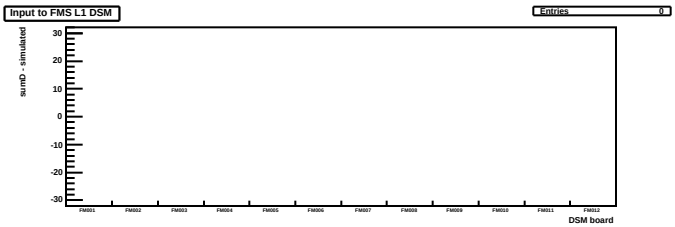

Input to FMS L0 DSM
Entries 2400000
HT ADC
QT board

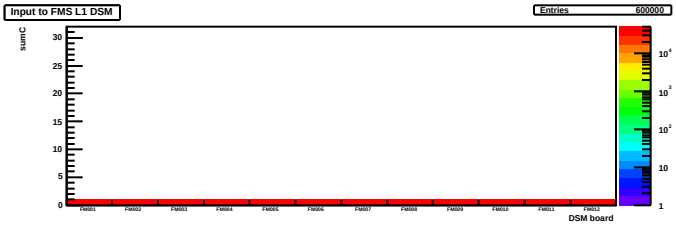

Input to FMS L0 DSM
Entries 400000
HT ADC - simulated
QT board

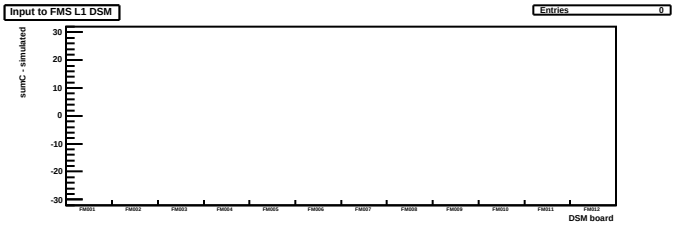

Input to FMS L0 DSM
Entries 2400000
HT ID
QT board

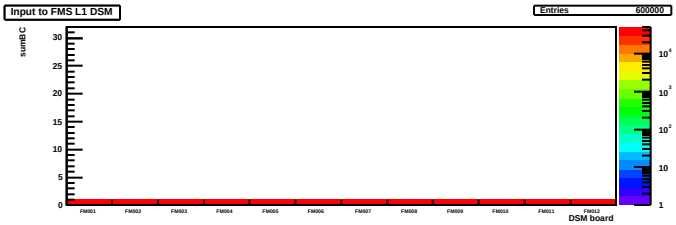

Input to FMS L0 DSM
Entries 400000
HT ID - simulated
QT board

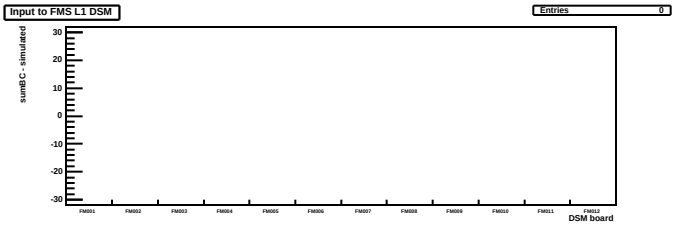

Input to FMS L1 DSM
Entries 600000
sumD
DSM board

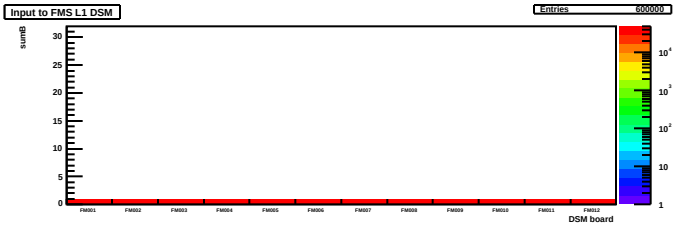

Input to FMS L1 DSM
Entries 0
sumD - simulated
DSM board

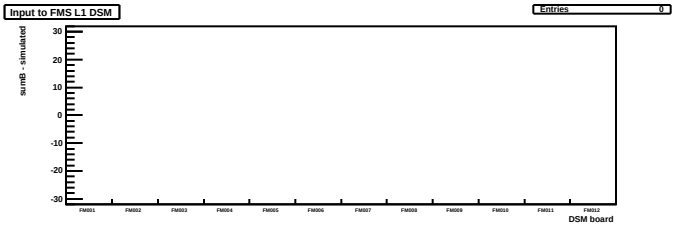

Input to FMS L1 DSM
Entries 600000
sumC
DSM board

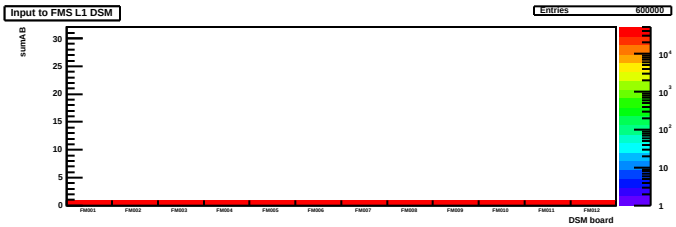

Input to FMS L1 DSM
Entries 0
sumC - simulated
DSM board

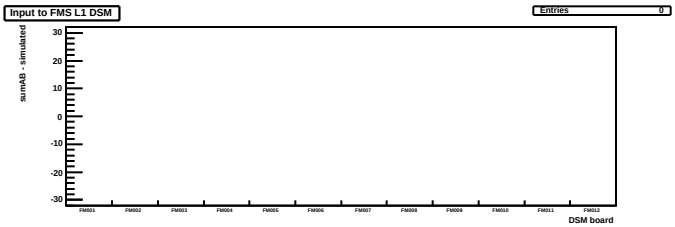

Input to FMS L1 DSM
Entries 600000
sumBC
DSM board

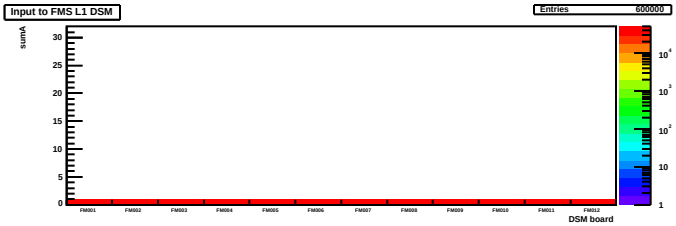

Input to FMS L1 DSM
Entries 0
sumBC - simulated
DSM board

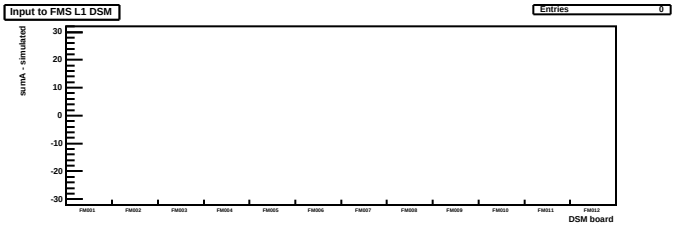

Input to FMS L1 DSM
Entries 600000
sumB
DSM board

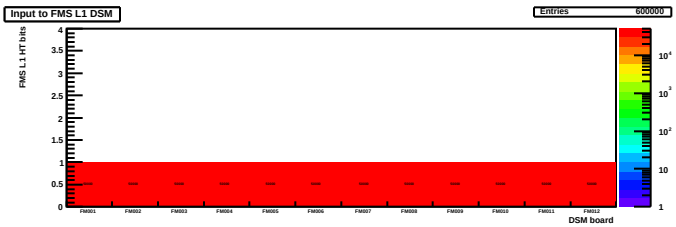

Input to FMS L1 DSM
Entries 0
sumB - simulated
DSM board

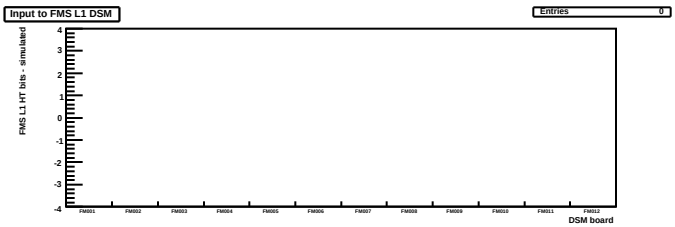

Input to FMS L1 DSM
Entries 600000
sumAB
DSM board

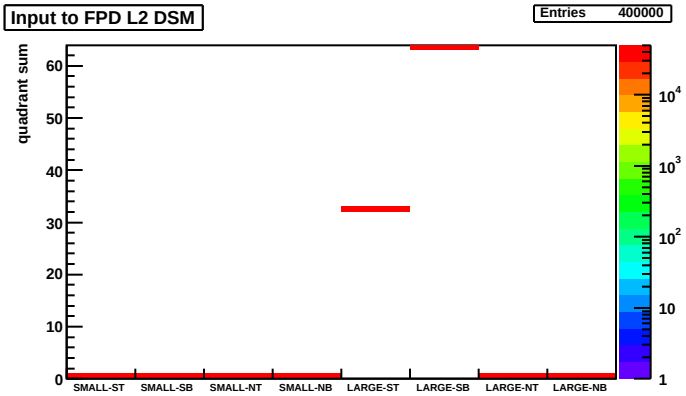

Input to FMS L1 DSM
Entries 0
sumAB - simulated
DSM board

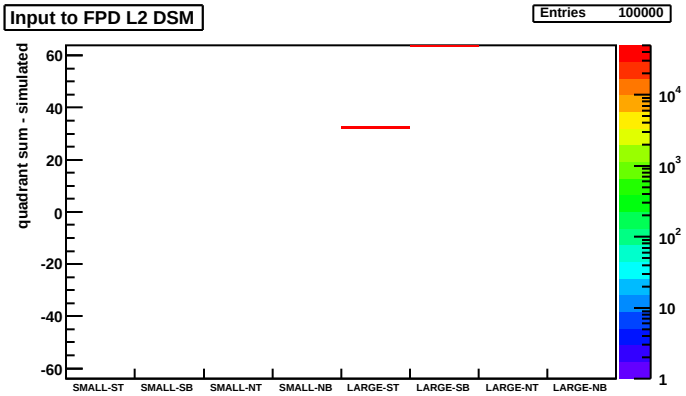

Input to FMS L1 DSM
Entries 600000
sumA
DSM board

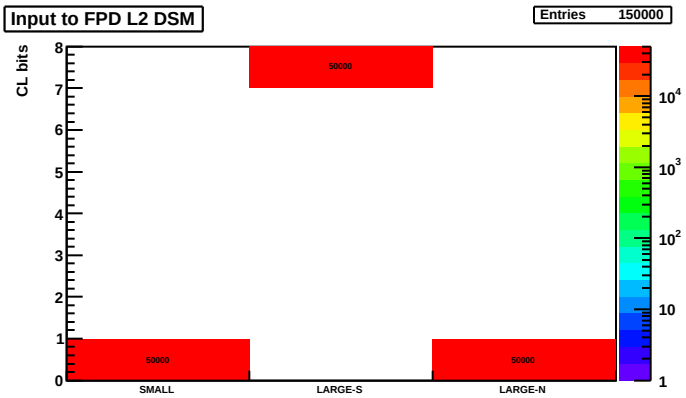

Input to FMS L1 DSM
Entries 0
sumA - simulated
DSM board

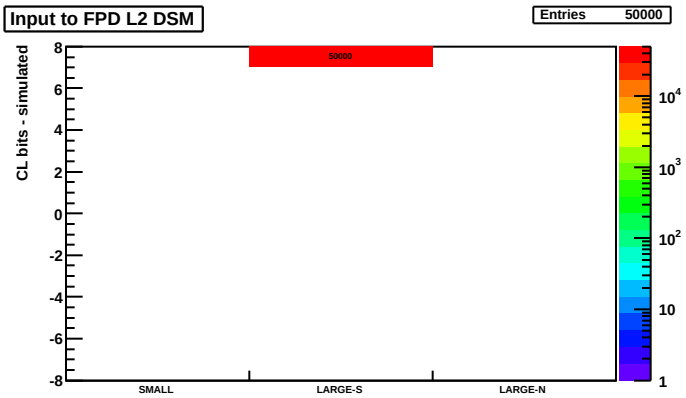

Input to FMS L1 DSM
Entries 600000
FMS L1 HT bits
DSM board

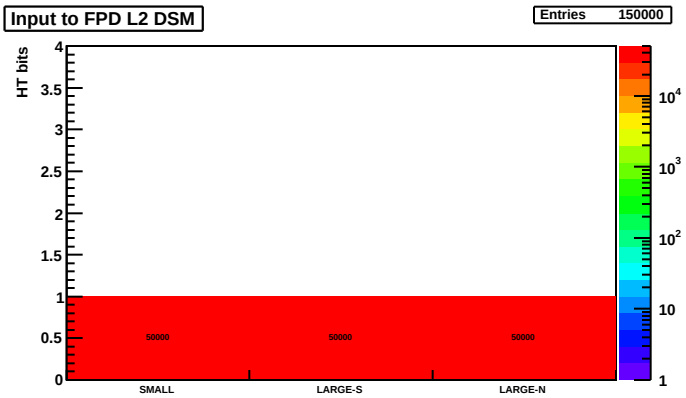

Input to FMS L1 DSM
Entries 0
FMS L1 HT bits - simulated
DSM board

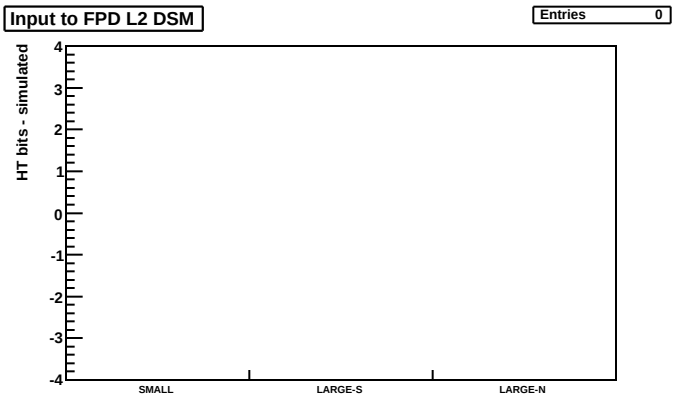

Input to FPD L2 DSM
Entries 400000
quadrant sum
SMALL-ST
SMALL-SB
SMALL-NT
SMALL-NB
LARGE-ST
LARGE-SB
LARGE-NT
LARGE-NB

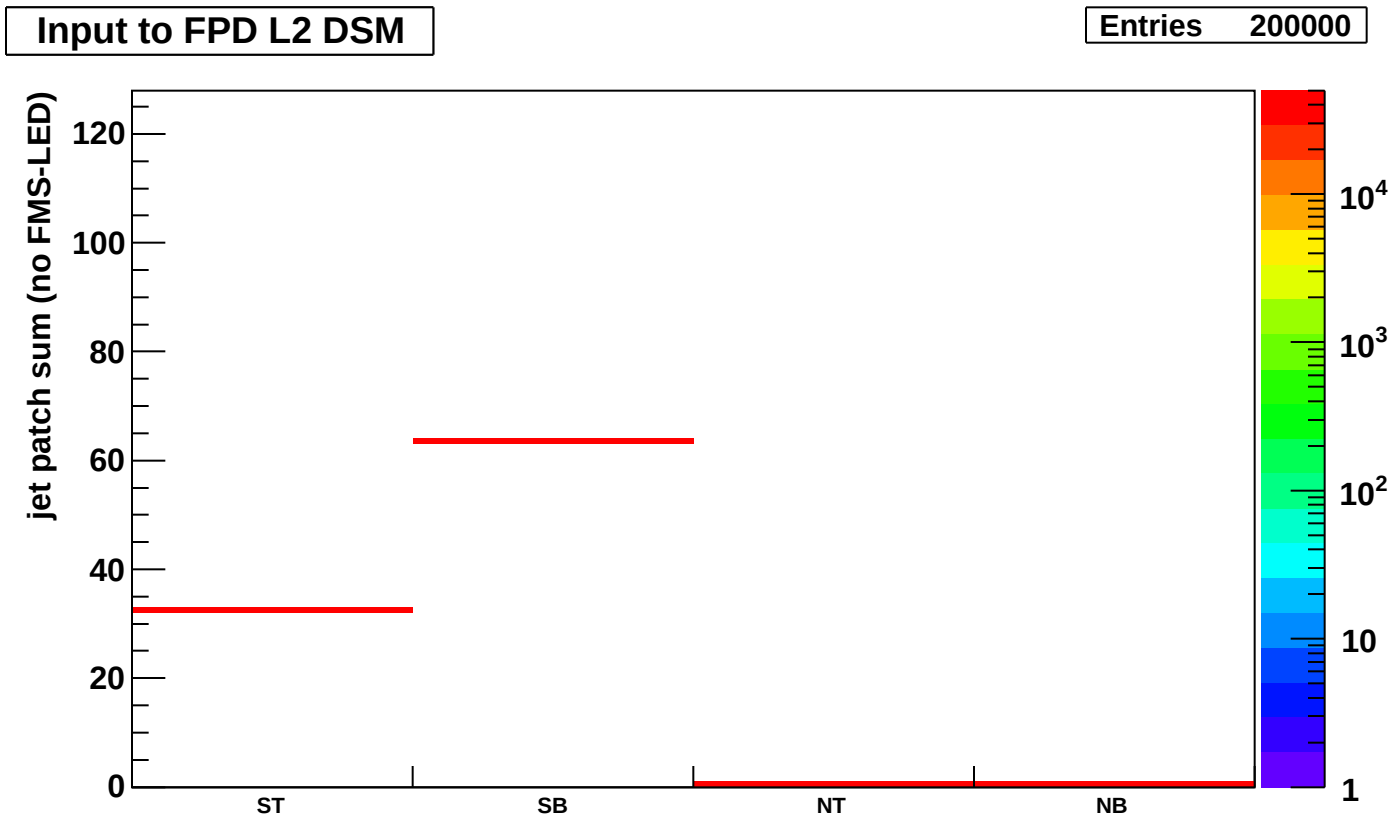

Input to FPD L2 DSM
Entries 100000
quadrant sum - simulated
SMALL-ST
SMALL-SB
SMALL-NT
SMALL-NB
LARGE-ST
LARGE-SB
LARGE-NT
LARGE-NB

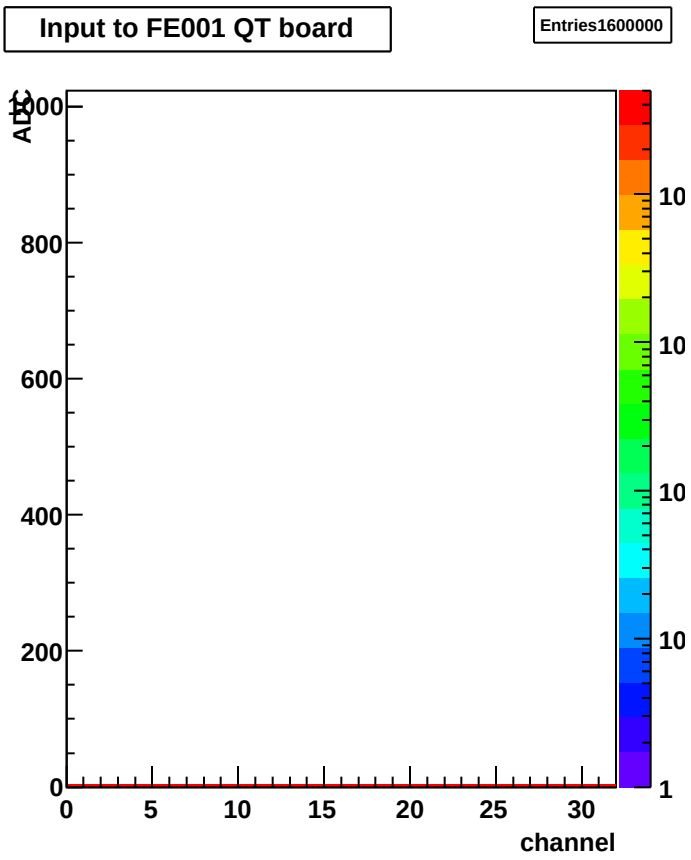

Input to FPD L2 DSM
Entries 150000
CL bits
50000
50000
50000
SMALL
LARGE-S
LARGE-N

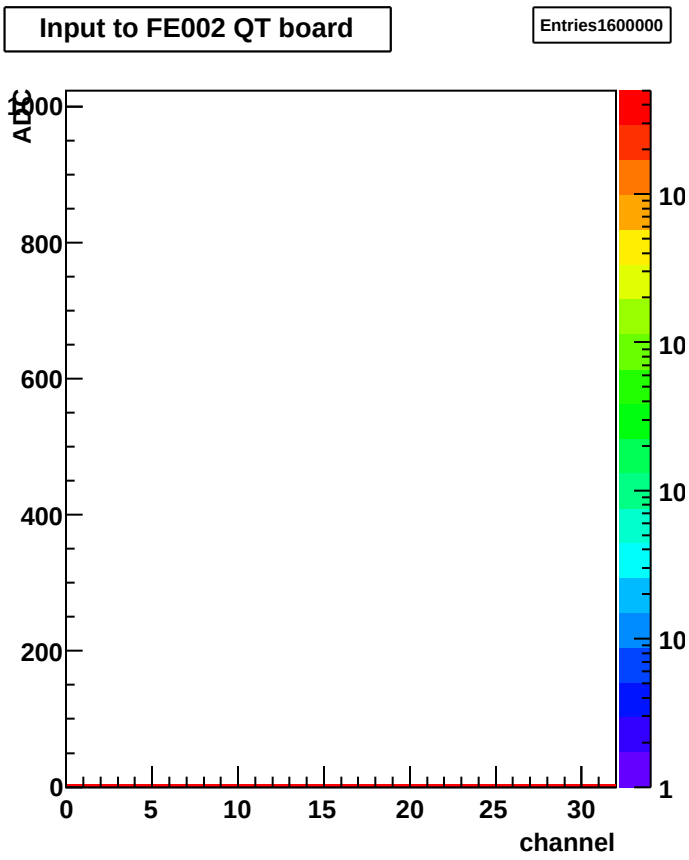

Input to FPD L2 DSM
Entries 50000
CL bits - simulated
50000
SMALL
LARGE-S
LARGE-N

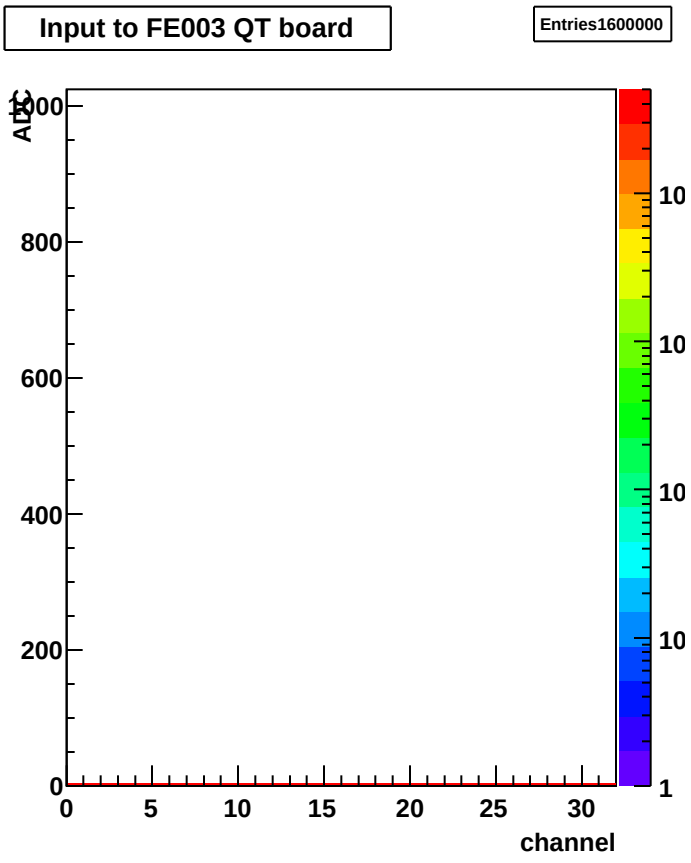

Input to FPD L2 DSM
Entries 150000
HT bits
50000
50000
50000
SMALL
LARGE-S
LARGE-N

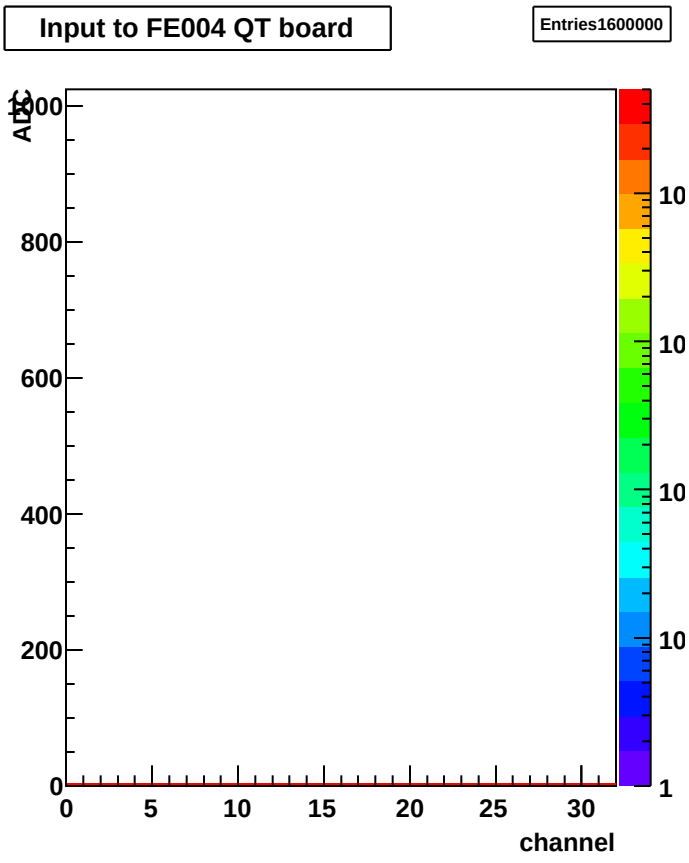

Input to FPD L2 DSM
Entries 0
HT bits - simulated
SMALL
LARGE-S
LARGE-N

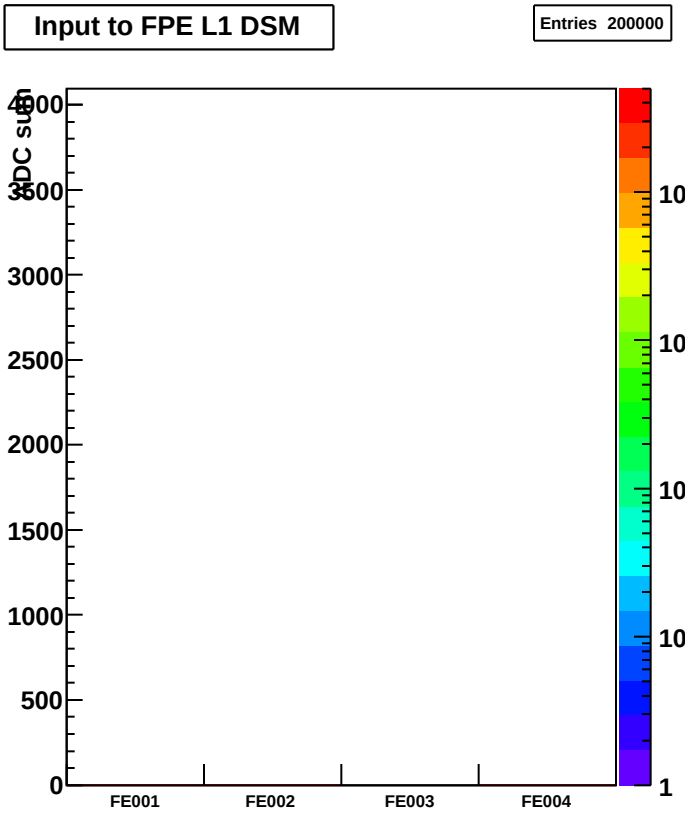

Input to FPD L2 DSM
Entries 200000
jet patch sum (no FMS-LED)
0
20
40
60
80
100
120
ST
SB
NT
NB
1
10
$10^2$
$10^3$
$10^4$

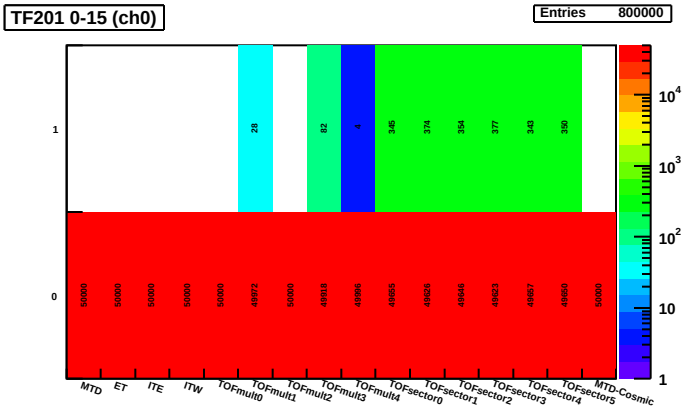

Input to FE001 QT board
Entries1600000
ADC
channel

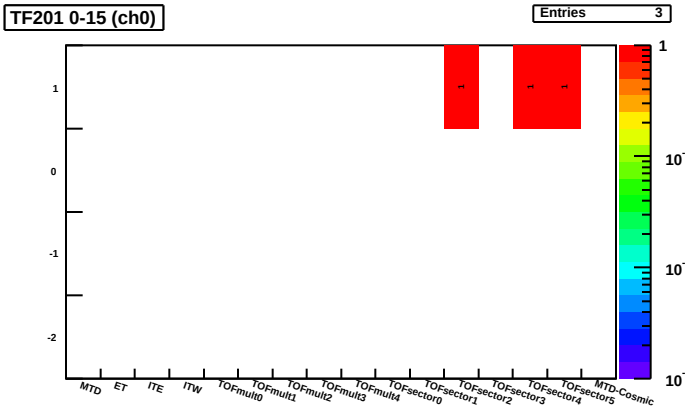

Input to FE002 QT board
Entries1600000
ADC
channel

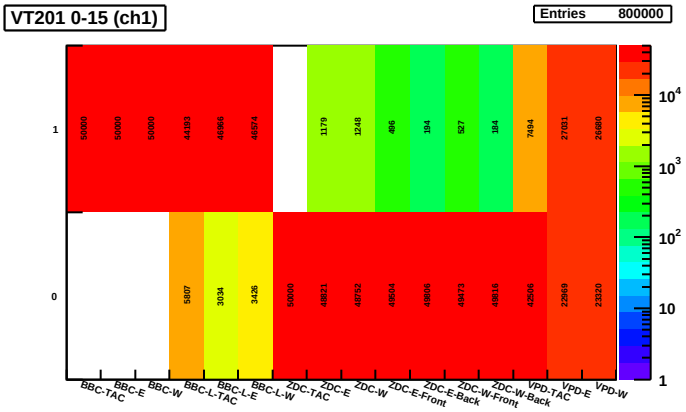

Input to FE003 QT board
Entries1600000
ADC
channel

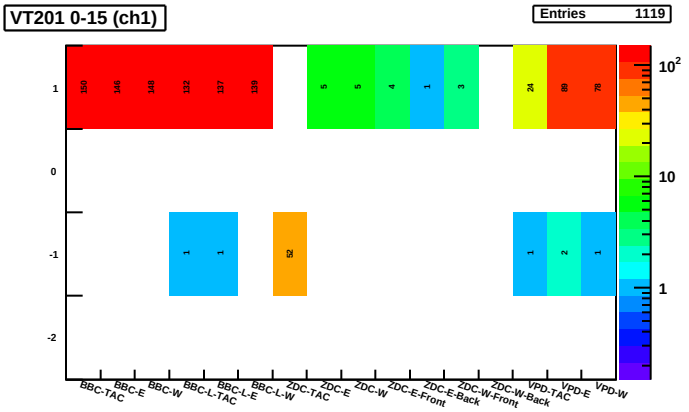

Input to FE004 QT board
Entries1600000
ADC
channel

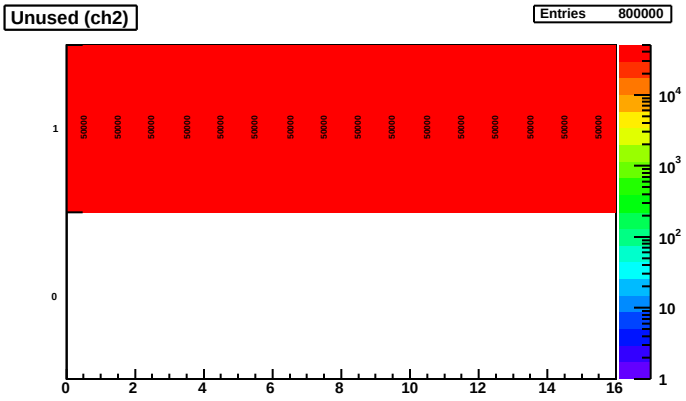

Input to FPE L1 DSM
Entries 200000
ADC sum
4000
3500
3000
2500
2000
1500
1000
500
0
FE001
FE002
FE003
FE004
10
10
10
10
1

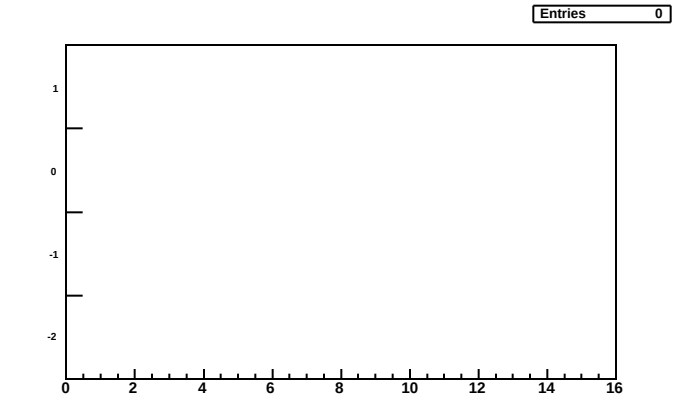

TF201 0-15 (ch0)
Entries 800000
MTD ET ITE ITW TOFmult0 TOFmult1 TOFmult2 TOFmult3 TOFmult4 TOFsector0 TOFsector1 TOFsector2 TOFsector3 TOFsector4 TOFsector5 MTD-Cosmic

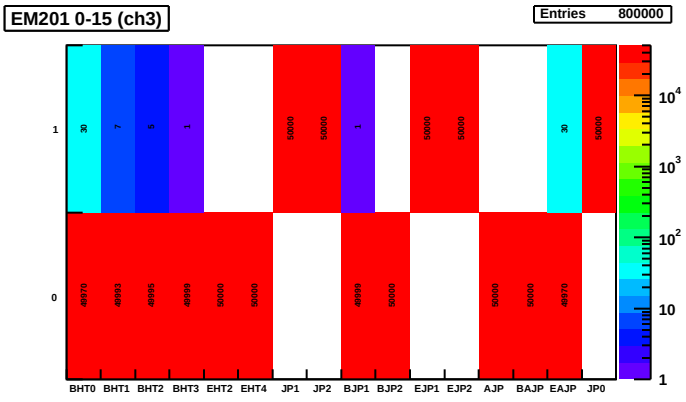

TF201 0-15 (ch0)
Entries 3
MTD ET ITE ITW TOFmult0 TOFmult1 TOFmult2 TOFmult3 TOFmult4 TOFsector0 TOFsector1 TOFsector2 TOFsector3 TOFsector4 TOFsector5 MTD-Cosmic

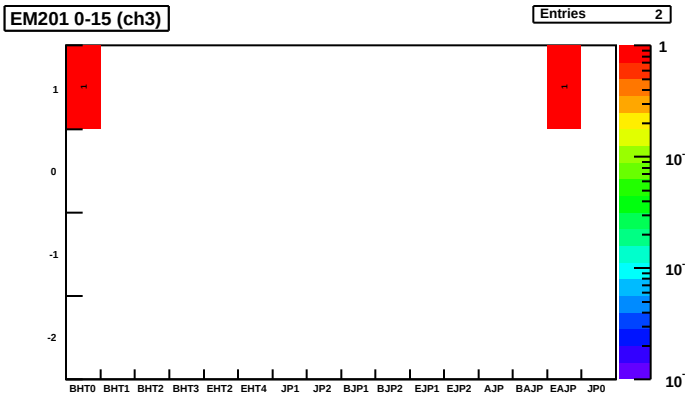

VT201 0-15 (ch1)
Entries 800000
BBC-TAC BBC-E BBC-W BBC-L-TAC BBC-L-E BBC-L-W ZDC-TAC ZDC-E ZDC-W ZDC-E-Front ZDC-E-Back ZDC-W-Front ZDC-W-Back VPD-TAC VPD-E VPD-W


VT201 0-15 (ch1)
Entries 1119
BBC-TAC BBC-E BBC-W BBC-L-TAC BBC-L-E BBC-L-W ZDC-TAC ZDC-E ZDC-W ZDC-E-Front ZDC-E-Back ZDC-W-Front ZDC-W-Back VPD-TAC VPD-E VPD-W

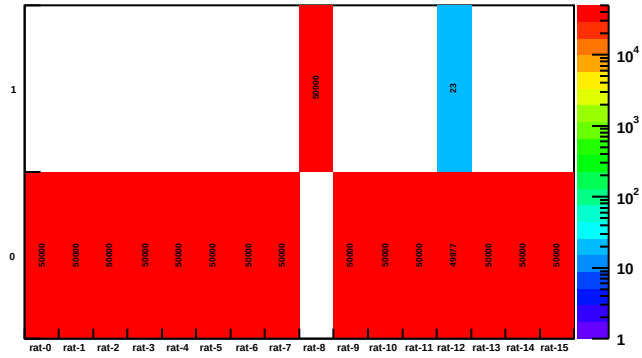

Unused (ch2)
Entries 800000

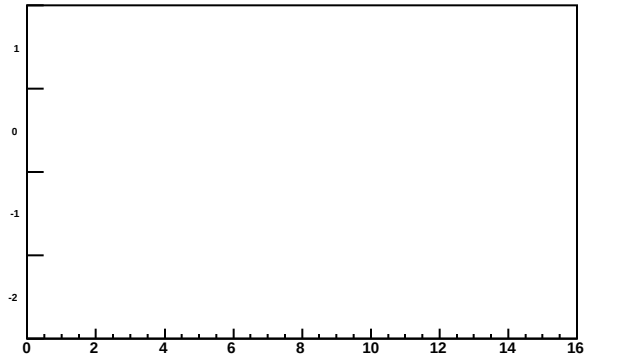

Entries 0


EM201 0-15 (ch3)
Entries 800000
BHT0 BHT1 BHT2 BHT3 EHT2 EHT4 JP1 JP2 BJP1 BJP2 EJP1 EJP2 AJP BAJP EAJP JP0

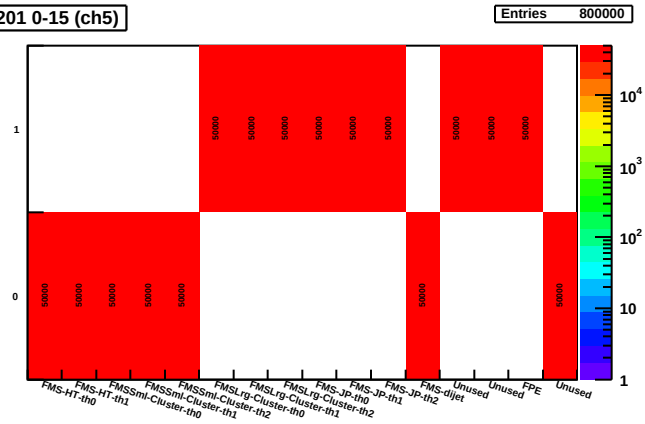

EM201 0-15 (ch3)
Entries 2
BHT0 BHT1 BHT2 BHT3 EHT2 EHT4 JP1 JP2 BJP1 BJP2 EJP1 EJP2 AJP BAJP EAJP JP0

**RAT board (ch4)**

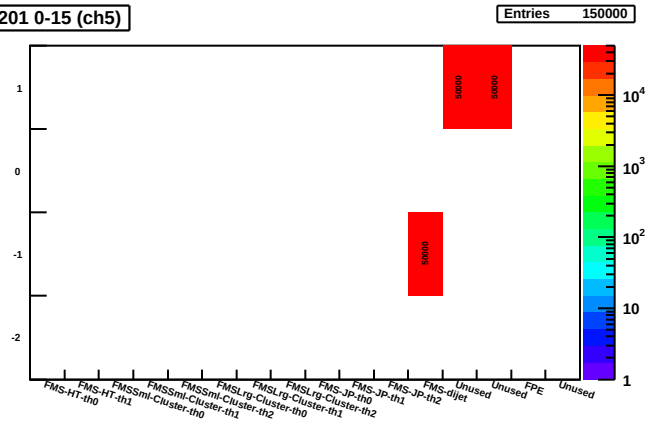


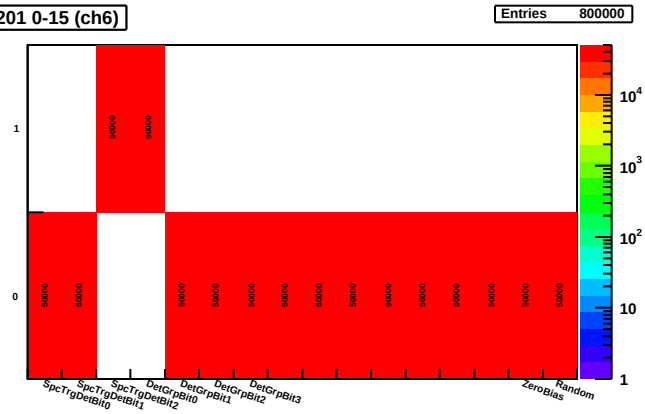

**FP201 0-15 (ch5)**

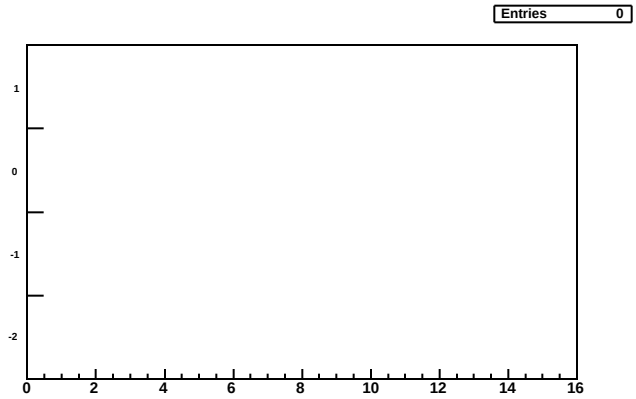


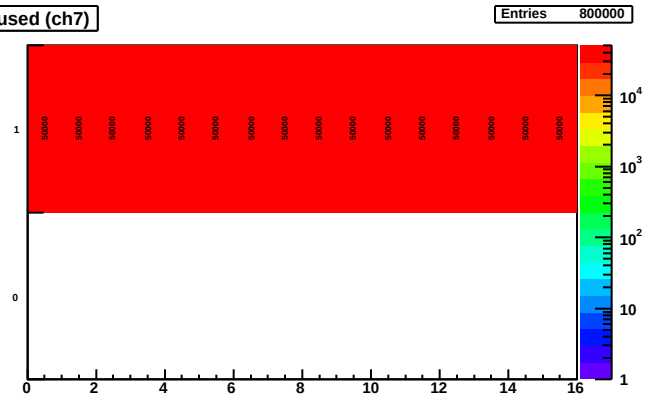
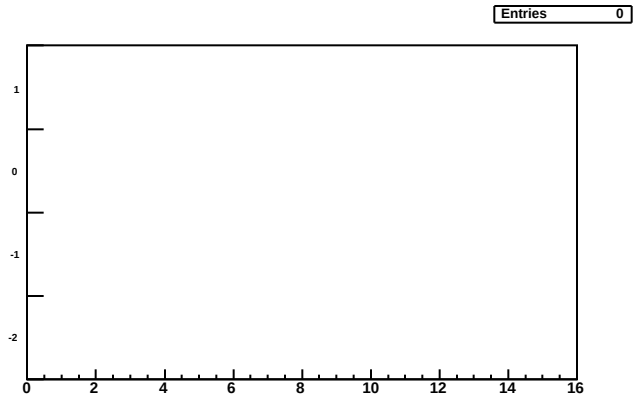

**FP201 0-15 (ch5)**




**ST201 0-15 (ch6)**




**Unused (ch7)**