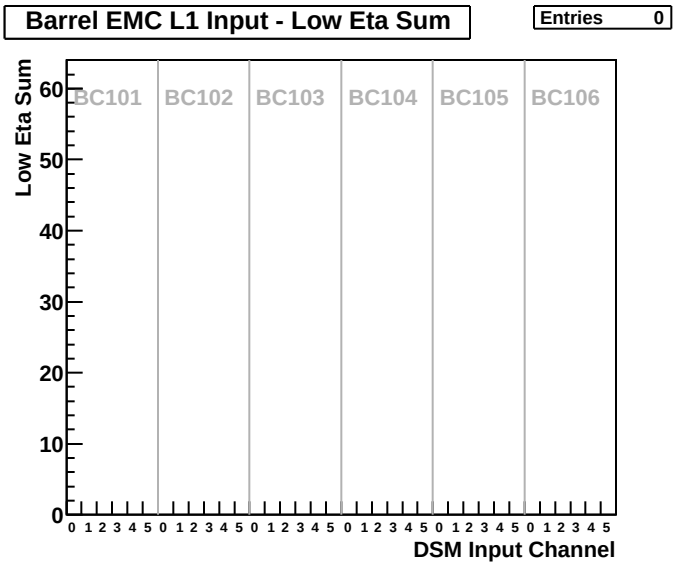
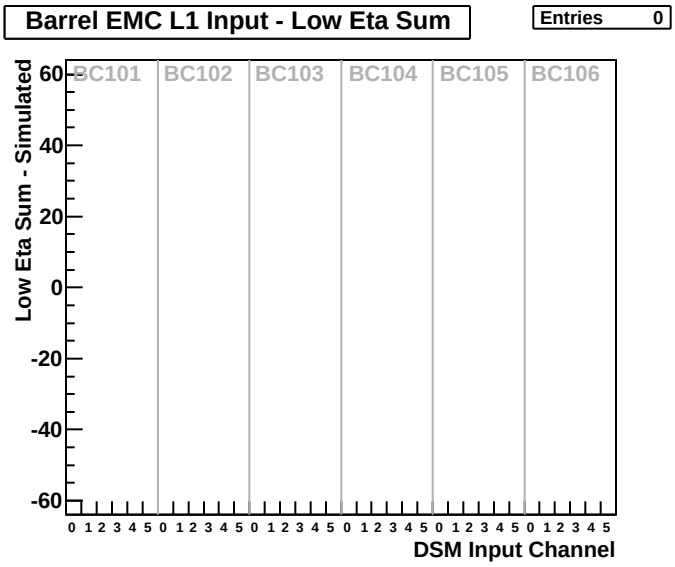
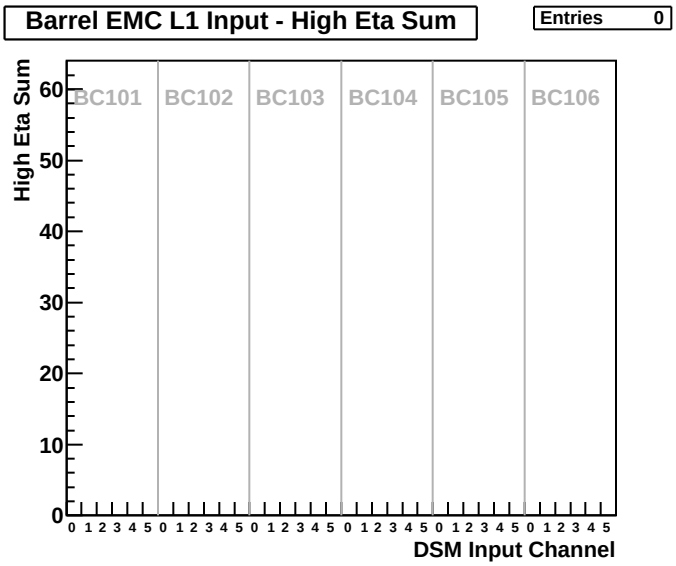
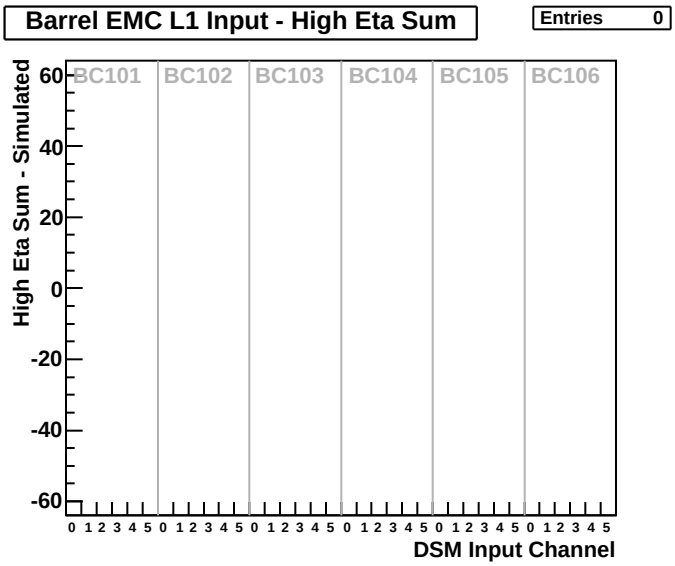
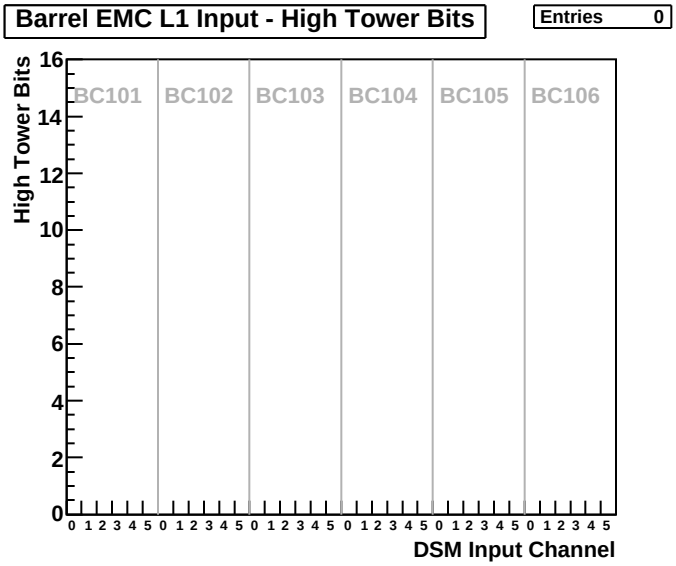
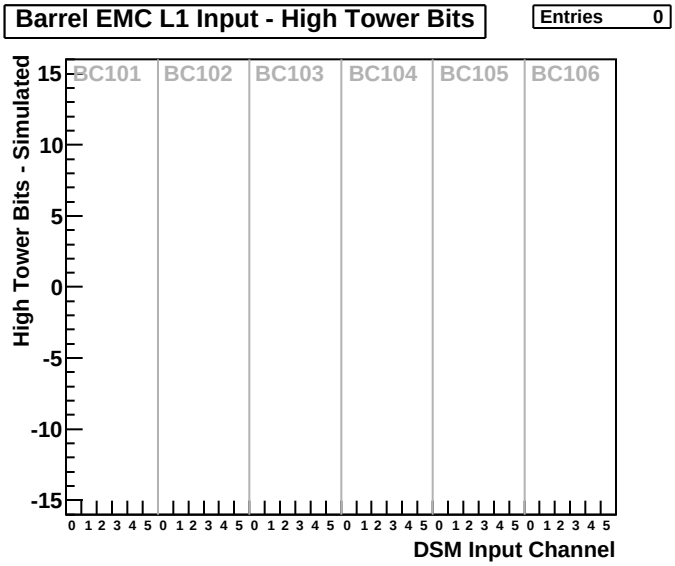

Barrel EMC L1 Input - Low Eta Sum
Entries 0
Low Eta Sum
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

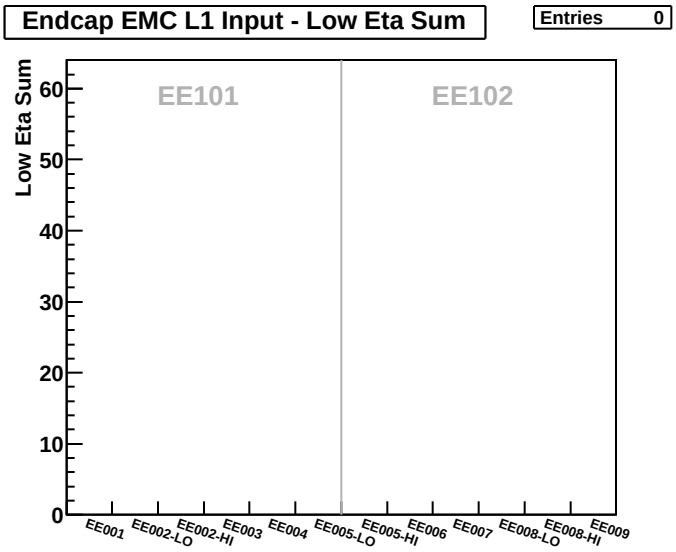

Barrel EMC L1 Input - Low Eta Sum
Entries 0
Low Eta Sum - Simulated
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

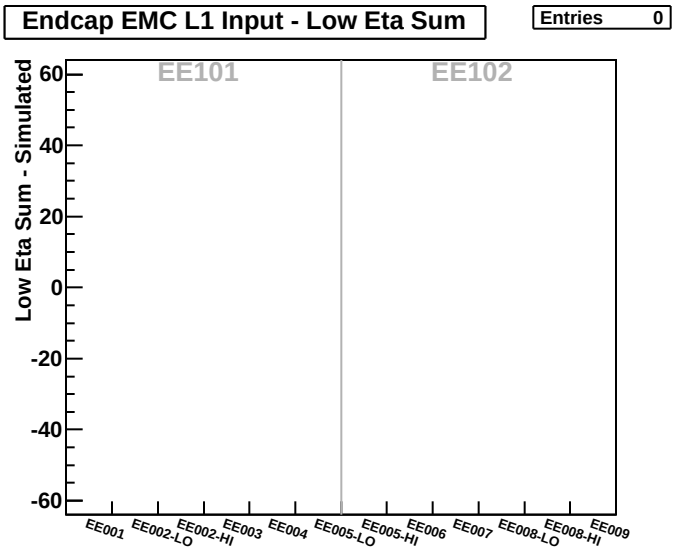

Barrel EMC L1 Input - High Eta Sum
Entries 0
High Eta Sum
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

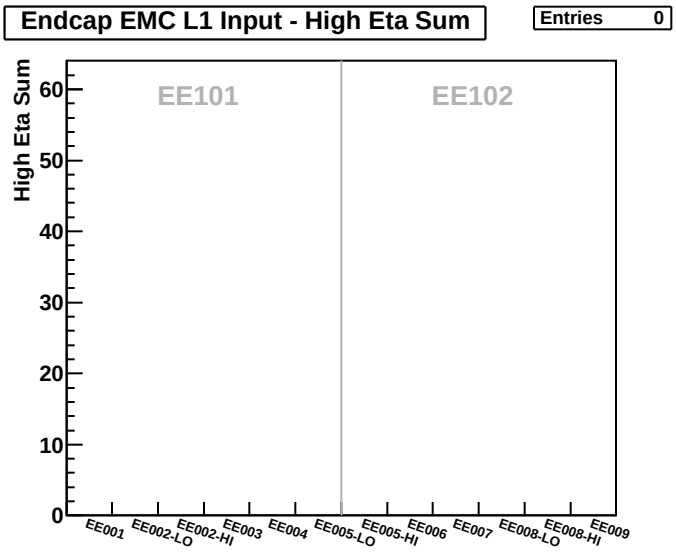

Barrel EMC L1 Input - High Eta Sum
Entries 0
High Eta Sum - Simulated
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

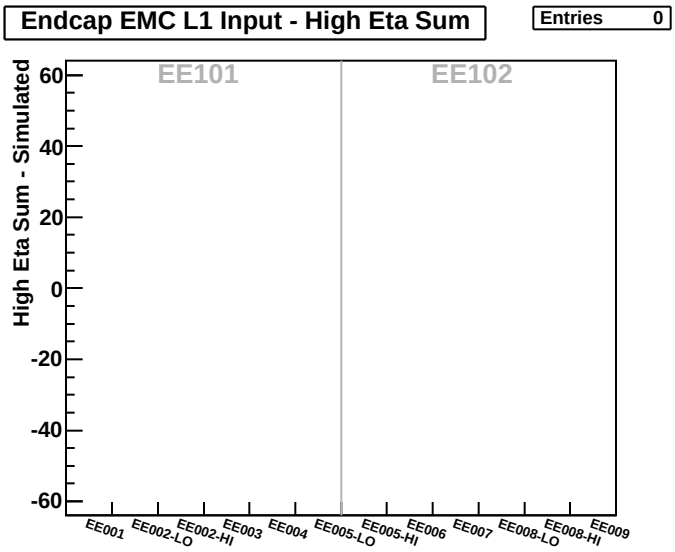

Barrel EMC L1 Input - High Tower Bits
Entries 0
High Tower Bits
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

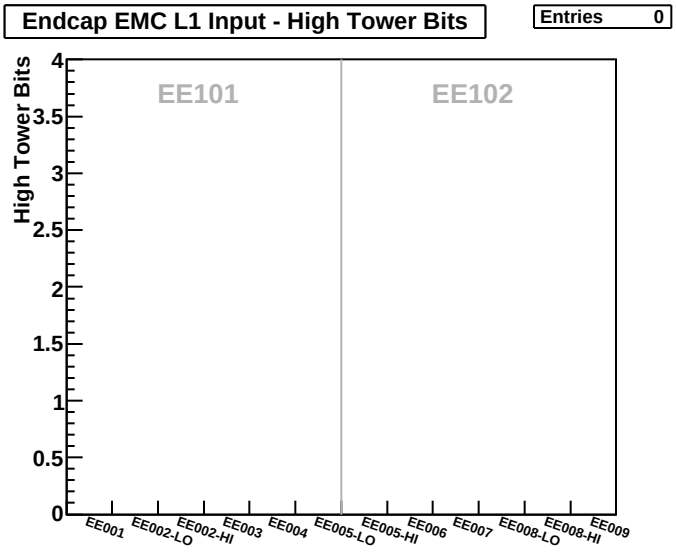

Barrel EMC L1 Input - High Tower Bits
Entries 0
High Tower Bits - Simulated
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

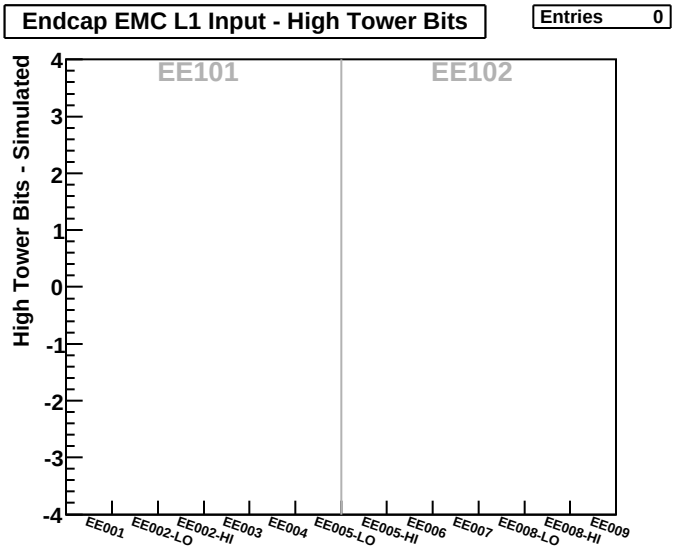

Endcap EMC L1 Input - Low Eta Sum
Entries 0
Low Eta Sum
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

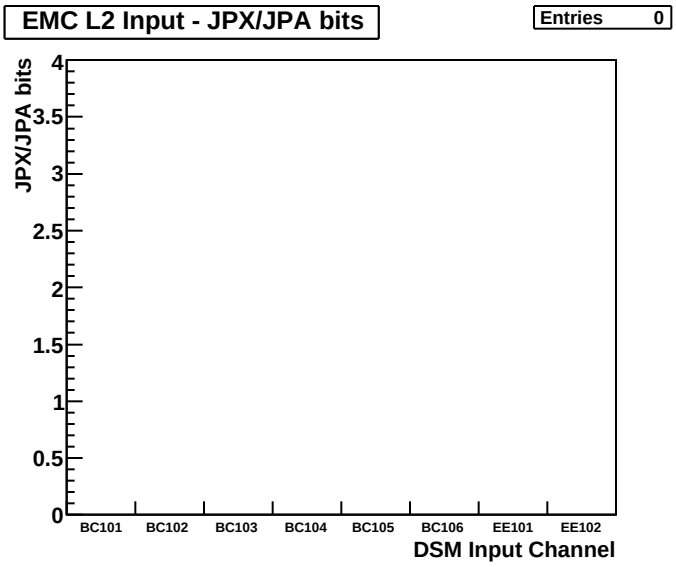

Endcap EMC L1 Input - Low Eta Sum
Entries 0
Low Eta Sum - Simulated
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

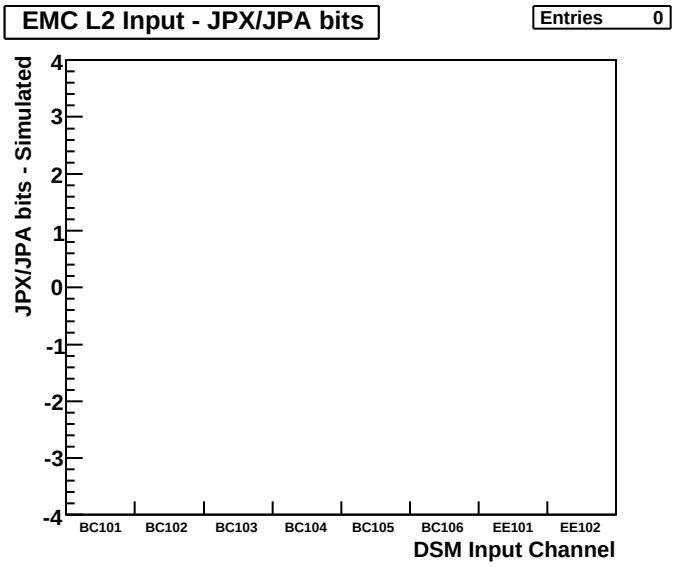

Endcap EMC L1 Input - High Eta Sum
Entries 0
High Eta Sum
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

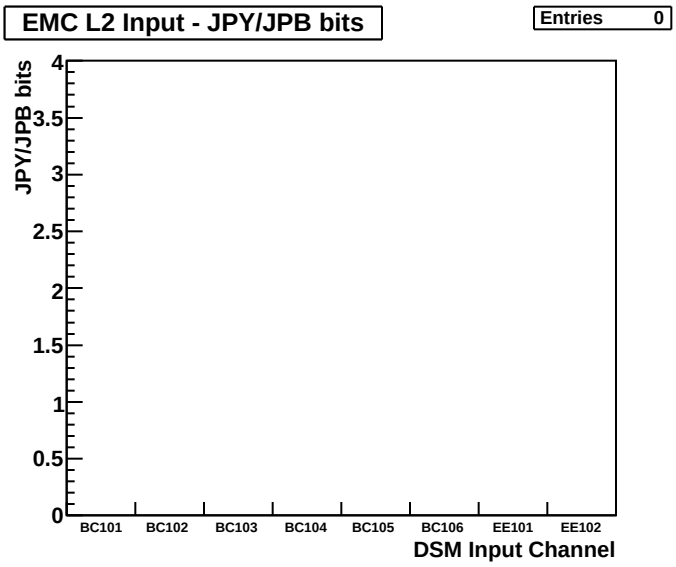

Endcap EMC L1 Input - High Eta Sum
Entries 0
High Eta Sum - Simulated
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

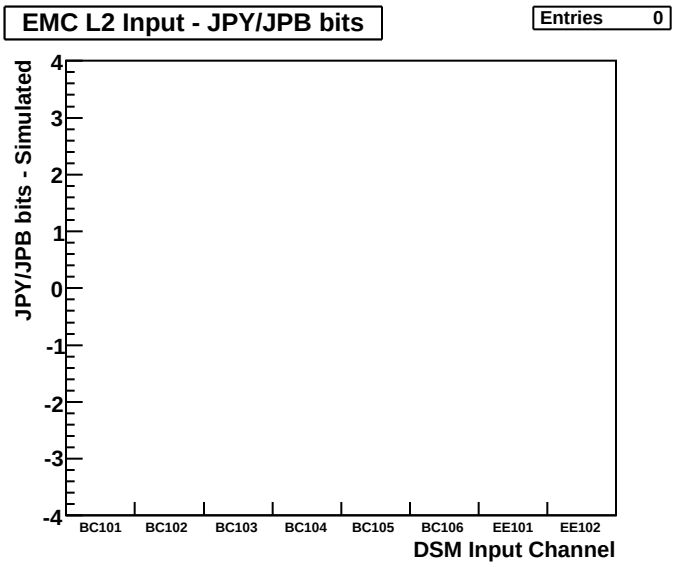

Endcap EMC L1 Input - High Tower Bits
Entries 0
High Tower Bits
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

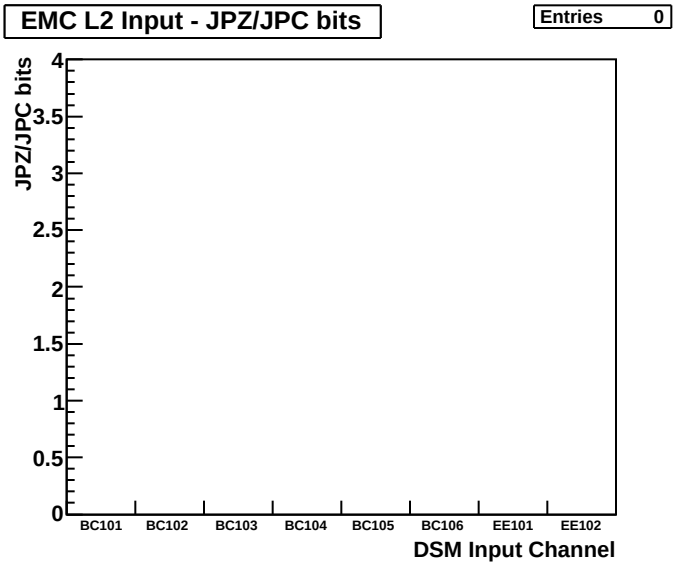

Endcap EMC L1 Input - High Tower Bits
Entries 0
High Tower Bits - Simulated
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

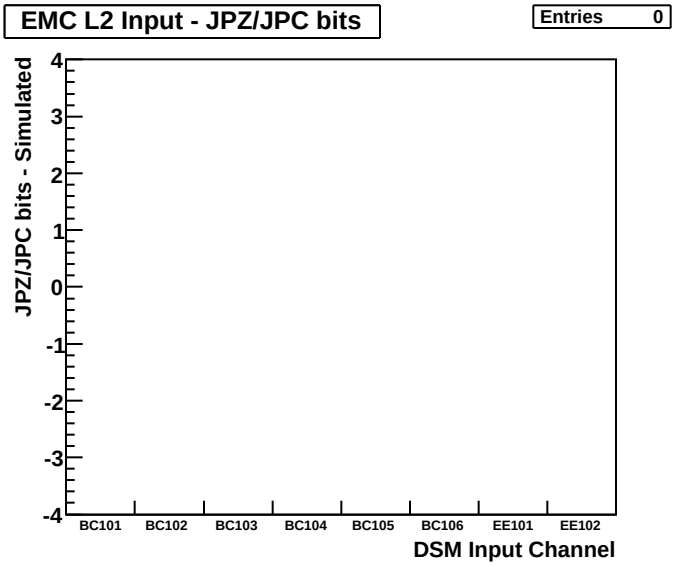

EMC L2 Input - JPX/JPA bits
Entries 0
JPX/JPA bits
4
3.5
3
2.5
2
1.5
1
0.5
0
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102
DSM Input Channel

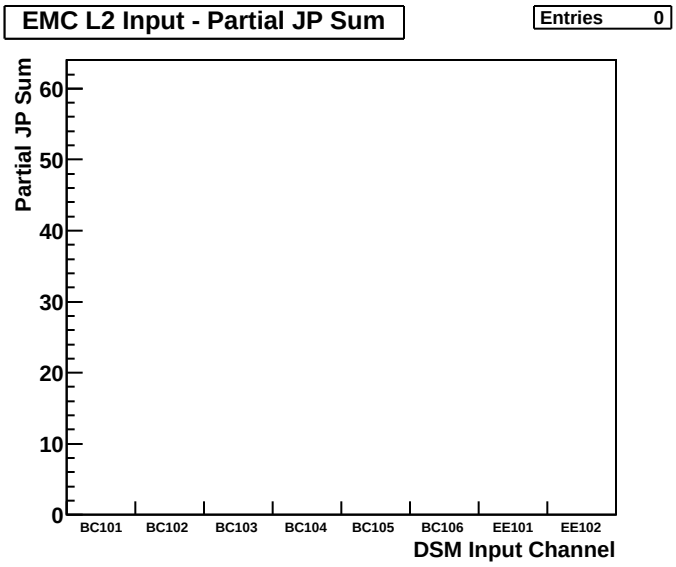

EMC L2 Input - JPX/JPA bits
Entries 0
JPX/JPA bits - Simulated
4
3
2
1
0
-1
-2
-3
-4
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102
DSM Input Channel

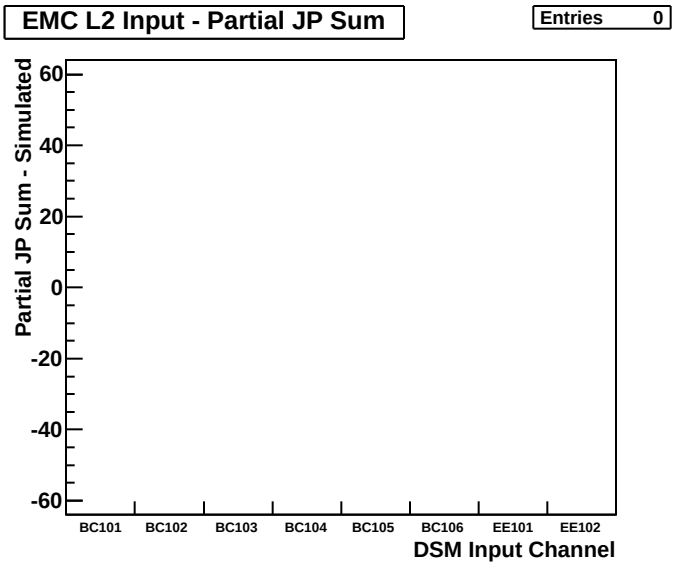

EMC L2 Input - JPY/JPB bits
Entries 0
JPY/JPB bits
4
3.5
3
2.5
2
1.5
1
0.5
0
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102
DSM Input Channel

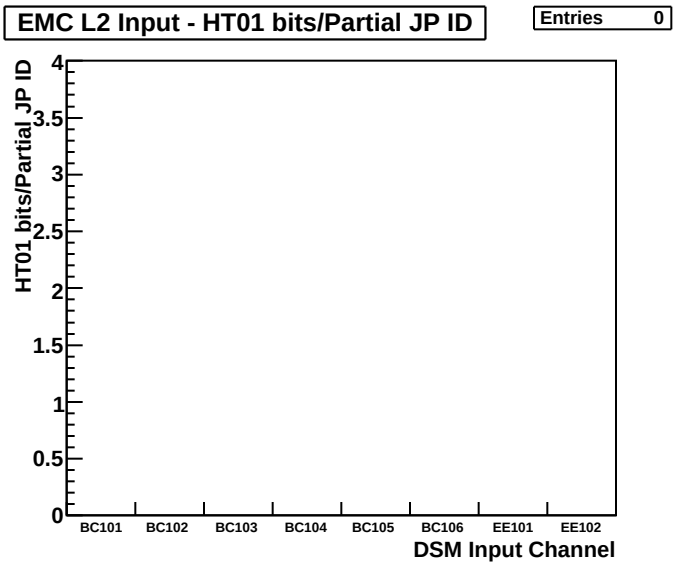

EMC L2 Input - JPY/JPB bits
Entries 0
JPY/JPB bits - Simulated
4
3
2
1
0
-1
-2
-3
-4
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102
DSM Input Channel

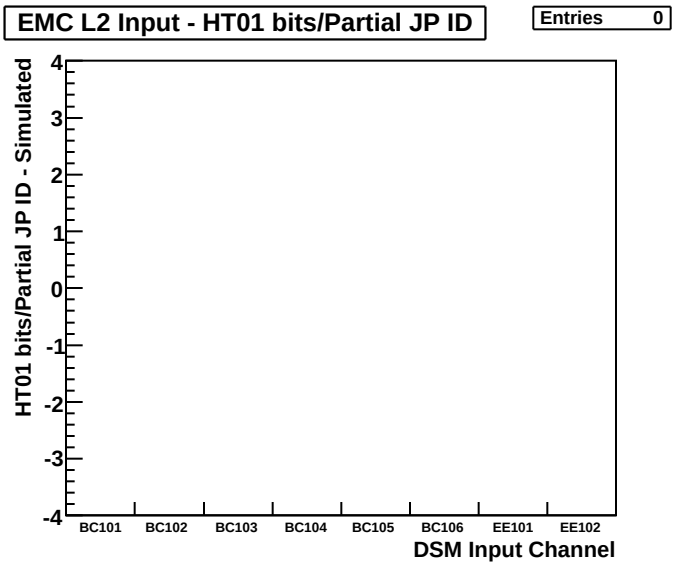

EMC L2 Input - JPZ/JPC bits
Entries 0
JPZ/JPC bits
4
3.5
3
2.5
2
1.5
1
0.5
0
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102
DSM Input Channel

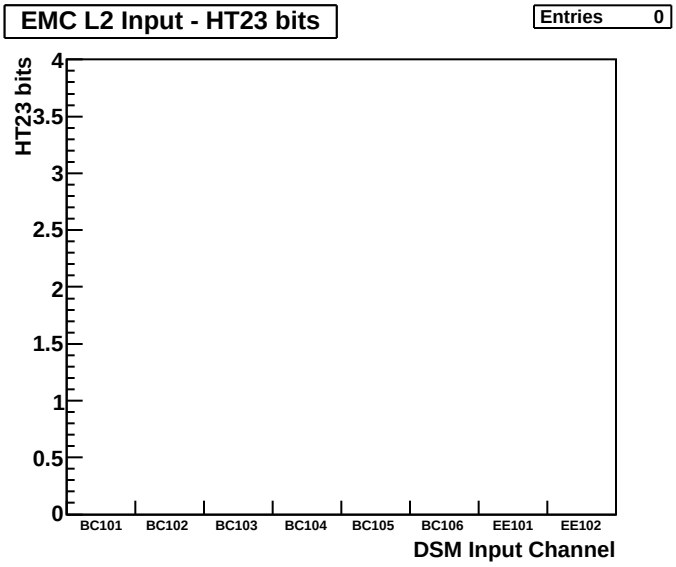

EMC L2 Input - JPZ/JPC bits
Entries 0
JPZ/JPC bits - Simulated
4
3
2
1
0
-1
-2
-3
-4
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102
DSM Input Channel

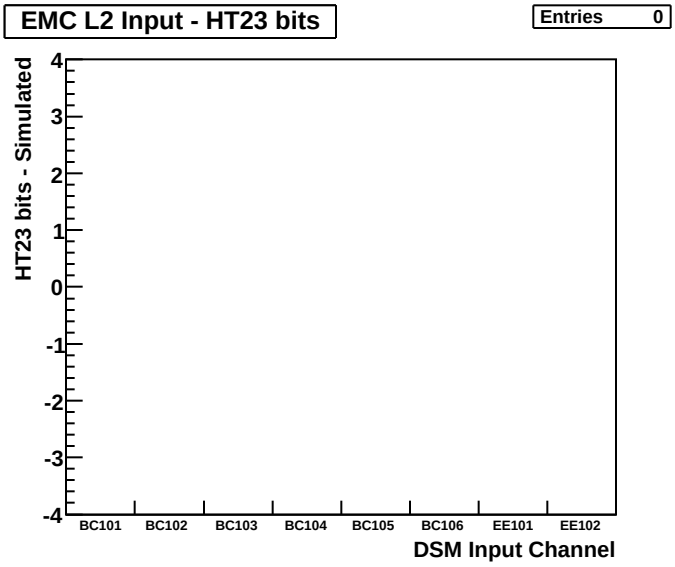

EMC L2 Input - Partial JP Sum
Entries 0
Partial JP Sum
0
10
20
30
40
50
60
BC101
BC102
BC103
BC104
BC105
BC106
EE101
EE102
DSM Input Channel

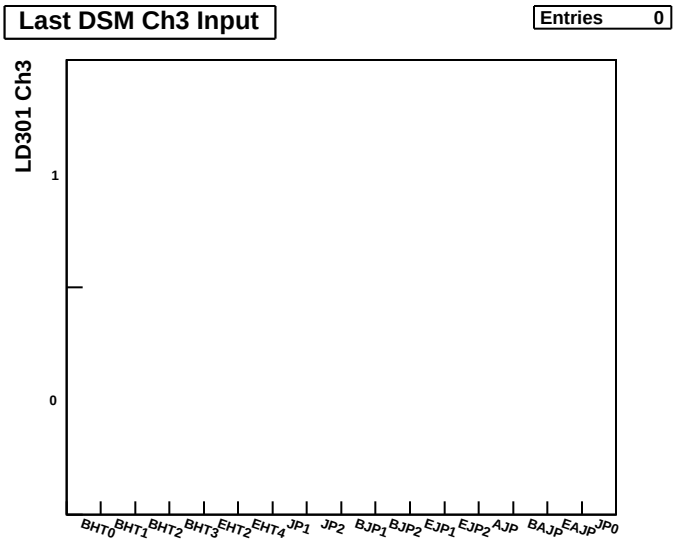

EMC L2 Input - Partial JP Sum
Entries 0
Partial JP Sum - Simulated
60
40
20
0
-20
-40
-60
BC101
BC102
BC103
BC104
BC105
BC106
EE101
EE102
DSM Input Channel

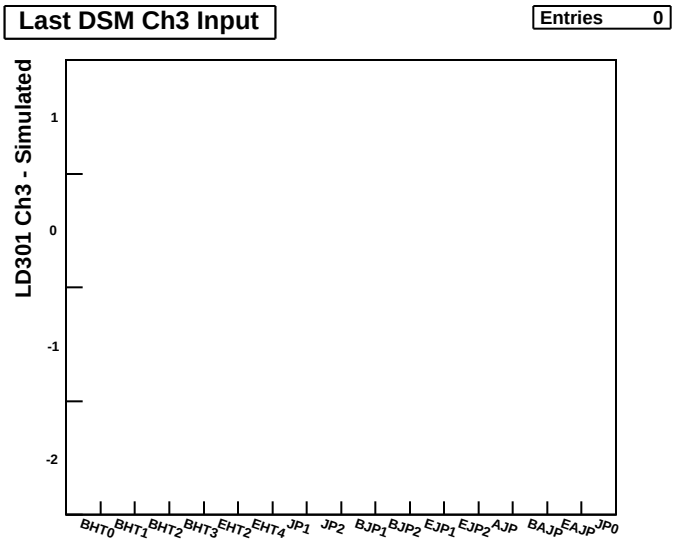

EMC L2 Input - HT01 bits/Partial JP ID
Entries 0
HT01 bits/Partial JP ID
0
0.5
1
1.5
2
2.5
3
3.5
4
BC101
BC102
BC103
BC104
BC105
BC106
EE101
EE102
DSM Input Channel

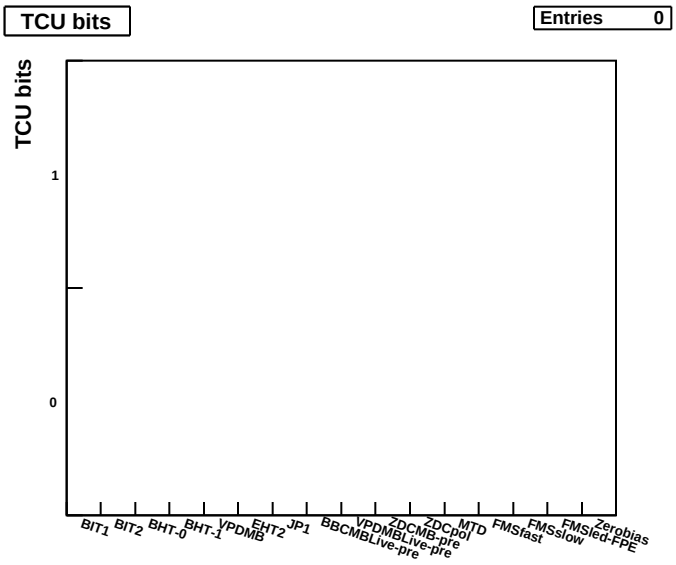

EMC L2 Input - HT01 bits/Partial JP ID
Entries 0
HT01 bits/Partial JP ID - Simulated
4
3
2
1
0
-1
-2
-3
-4
BC101
BC102
BC103
BC104
BC105
BC106
EE101
EE102
DSM Input Channel

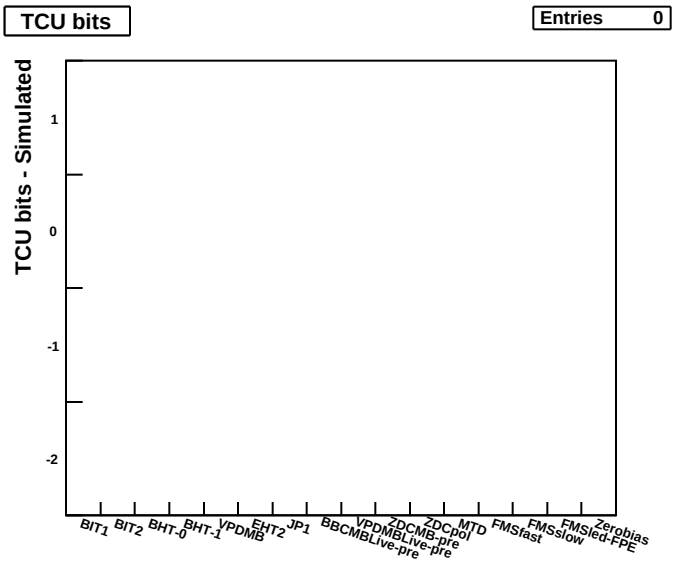

EMC L2 Input - HT23 bits
Entries 0
HT23 bits
0
0.5
1
1.5
2
2.5
3
3.5
4
BC101
BC102
BC103
BC104
BC105
BC106
EE101
EE102
DSM Input Channel

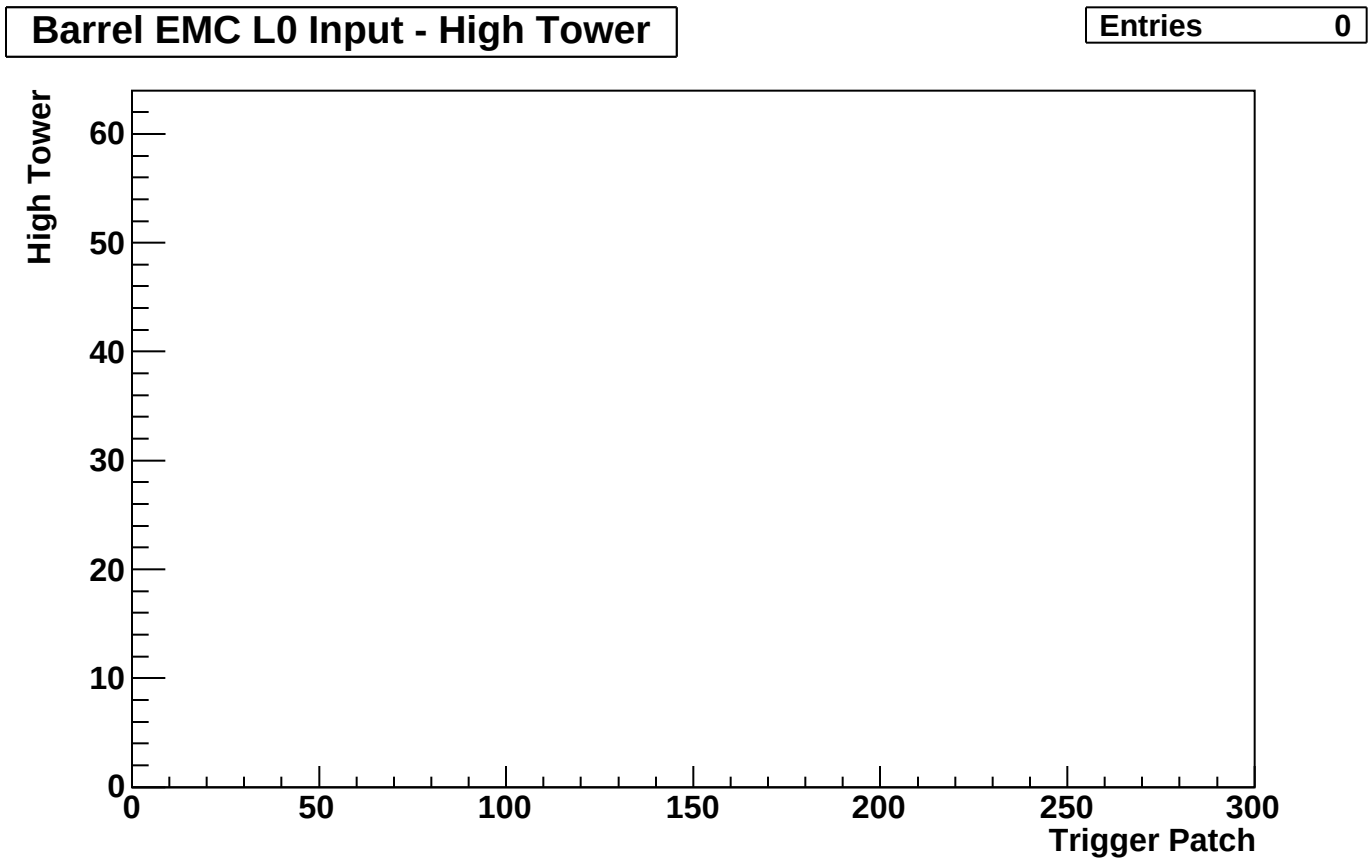

EMC L2 Input - HT23 bits
Entries 0
HT23 bits - Simulated
4
3
2
1
0
-1
-2
-3
-4
BC101
BC102
BC103
BC104
BC105
BC106
EE101
EE102
DSM Input Channel

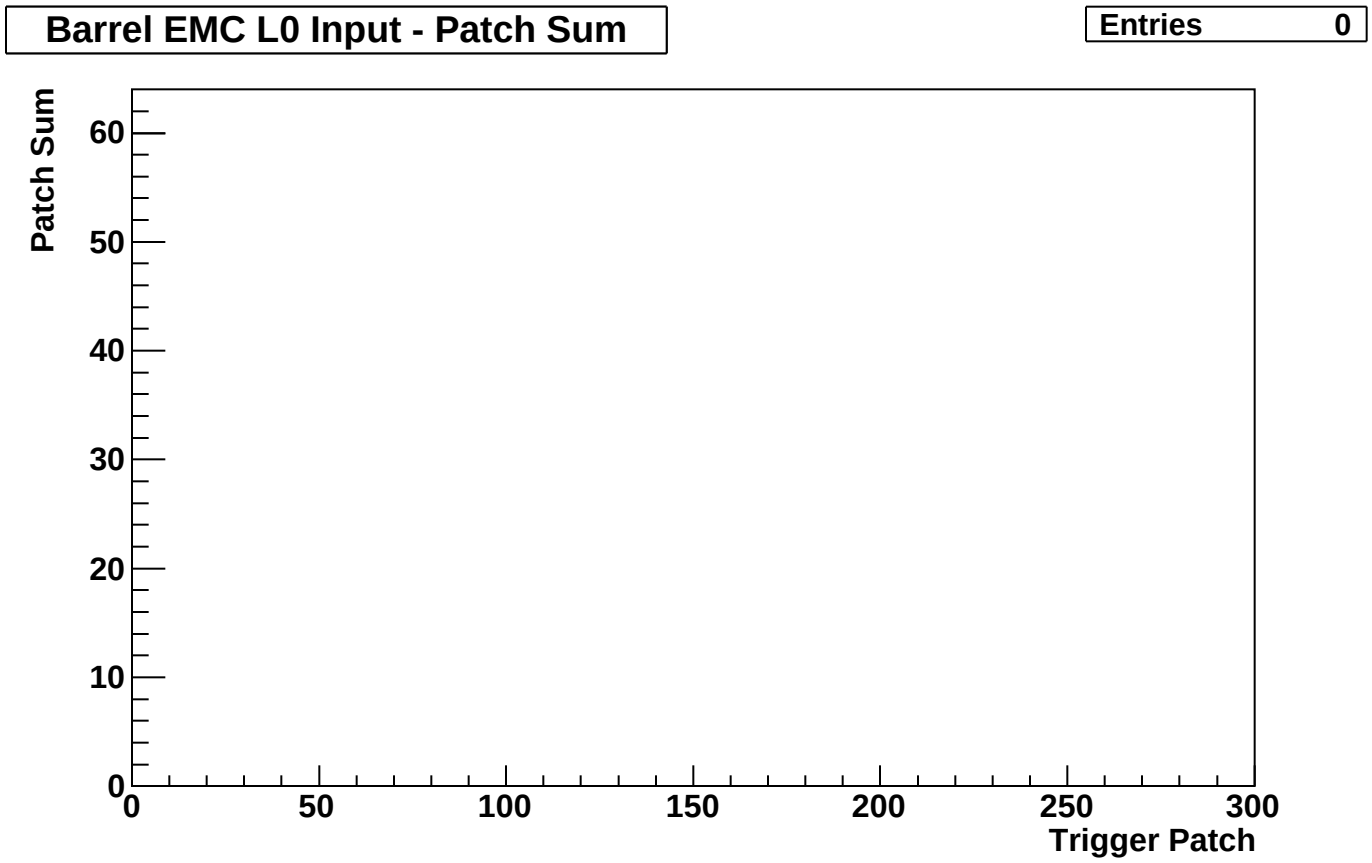

Last DSM Ch3 Input
Entries 0
LD301 Ch3
1
0
BHT0 BHT1 BHT2 BHT3 EHT2 EHT4 JP1 JP2 BJP1 BJP2 EJP1 EJP2 AJP BAJP EAJP JP0

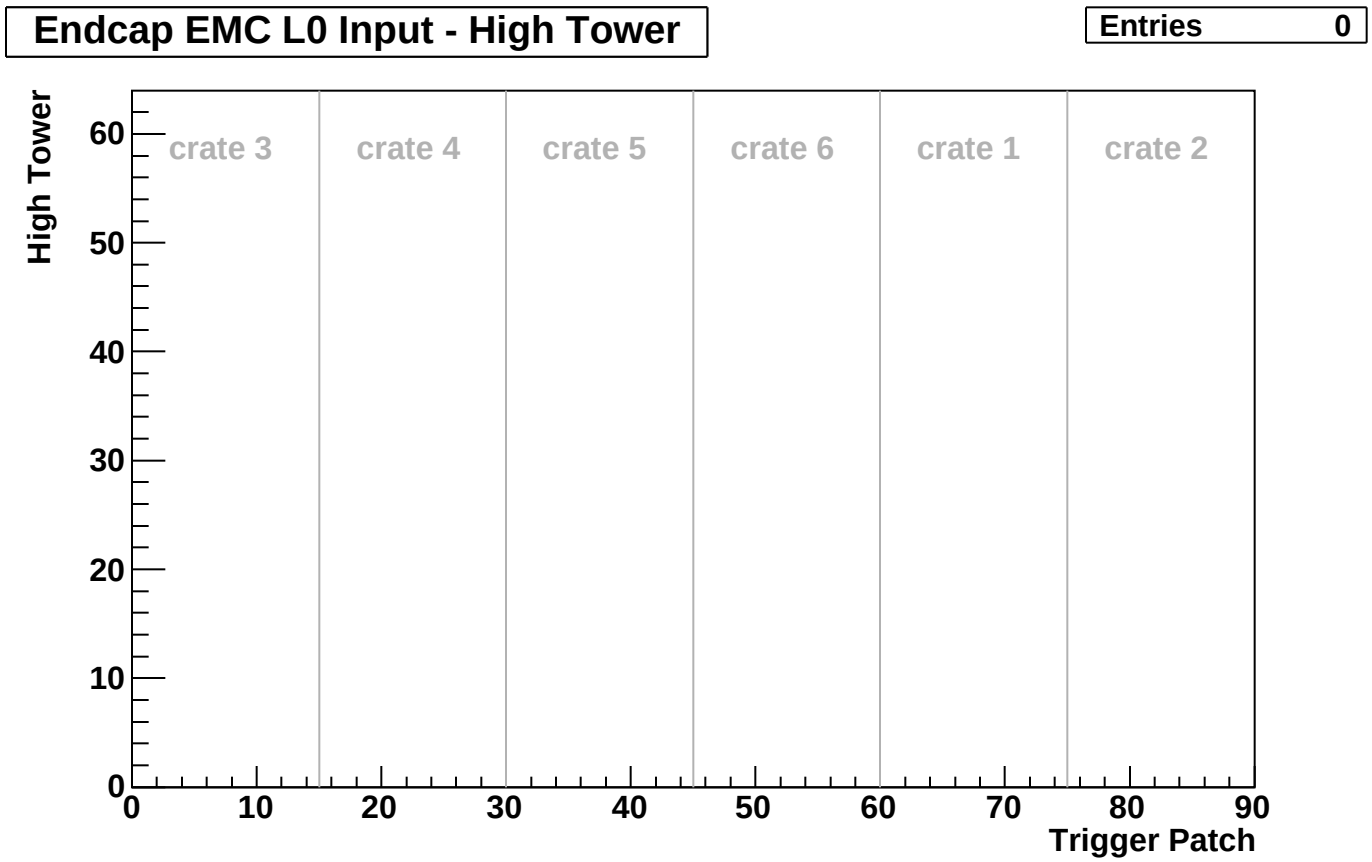

Last DSM Ch3 Input
Entries 0
LD301 Ch3 - Simulated
1
0
-1
-2
BHT0 BHT1 BHT2 BHT3 EHT2 EHT4 JP1 JP2 BJP1 BJP2 EJP1 EJP2 AJP BAJP EAJP JP0

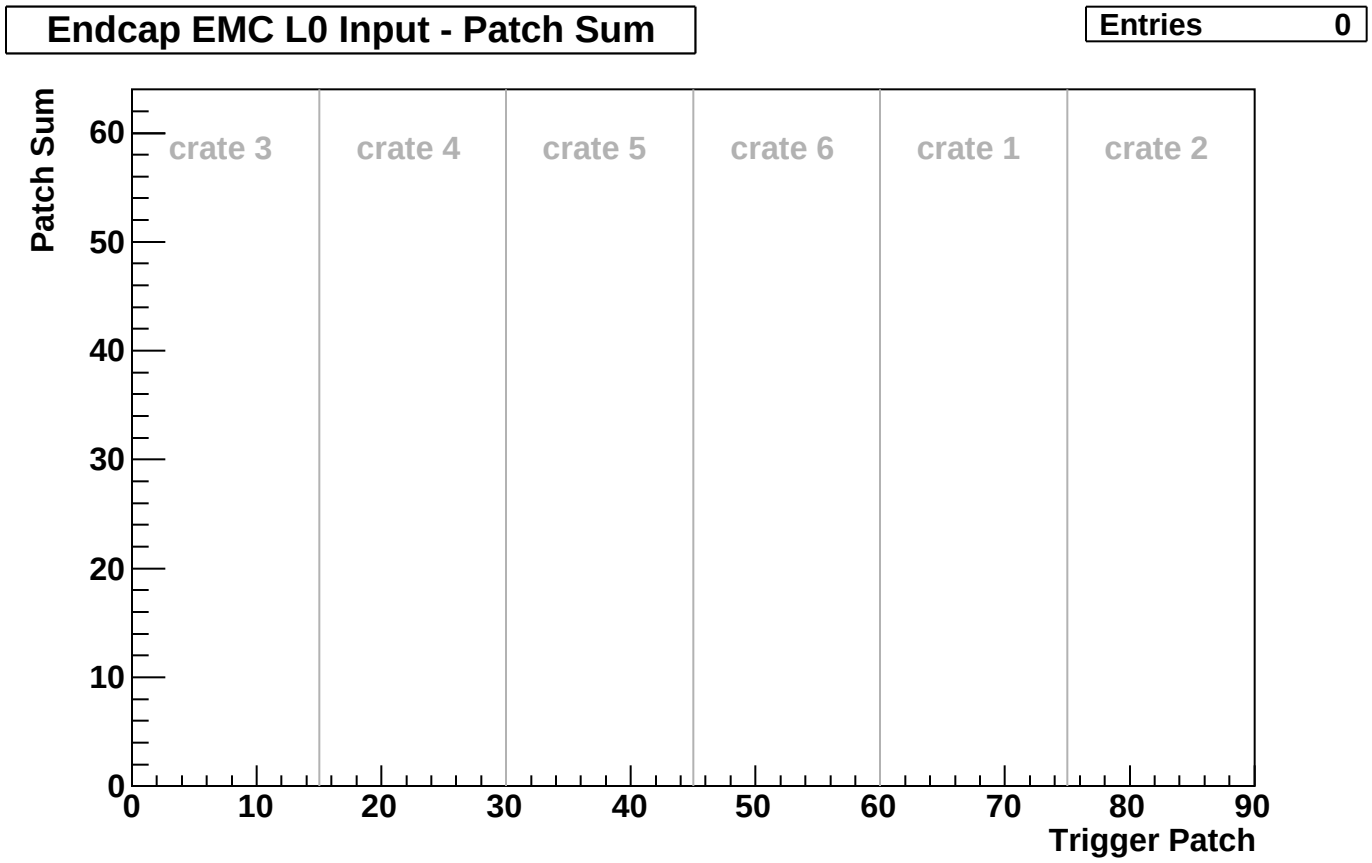

TCU bits
Entries 0
TCU bits
1
0
BIT1 BIT2 BHT-0 BHT-1 VPDMB EHT2 JP1 BBCMBLive-pre VPDMBLive-pre ZDCMB-pre ZDCpol MTD FMSfast FMSslow FMSled-FPE Zerobias

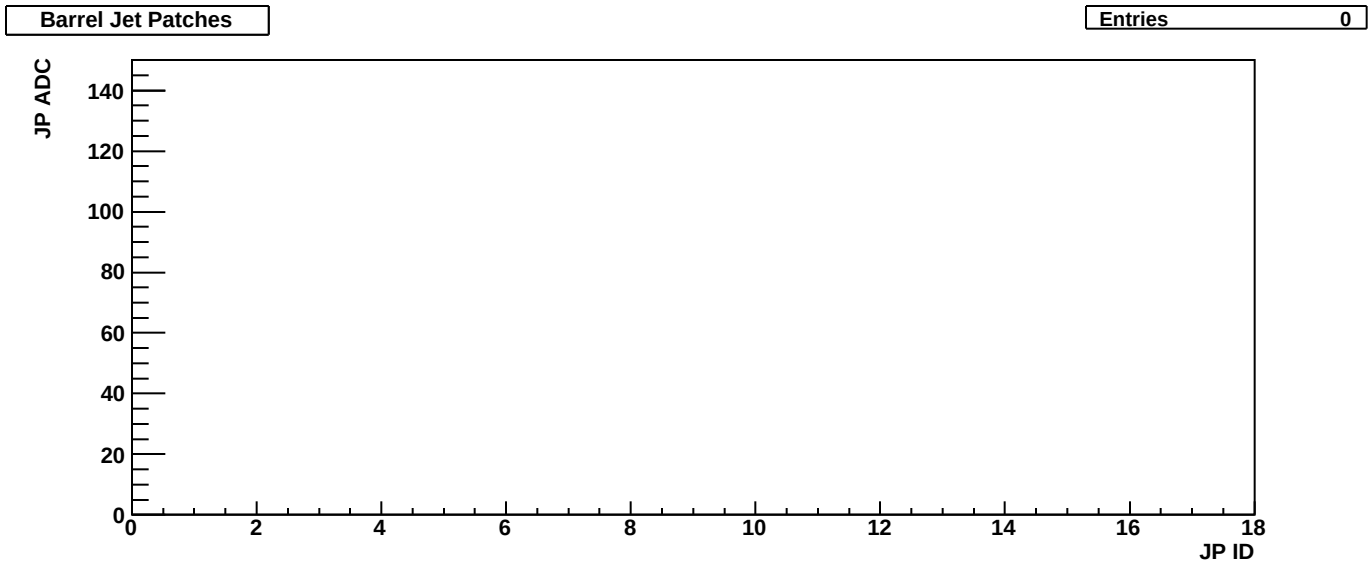

TCU bits
Entries 0
TCU bits - Simulated
1
0
-1
-2
BIT1 BIT2 BHT-0 BHT-1 VPDMB EHT2 JP1 BBCMBLive-pre VPDMBLive-pre ZDCMB-pre ZDCpol MTD FMSfast FMSslow FMSled-FPE Zerobias

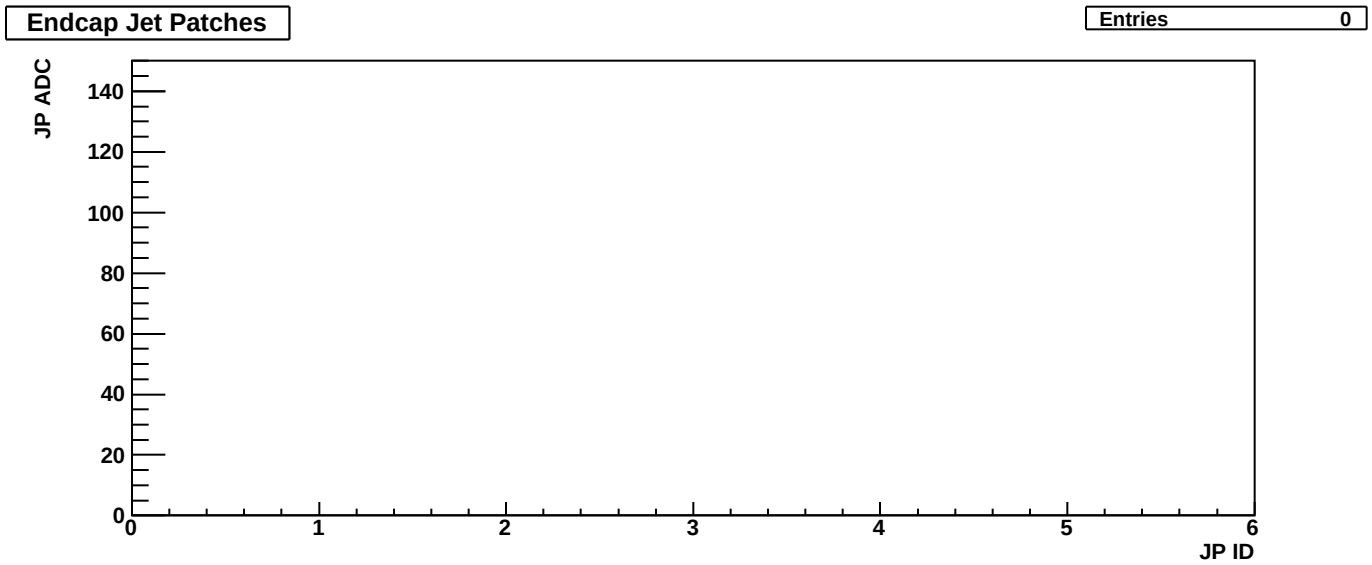

Barrel EMC L0 Input - High Tower
Entries 0
High Tower
0
10
20
30
40
50
60
0
50
100
150
200
250
300
Trigger Patch

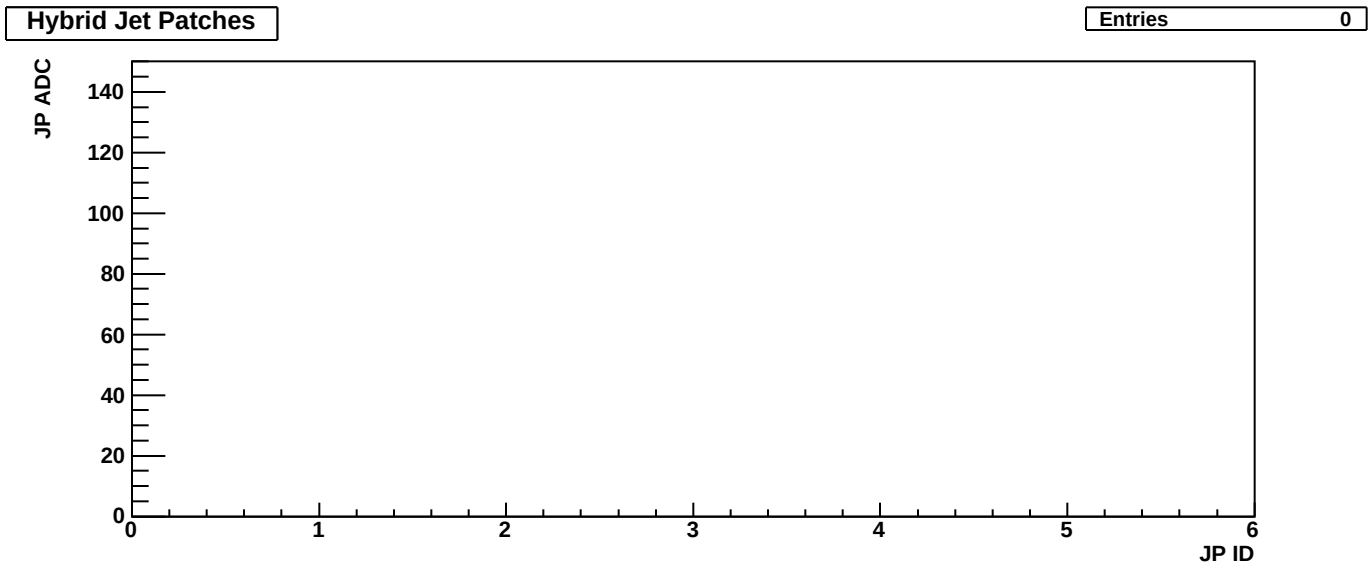

Barrel EMC L0 Input - Patch Sum
Entries 0
Patch Sum
0
10
20
30
40
50
60
0
50
100
150
200
250
300
Trigger Patch


Endcap EMC L0 Input - High Tower
Entries 0
High Tower
crate 3
crate 4
crate 5
crate 6
crate 1
crate 2
0
10
20
30
40
50
60
70
80
90
Trigger Patch


Endcap EMC L0 Input - Patch Sum
Entries 0
Patch Sum
crate 3
crate 4
crate 5
crate 6
crate 1
crate 2
0
10
20
30
40
50
60
70
80
90
Trigger Patch

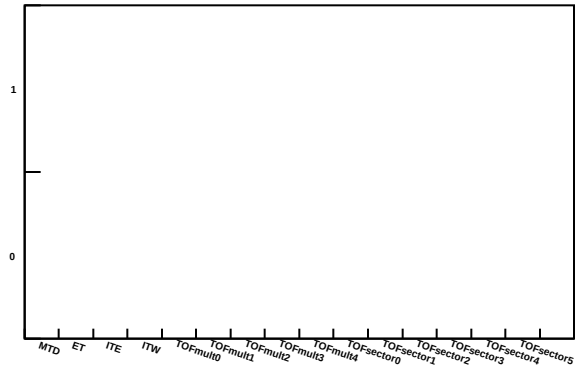

Barrel Jet Patches
Entries 0
JP ADC
0
20
40
60
80
100
120
140
0
2
4
6
8
10
12
14
16
18
JP ID


Endcap Jet Patches
Entries 0
JP ADC
0
20
40
60
80
100
120
140
0
1
2
3
4
5
6
JP ID


Hybrid Jet Patches
Entries 0
JP ADC
0
20
40
60
80
100
120
140
0
1
2
3
4
5
6
JP ID

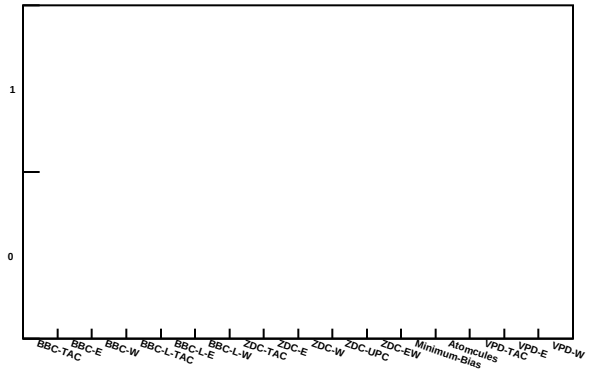
TF201 0-15 (ch0)

Entries 0



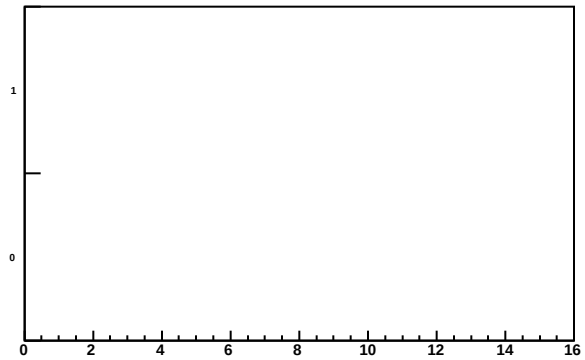
VT201 0-15 (ch1)

Entries 0



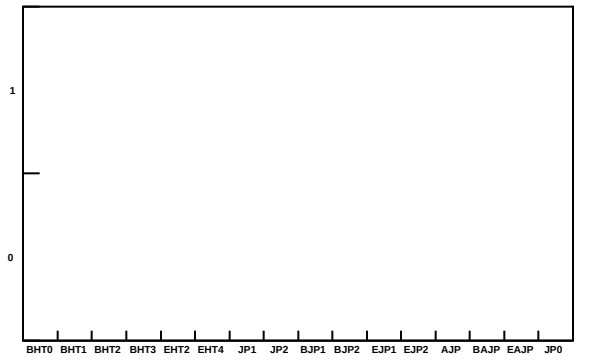
Unused (ch2)

Entries 0



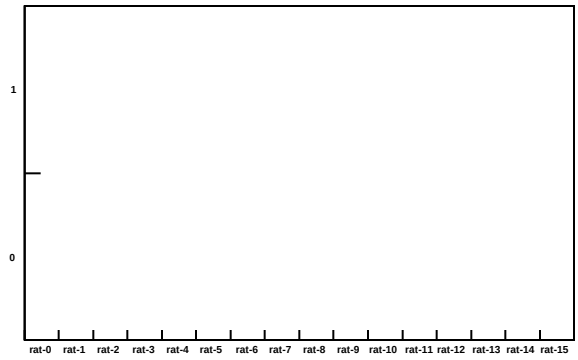
EM201 0-15 (ch3)

Entries 0



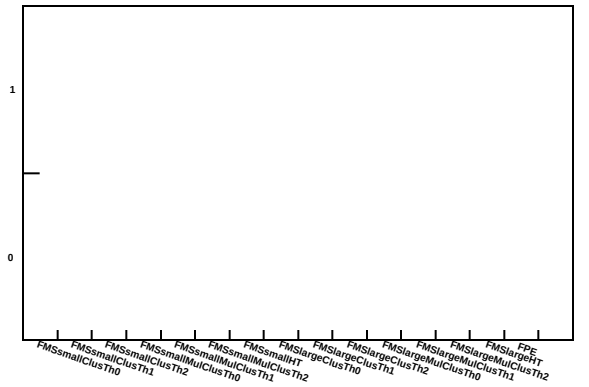
RAT board (ch4)

Entries 0



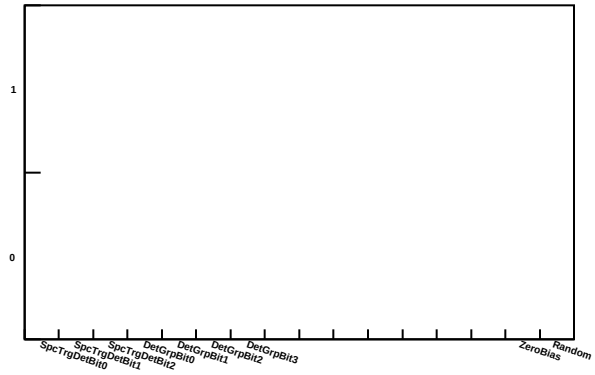
FP201 0-15 (ch5)

Entries 0



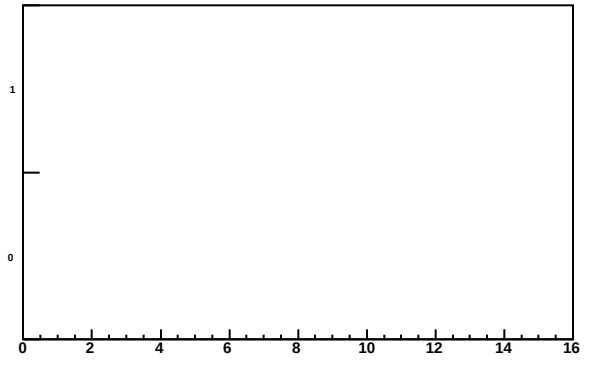
ST201 0-15 (ch6)

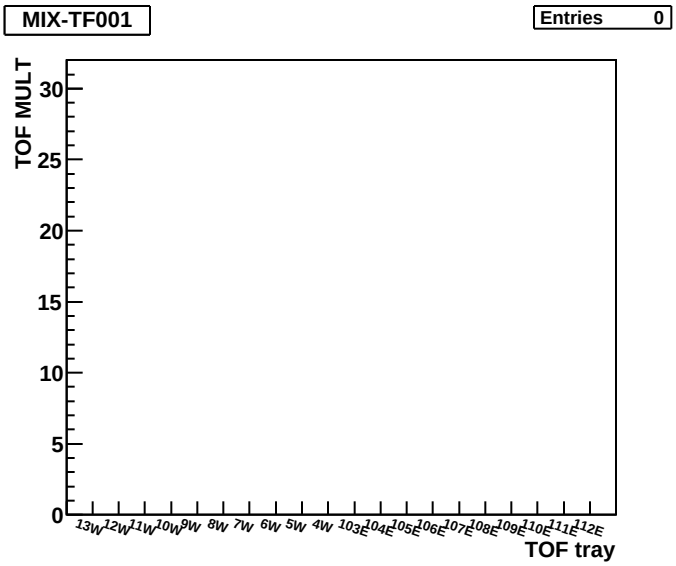
Entries 0

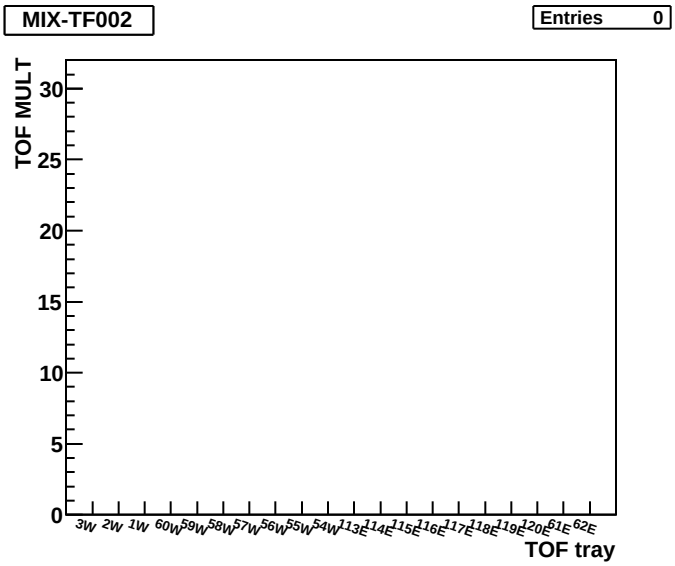


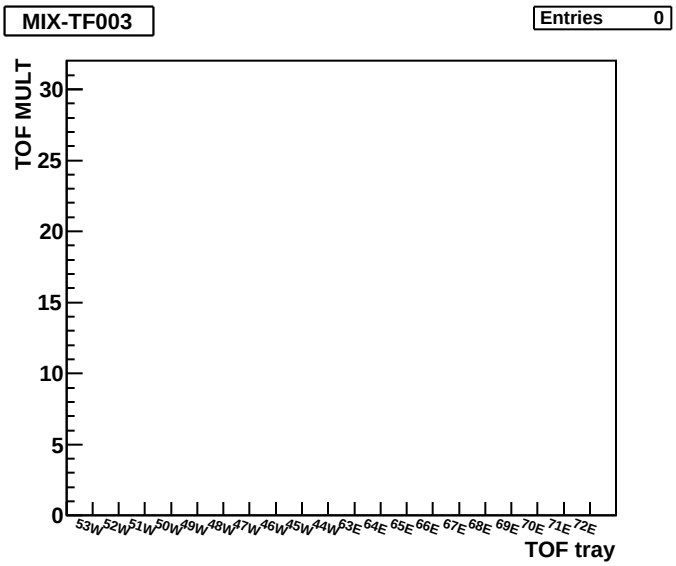
Unused (ch7)

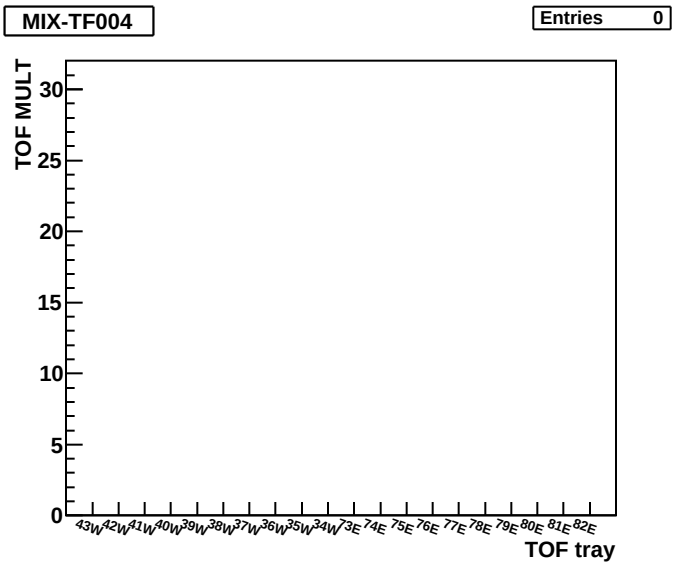
Entries 0

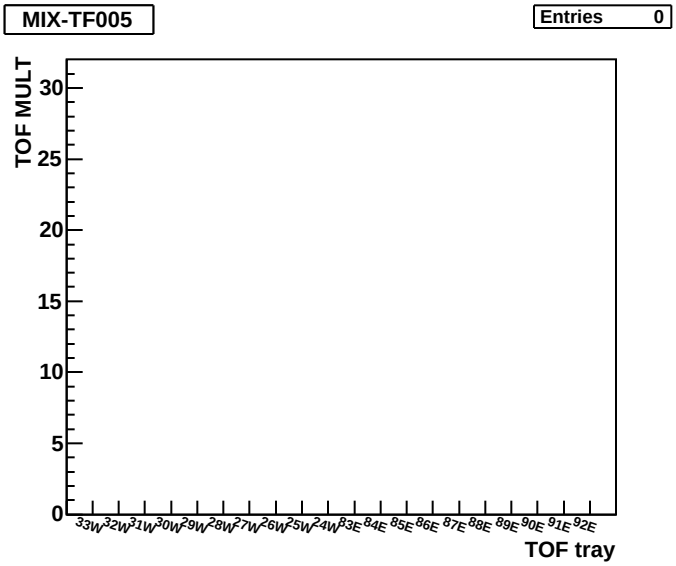


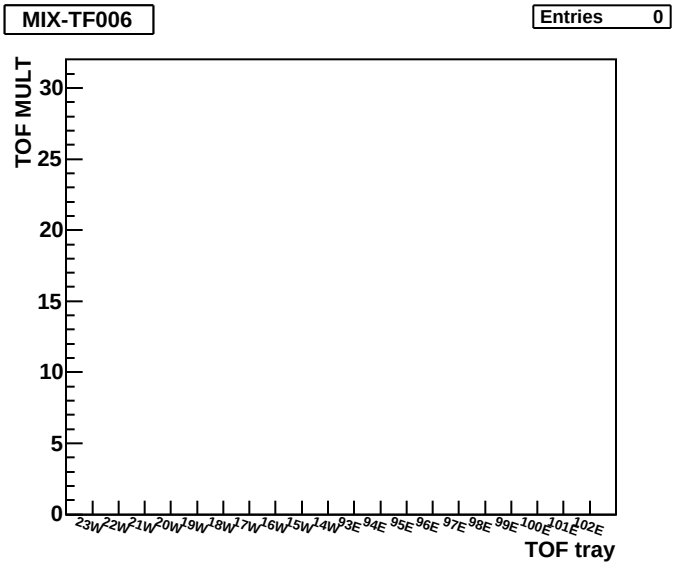

MIX-TF001
Entries 0
TOF MULT
0 5 10 15 20 25 30
13W 12W 11W 10W 9W 8W 7W 6W 5W 4W 103E 104E 105E 106E 107E 108E 109E 110E 111E 112E
TOF tray

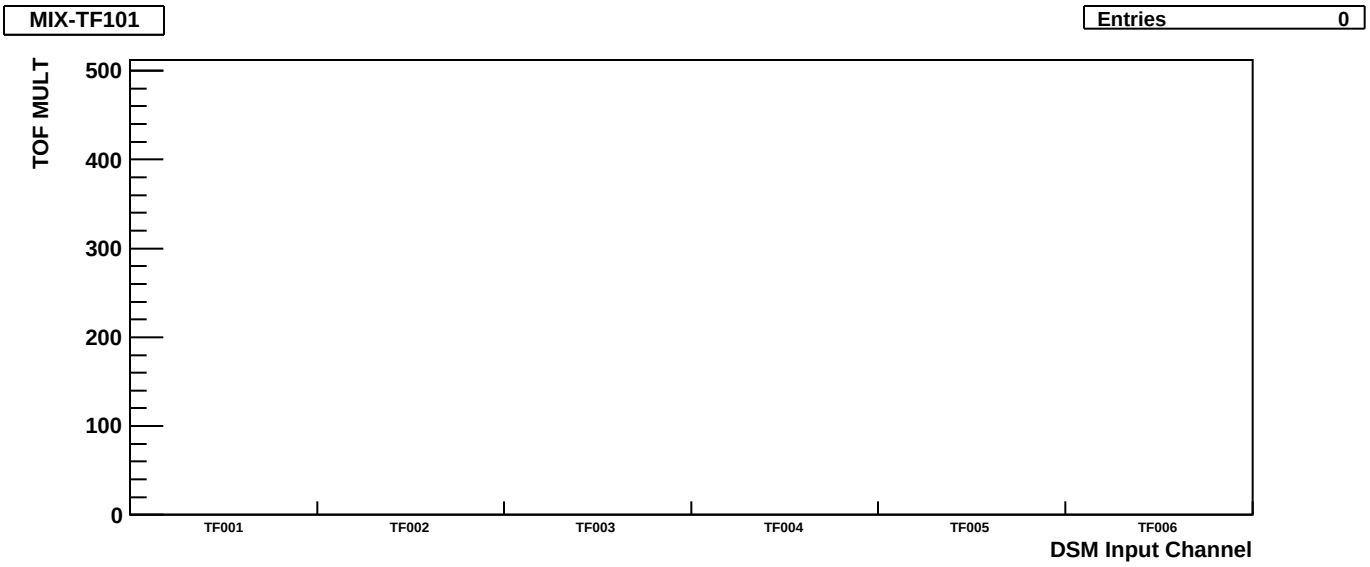

MIX-TF002
Entries 0
TOF MULT
0 5 10 15 20 25 30
3W 2W 1W 60W 59W 58W 57W 56W 55W 54W 113E 114E 115E 116E 117E 118E 119E 120E 61E 62E
TOF tray

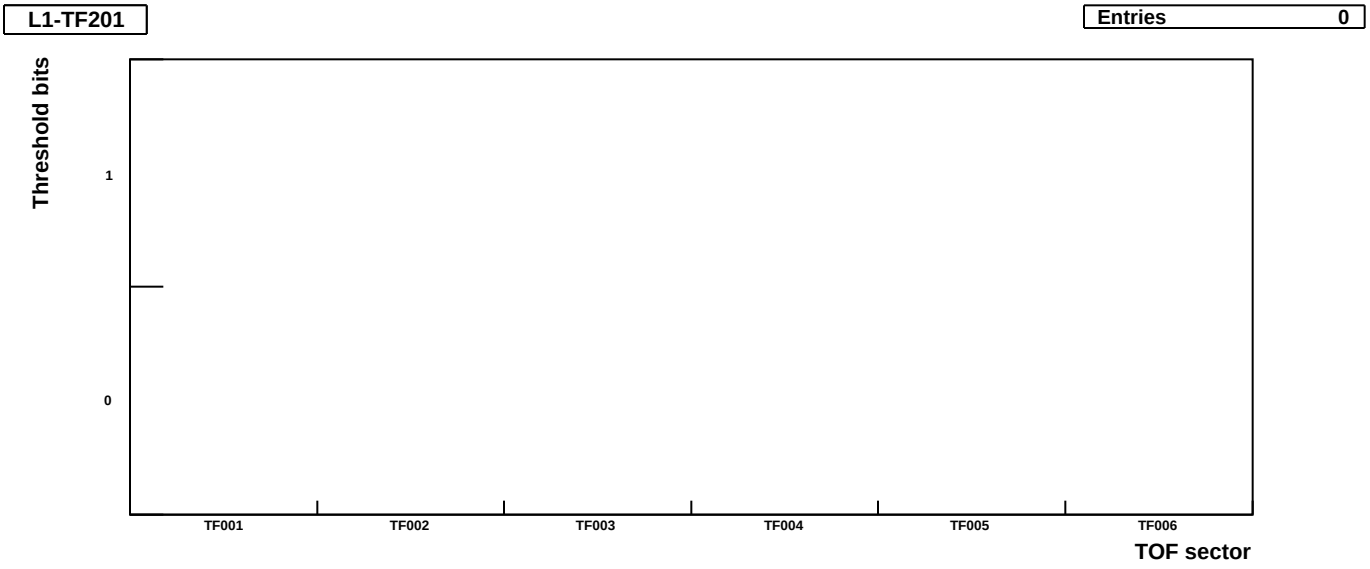

MIX-TF003
Entries 0
TOF MULT
0 5 10 15 20 25 30
53W 52W 51W 50W 49W 48W 47W 46W 45W 44W 63E 64E 65E 66E 67E 68E 69E 70E 71E 72E
TOF tray

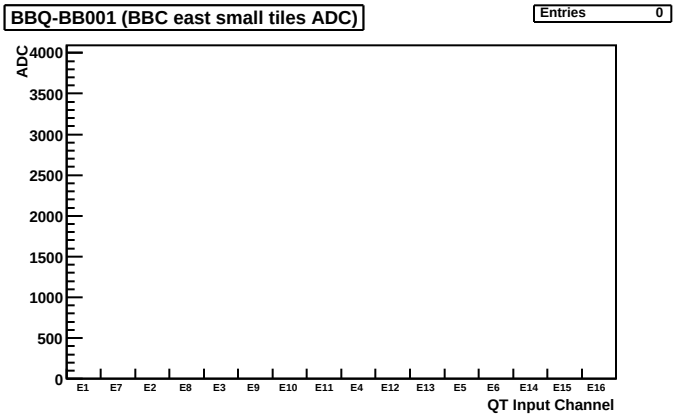

MIX-TF004
Entries 0
TOF MULT
0 5 10 15 20 25 30
43W 42W 41W 40W 39W 38W 37W 36W 35W 34W 73E 74E 75E 76E 77E 78E 79E 80E 81E 82E
TOF tray

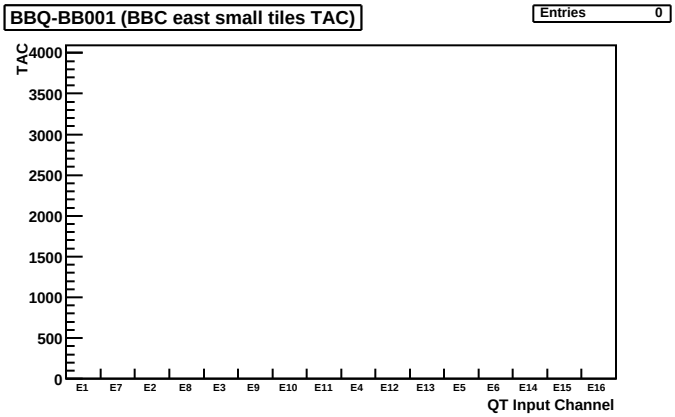

MIX-TF005
Entries 0
TOF MULT
0 5 10 15 20 25 30
33W 32W 31W 30W 29W 28W 27W 26W 25W 24W 83E 84E 85E 86E 87E 88E 89E 90E 91E 92E
TOF tray

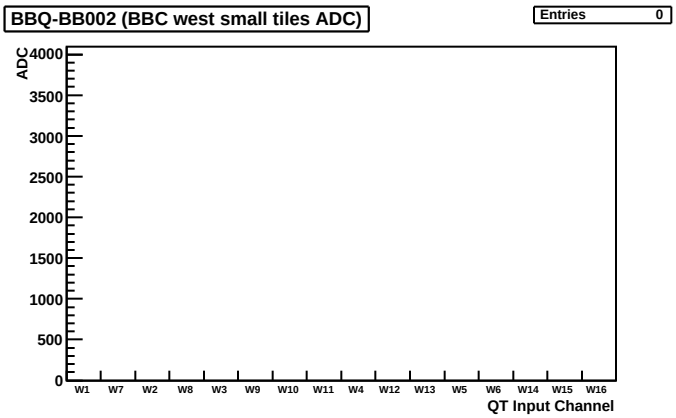

MIX-TF006
Entries 0
TOF MULT
0 5 10 15 20 25 30
23W 22W 21W 20W 19W 18W 17W 16W 15W 14W 93E 94E 95E 96E 97E 98E 99E 100E 101E 102E
TOF tray

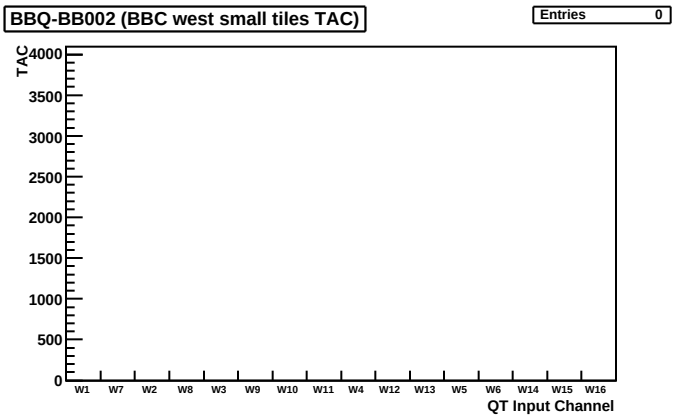

MIX-TF101
Entries 0
TOF MULT
500
400
300
200
100
0
TF001
TF002
TF003
TF004
TF005
TF006
DSM Input Channel

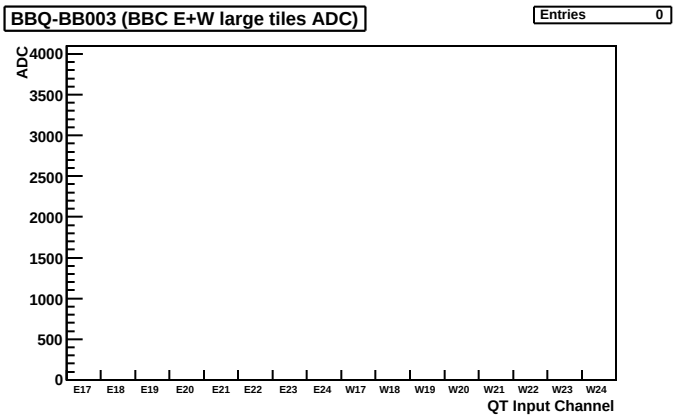

L1-TF201
Entries 0
Threshold bits
1
0
TF001
TF002
TF003
TF004
TF005
TF006
TOF sector

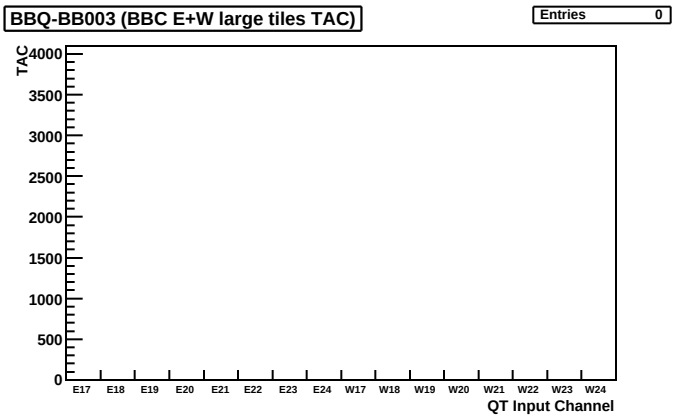

BBQ-BB001 (BBC east small tiles ADC)
Entries 0
ADC
4000
3500
3000
2500
2000
1500
1000
500
0
E1 E7 E2 E8 E3 E9 E10 E11 E4 E12 E13 E5 E6 E14 E15 E16
QT Input Channel

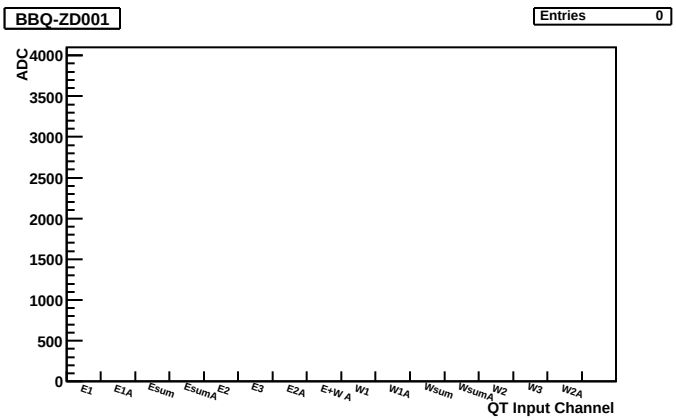

BBQ-BB001 (BBC east small tiles TAC)
Entries 0
TAC
4000
3500
3000
2500
2000
1500
1000
500
0
E1 E7 E2 E8 E3 E9 E10 E11 E4 E12 E13 E5 E6 E14 E15 E16
QT Input Channel

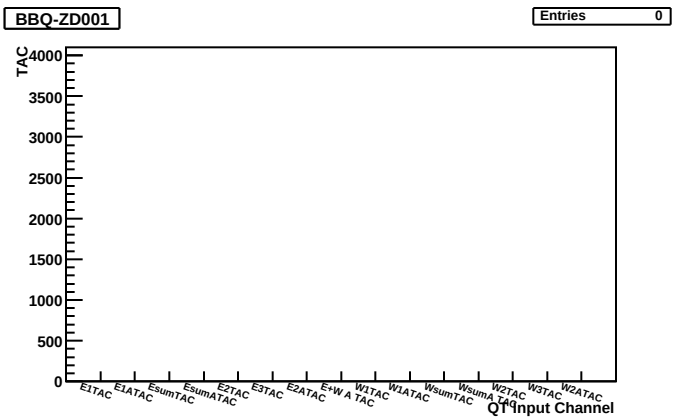

BBQ-BB002 (BBC west small tiles ADC)
Entries 0
ADC
4000
3500
3000
2500
2000
1500
1000
500
0
W1 W7 W2 W8 W3 W9 W10 W11 W4 W12 W13 W5 W6 W14 W15 W16
QT Input Channel

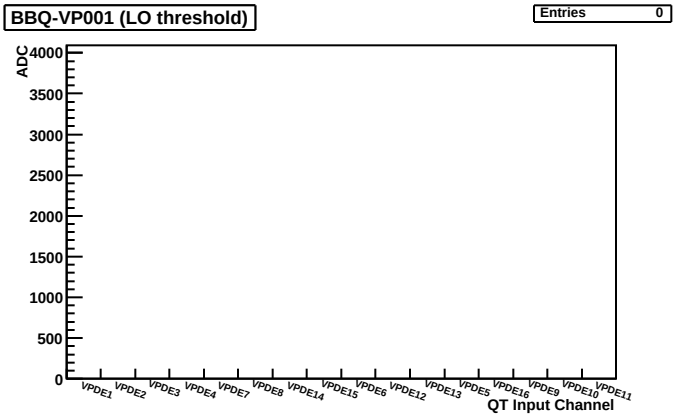

BBQ-BB002 (BBC west small tiles TAC)
Entries 0
TAC
4000
3500
3000
2500
2000
1500
1000
500
0
W1 W7 W2 W8 W3 W9 W10 W11 W4 W12 W13 W5 W6 W14 W15 W16
QT Input Channel

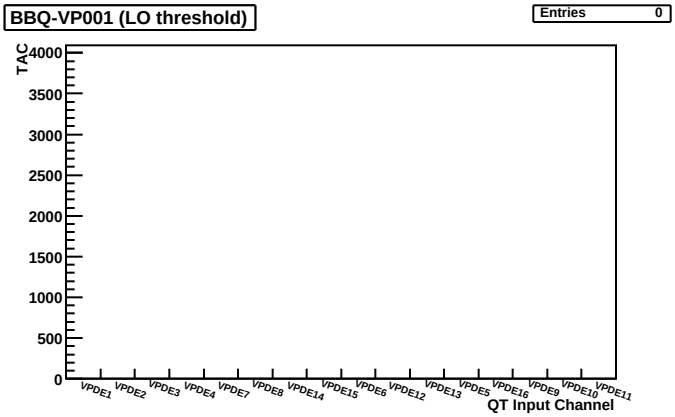

BBQ-BB003 (BBC E+W large tiles ADC)
Entries 0
ADC
4000
3500
3000
2500
2000
1500
1000
500
0
E17 E18 E19 E20 E21 E22 E23 E24 W17 W18 W19 W20 W21 W22 W23 W24
QT Input Channel

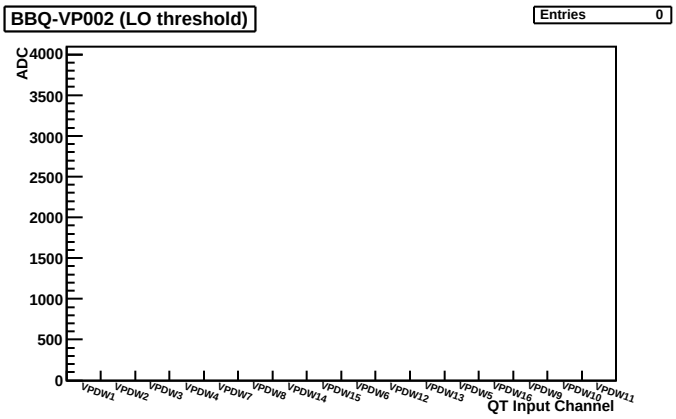

BBQ-BB003 (BBC E+W large tiles TAC)
Entries 0
TAC
4000
3500
3000
2500
2000
1500
1000
500
0
E17 E18 E19 E20 E21 E22 E23 E24 W17 W18 W19 W20 W21 W22 W23 W24
QT Input Channel

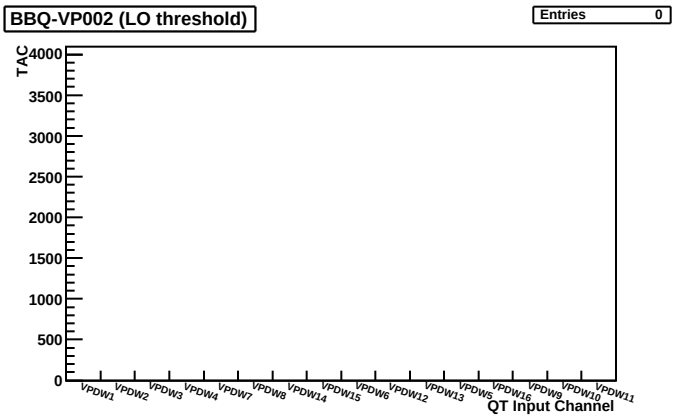

BBQ-ZD001
Entries 0
ADC
4000
3500
3000
2500
2000
1500
1000
500
0
E1 E1A Esum EsumA E2 E3 E2A E+W A W1 W1A Wsum WsumA W2 W3 W2A
QT Input Channel

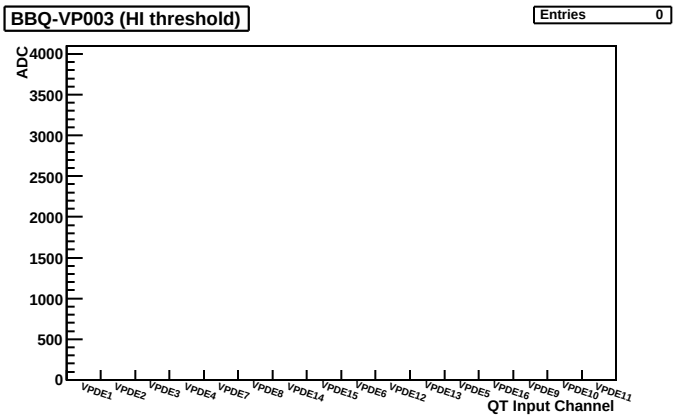

BBQ-ZD001
Entries 0
TAC
4000
3500
3000
2500
2000
1500
1000
500
0
E1TAC E1ATAC EsumTAC EsumATAC E2TAC E3TAC E2ATAC E+W A TAC W1TAC W1ATAC WsumTAC WsumA TAC W2TAC W3TAC W2ATAC
QT Input Channel

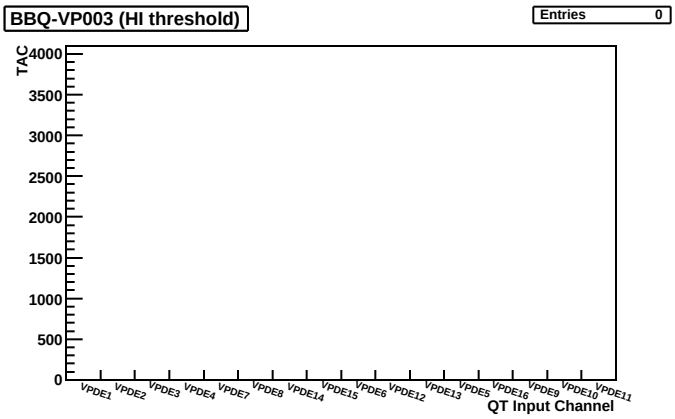

BBQ-VP001 (LO threshold)
Entries 0
ADC
4000
3500
3000
2500
2000
1500
1000
500
0
VPDE1 VPDE2 VPDE3 VPDE4 VPDE7 VPDE8 VPDE14 VPDE15 VPDE6 VPDE12 VPDE13 VPDE5 VPDE16 VPDE9 VPDE10 VPDE11
QT Input Channel

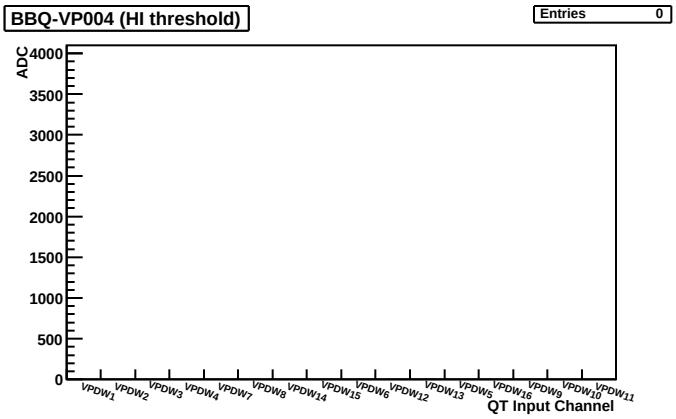

BBQ-VP001 (LO threshold)
Entries 0
TAC
4000
3500
3000
2500
2000
1500
1000
500
0
VPDE1 VPDE2 VPDE3 VPDE4 VPDE7 VPDE8 VPDE14 VPDE15 VPDE6 VPDE12 VPDE13 VPDE5 VPDE16 VPDE9 VPDE10 VPDE11
QT Input Channel

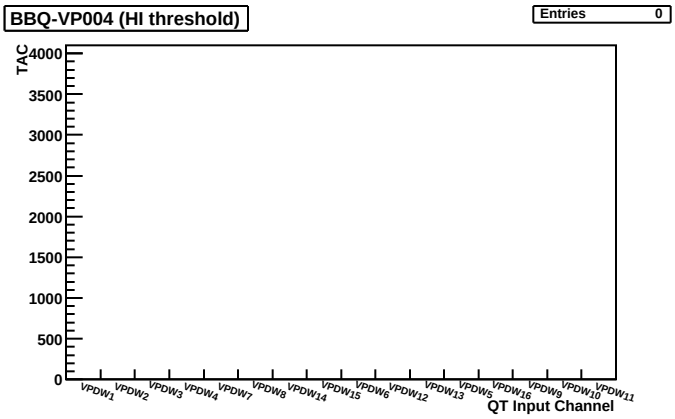

BBQ-VP002 (LO threshold)
Entries 0
ADC
4000
3500
3000
2500
2000
1500
1000
500
0
VPDW1 VPDW2 VPDW3 VPDW4 VPDW7 VPDW8 VPDW14 VPDW15 VPDW6 VPDW12 VPDW13 VPDW5 VPDW16 VPDW9 VPDW10 VPDW11
QT Input Channel

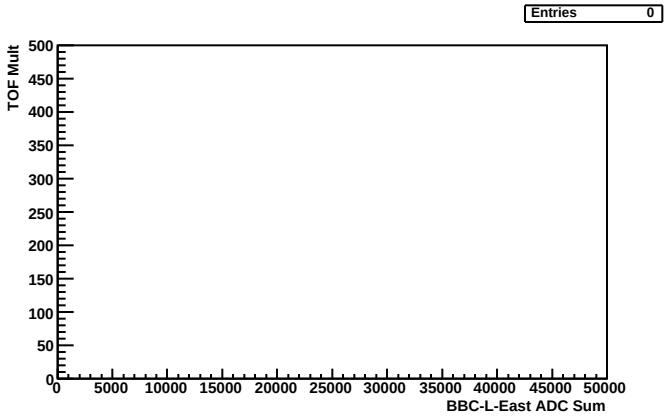

BBQ-VP002 (LO threshold)
Entries 0
TAC
4000
3500
3000
2500
2000
1500
1000
500
0
VPDW1 VPDW2 VPDW3 VPDW4 VPDW7 VPDW8 VPDW14 VPDW15 VPDW6 VPDW12 VPDW13 VPDW5 VPDW16 VPDW9 VPDW10 VPDW11
QT Input Channel

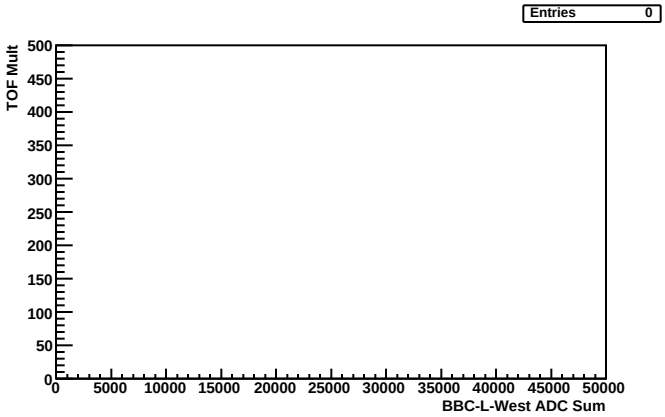

BBQ-VP003 (HI threshold)
Entries 0
ADC
4000
3500
3000
2500
2000
1500
1000
500
0
VPDE1 VPDE2 VPDE3 VPDE4 VPDE7 VPDE8 VPDE14 VPDE15 VPDE6 VPDE12 VPDE13 VPDE5 VPDE16 VPDE9 VPDE10 VPDE11
QT Input Channel

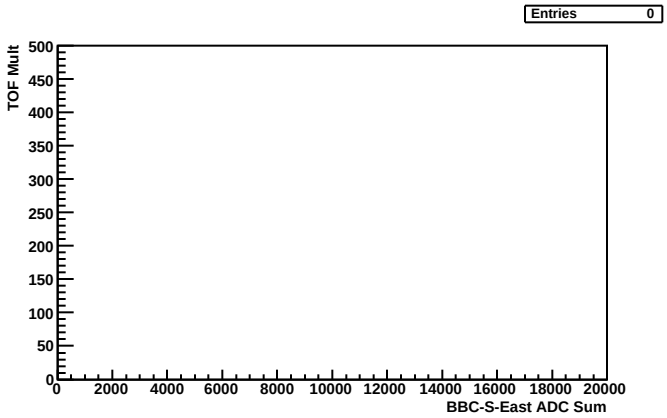

BBQ-VP003 (HI threshold)
Entries 0
TAC
4000
3500
3000
2500
2000
1500
1000
500
0
VPDE1 VPDE2 VPDE3 VPDE4 VPDE7 VPDE8 VPDE14 VPDE15 VPDE6 VPDE12 VPDE13 VPDE5 VPDE16 VPDE9 VPDE10 VPDE11
QT Input Channel

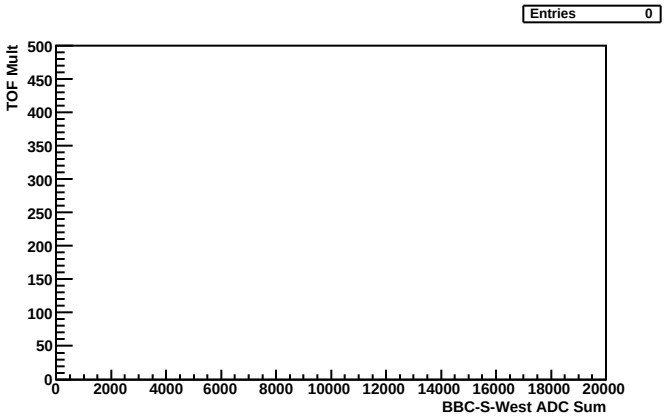

BBQ-VP004 (HI threshold)
Entries 0
ADC
4000
3500
3000
2500
2000
1500
1000
500
0
VPDW1 VPDW2 VPDW3 VPDW4 VPDW7 VPDW8 VPDW14 VPDW15 VPDW6 VPDW12 VPDW13 VPDW5 VPDW16 VPDW9 VPDW10 VPDW11
QT Input Channel

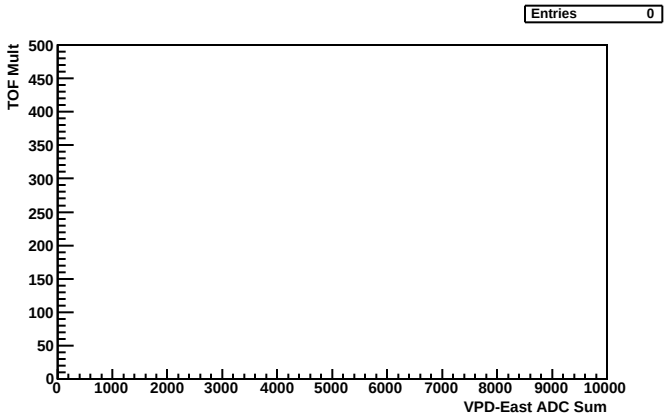

BBQ-VP004 (HI threshold)
Entries 0
TAC
4000
3500
3000
2500
2000
1500
1000
500
0
VPDW1 VPDW2 VPDW3 VPDW4 VPDW7 VPDW8 VPDW14 VPDW15 VPDW6 VPDW12 VPDW13 VPDW5 VPDW16 VPDW9 VPDW10 VPDW11
QT Input Channel

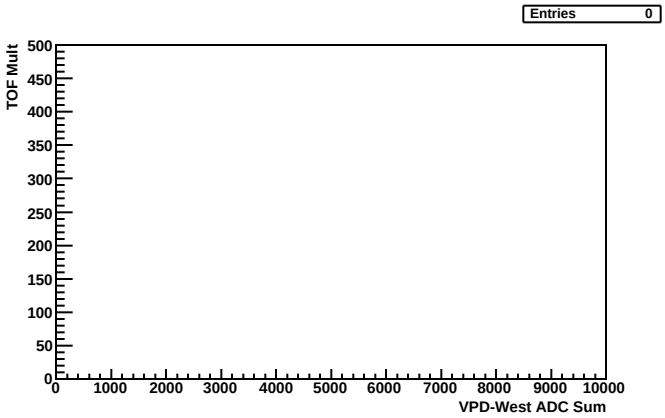

Entries 0
TOF Mult
BBC-L-East ADC Sum

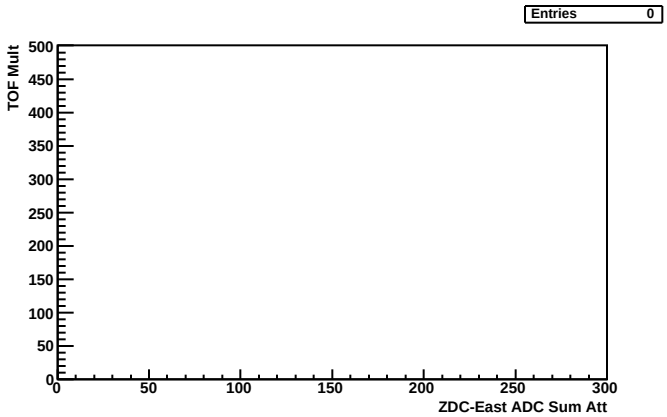

Entries 0
TOF Mult
BBC-L-West ADC Sum

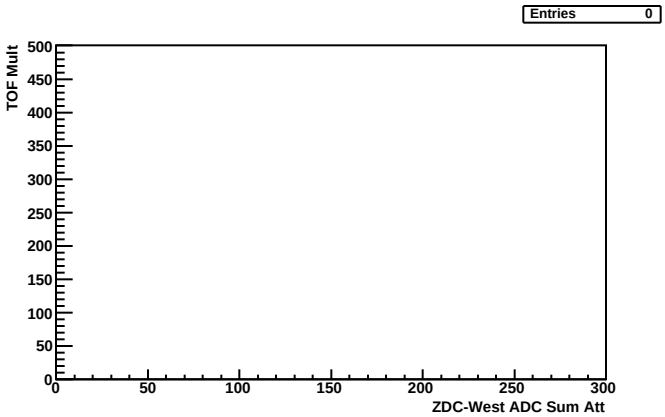

Entries 0
TOF Mult
BBC-S-East ADC Sum

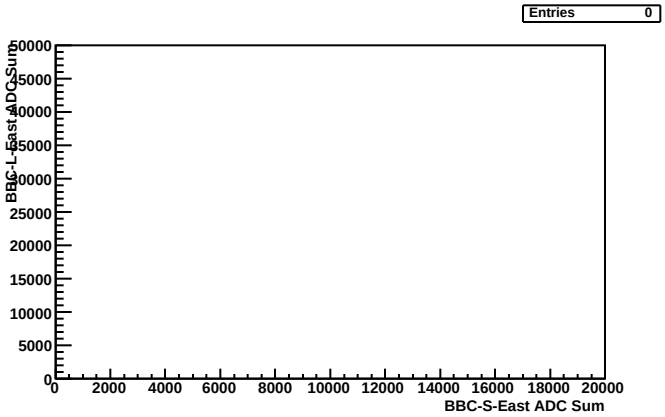

Entries 0
TOF Mult
BBC-S-West ADC Sum

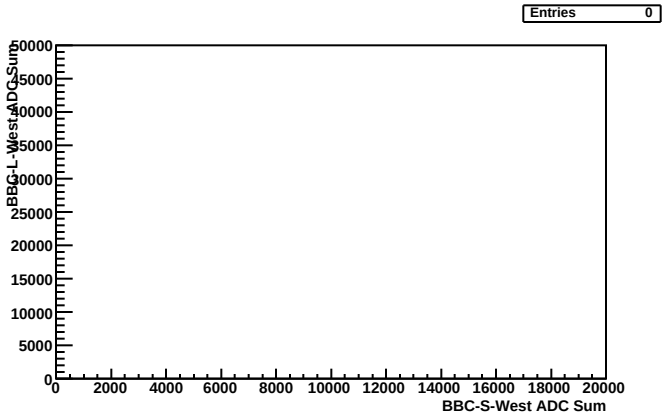

Entries 0
TOF Mult
VPD-East ADC Sum

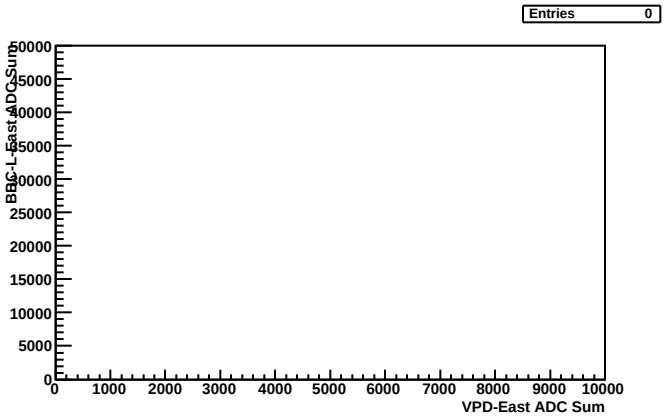

Entries 0
TOF Mult
VPD-West ADC Sum

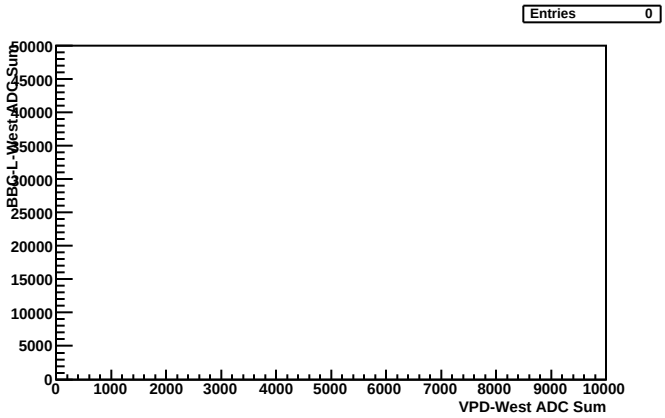

Entries 0
TOF Mult
ZDC-East ADC Sum Att

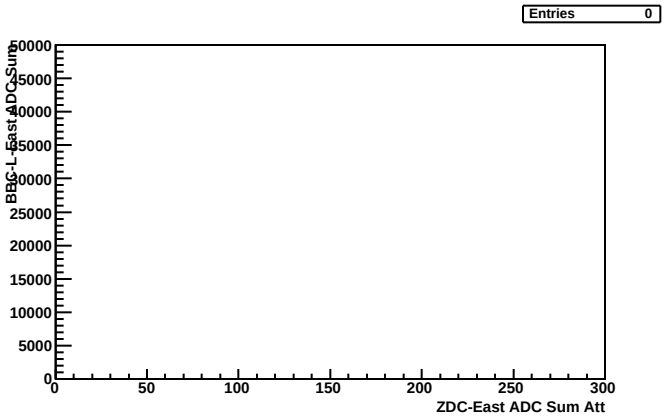

Entries 0
TOF Mult
ZDC-West ADC Sum Att

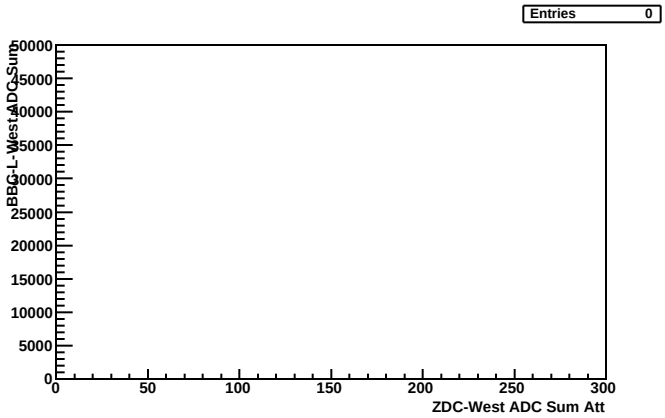

Entries 0
BBC-L-East ADC Sum
BBC-S-East ADC Sum

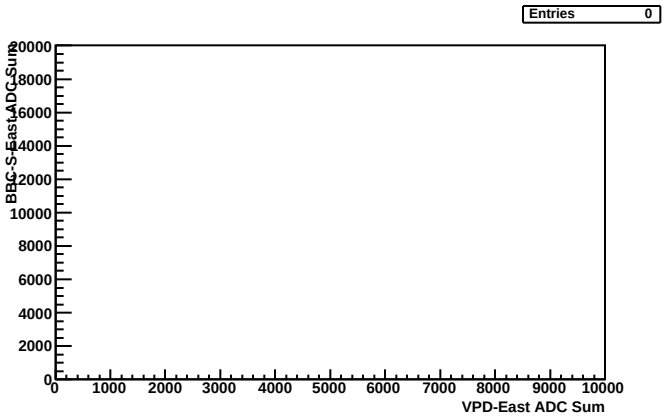

Entries 0
BBC-L-West ADC Sum
BBC-S-West ADC Sum

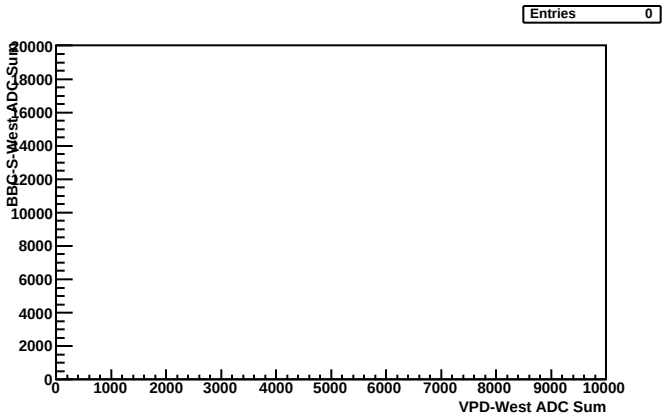

Entries 0
BBC-L-East ADC Sum
VPD-East ADC Sum

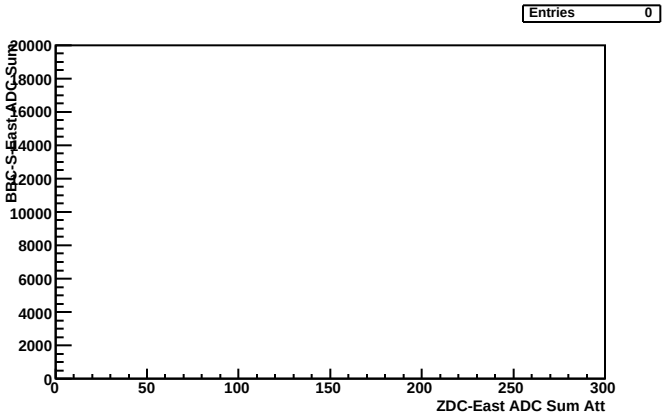

Entries 0
BBC-L-West ADC Sum
VPD-West ADC Sum

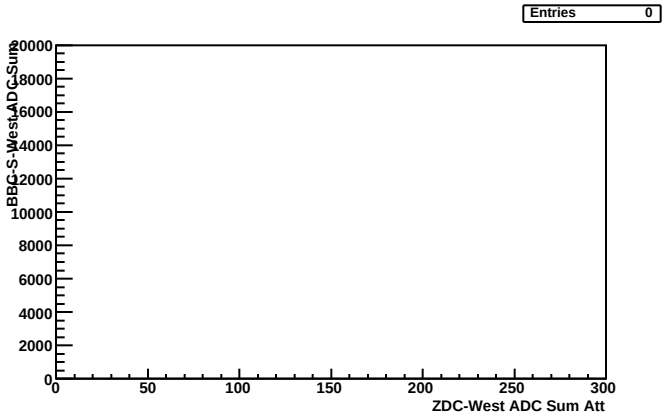

Entries 0
BBC-L-East ADC Sum
ZDC-East ADC Sum Att

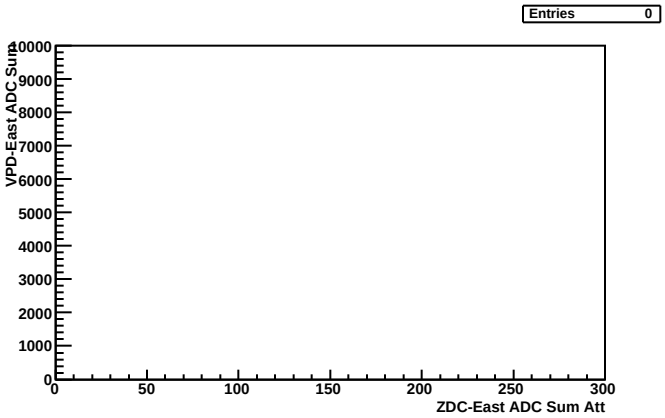

Entries 0
BBC-L-West ADC Sum
ZDC-West ADC Sum Att

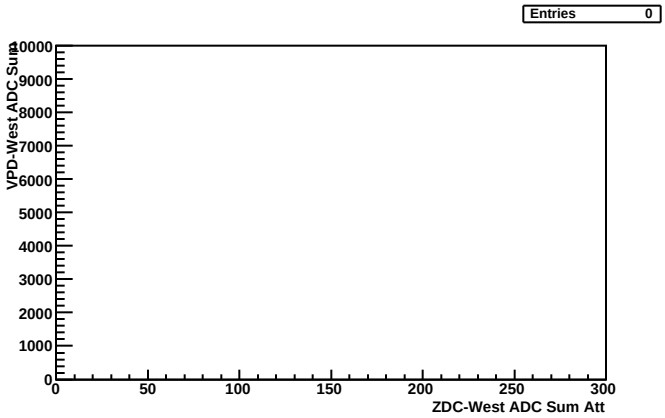

Entries 0
BBC-S-East ADC Sum
VPD-East ADC Sum

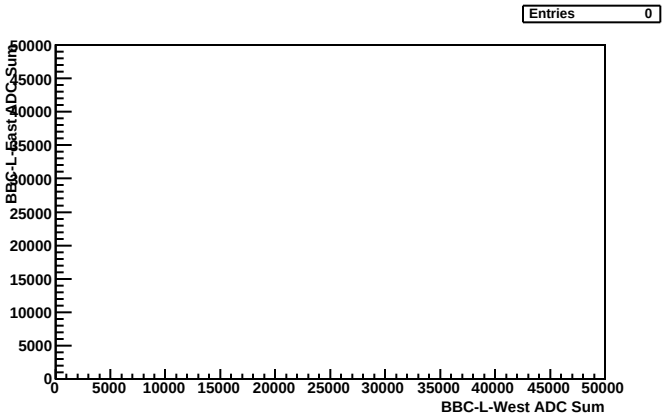

Entries 0
BBC-S-West ADC Sum
VPD-West ADC Sum

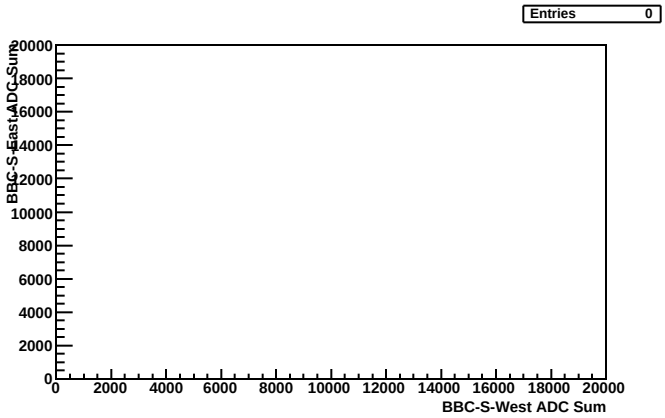

Entries 0
BBC-S-East ADC Sum
ZDC-East ADC Sum Att

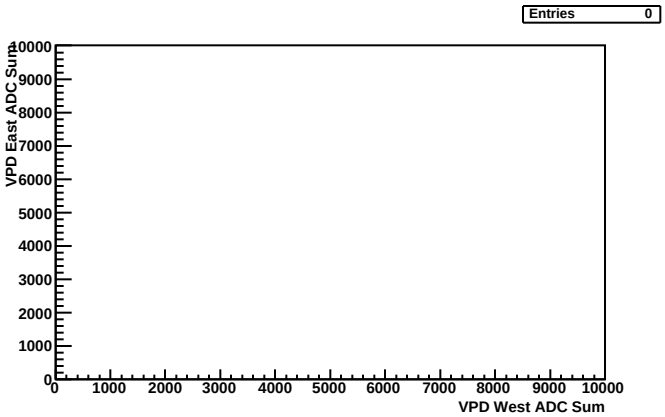

Entries 0
BBC-S-West ADC Sum
ZDC-West ADC Sum Att

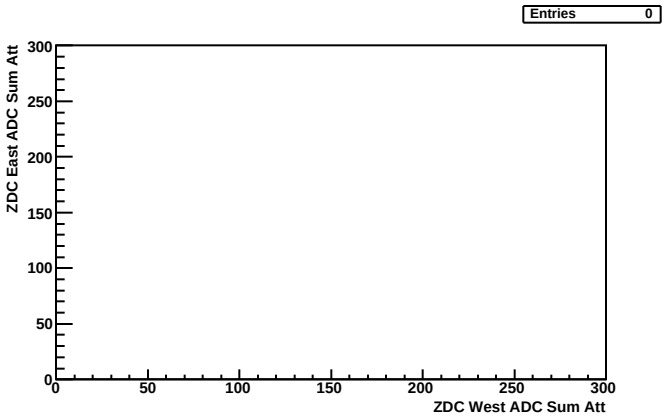

Entries 0
VPD-East ADC Sum
ZDC-East ADC Sum Att

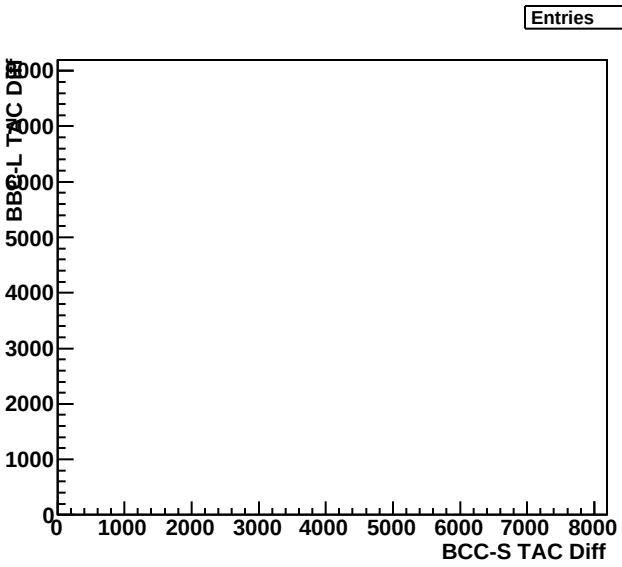

Entries 0
VPD-West ADC Sum
ZDC-West ADC Sum Att

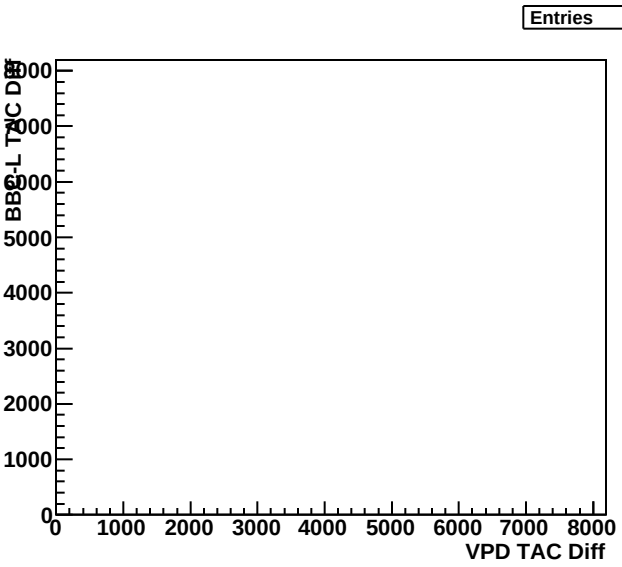

Entries 0
BBC-L-East ADC Sum
BBC-L-West ADC Sum

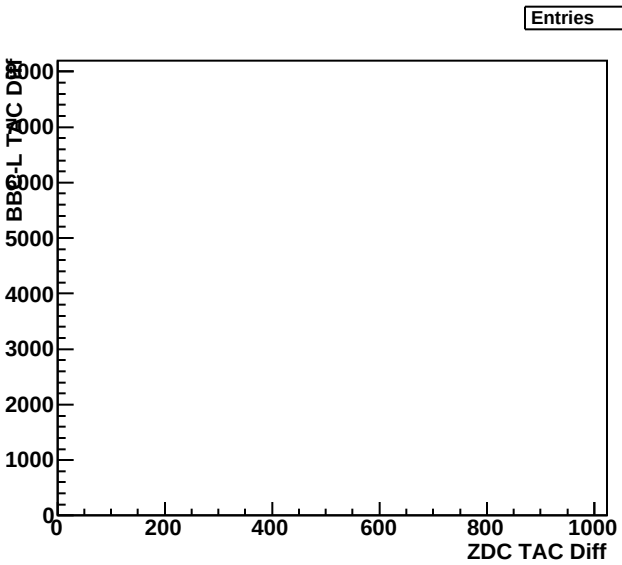

Entries 0
BBC-S-East ADC Sum
BBC-S-West ADC Sum

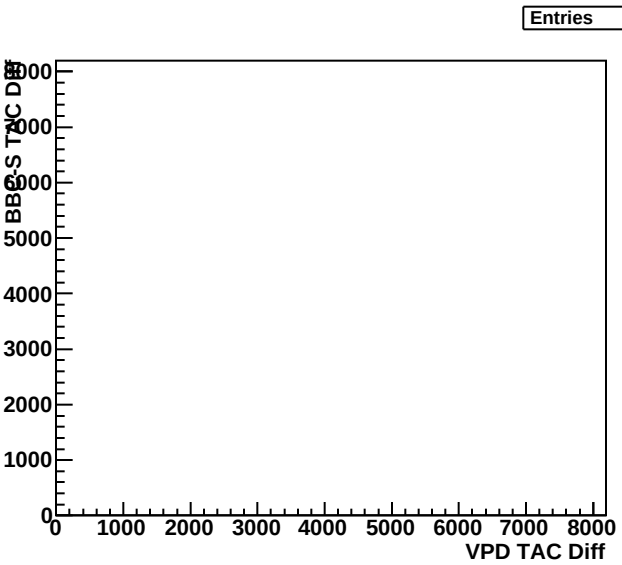

Entries 0
VPD East ADC Sum
VPD West ADC Sum

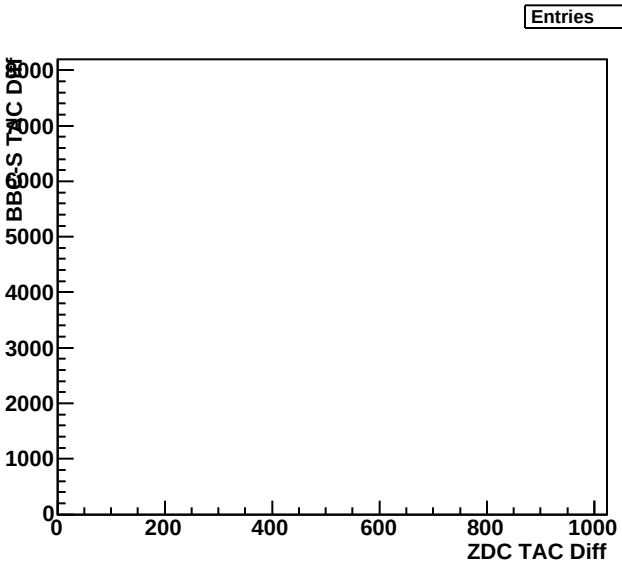

Entries 0
ZDC East ADC Sum Att
ZDC West ADC Sum Att

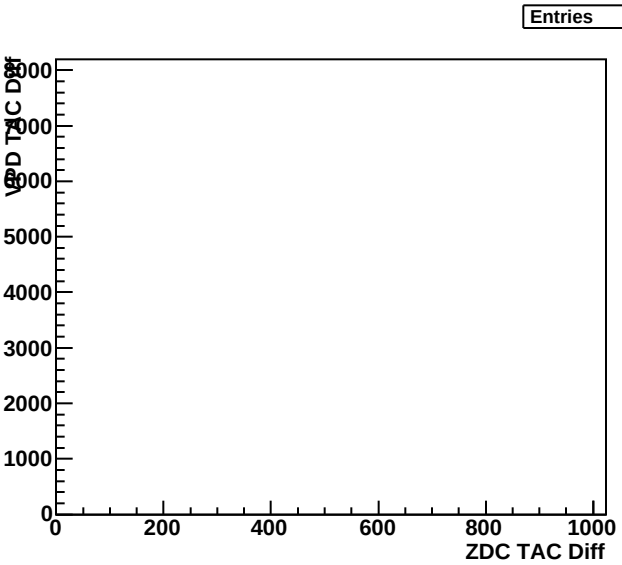

Entries 0
BBC-L TAC Diff
BCC-S TAC Diff

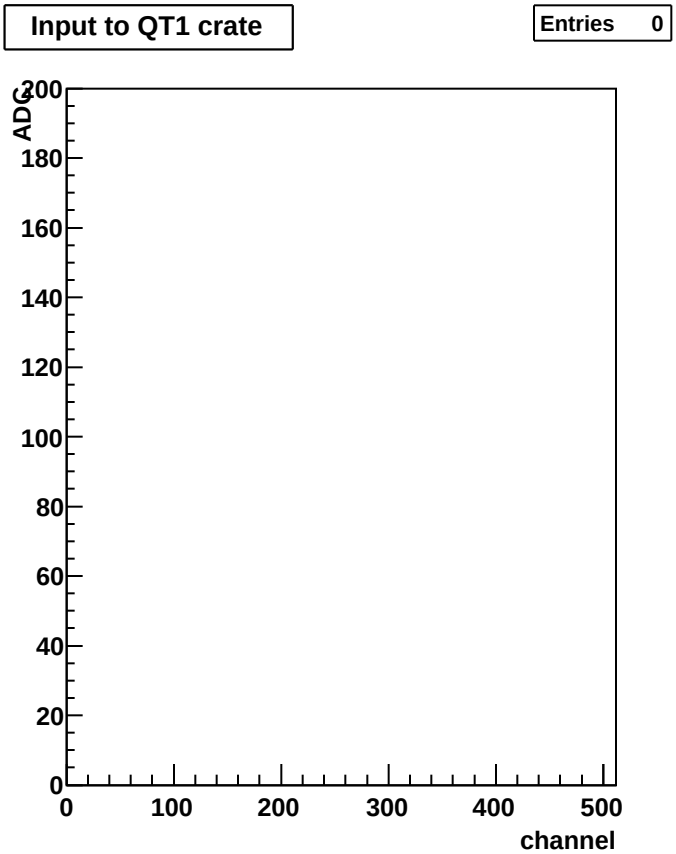

Entries 0
BBC-L TAC Diff
VPD TAC Diff

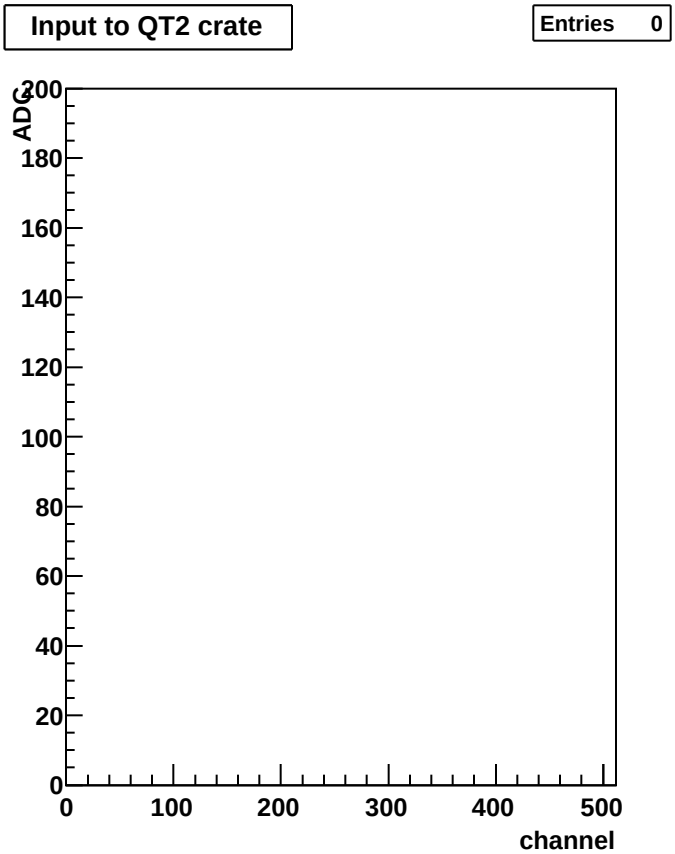

Entries 0
BBC-L TAC Diff
ZDC TAC Diff

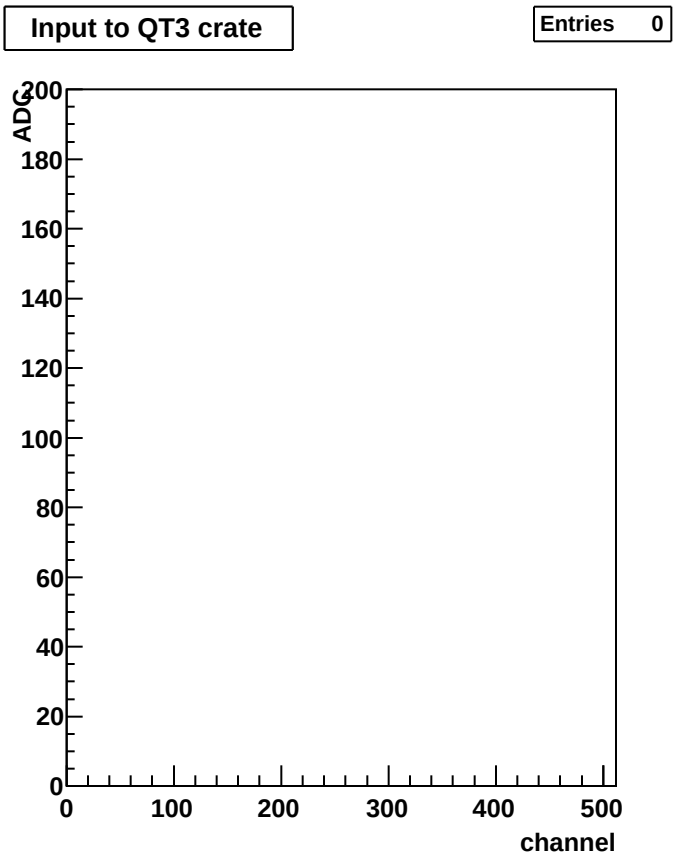

Entries 0
BBC-S TAC Diff
VPD TAC Diff

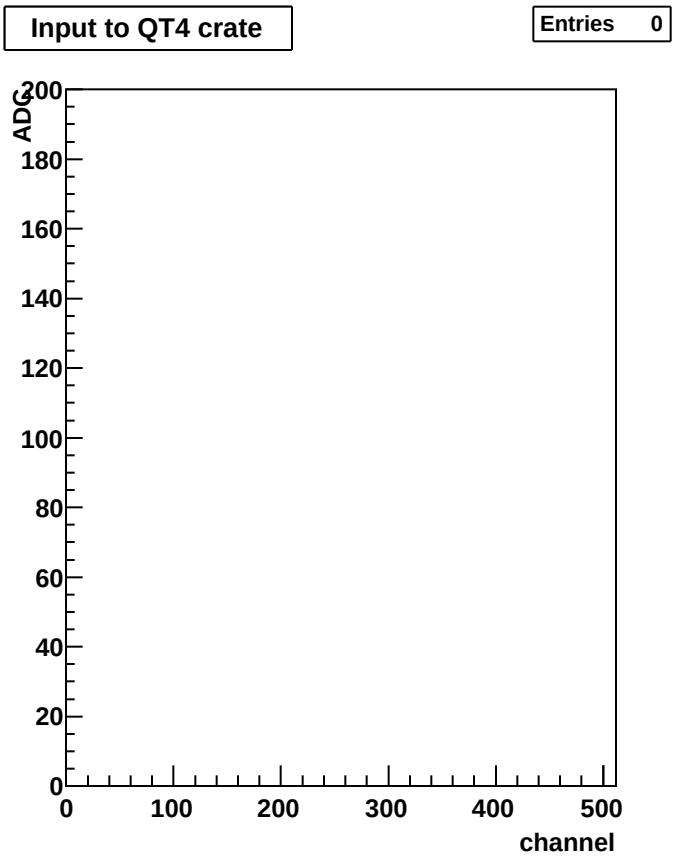

Entries 0
BBC-S TAC Diff
ZDC TAC Diff

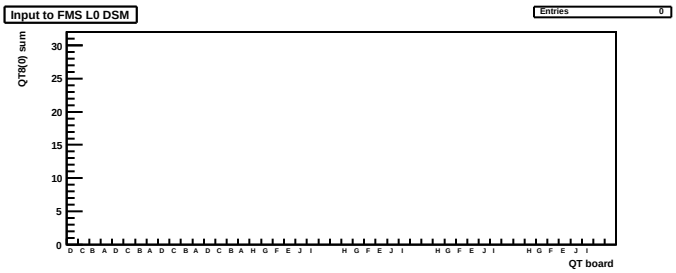

Entries 0
VPD TAC Diff
ZDC TAC Diff

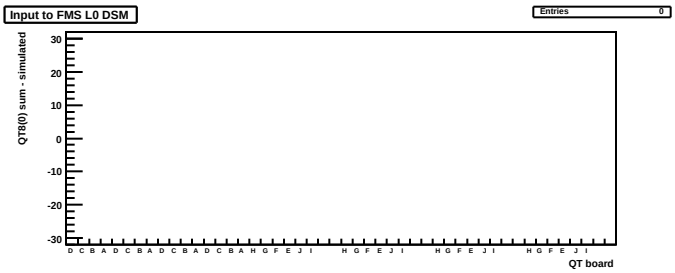

Input to QT1 crate
Entries 0
ADC
200
180
160
140
120
100
80
60
40
20
0
0
100
200
300
400
500
channel

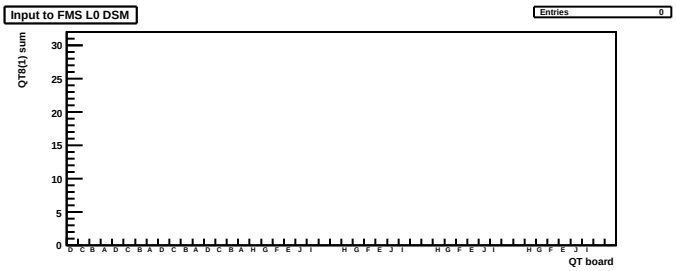

Input to QT2 crate
Entries 0
ADC
200
180
160
140
120
100
80
60
40
20
0
0
100
200
300
400
500
channel

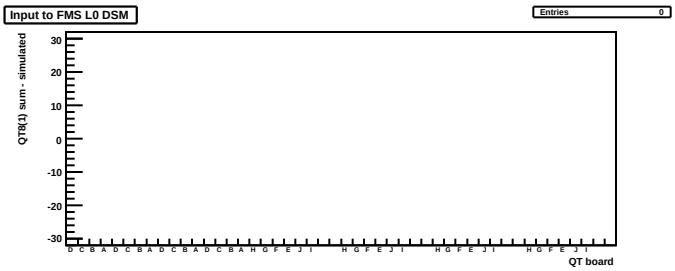

Input to QT3 crate
Entries 0
ADC
200
180
160
140
120
100
80
60
40
20
0
0
100
200
300
400
500
channel

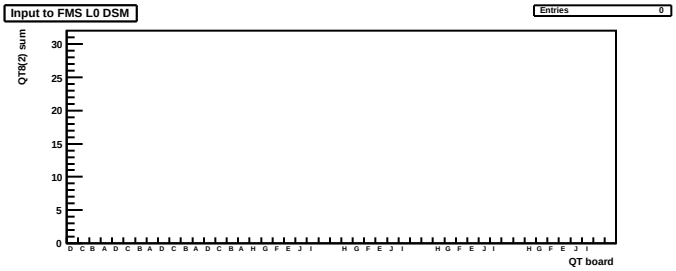

Input to QT4 crate
Entries 0
ADC
200
180
160
140
120
100
80
60
40
20
0
0
100
200
300
400
500
channel

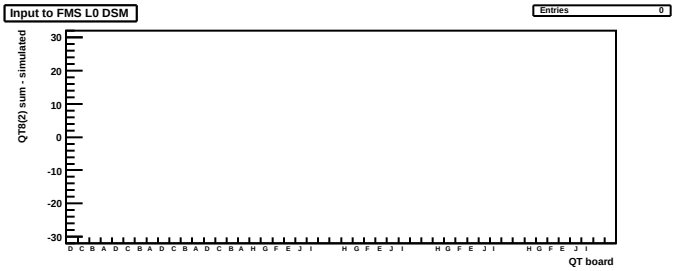

Input to FMS L0 DSM
Entries 0
QT8(0) sum
QT board

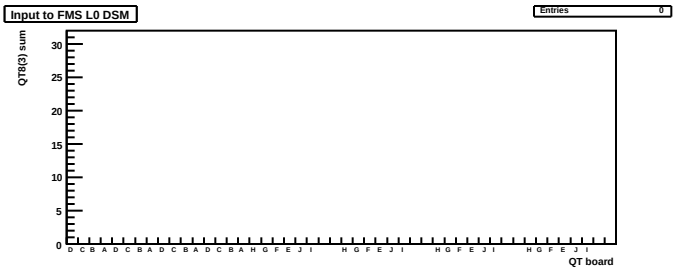

Input to FMS L0 DSM
Entries 0
QT8(0) sum - simulated
QT board

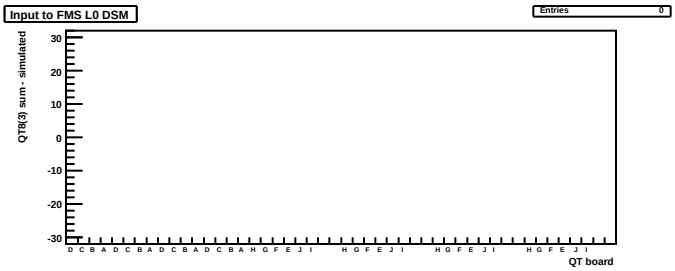

Input to FMS L0 DSM
Entries 0
QT8(1) sum
QT board

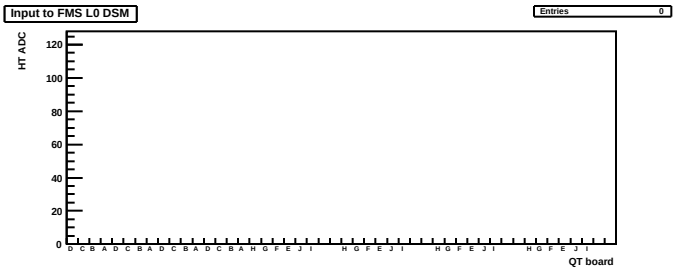

Input to FMS L0 DSM
Entries 0
QT8(1) sum - simulated
QT board

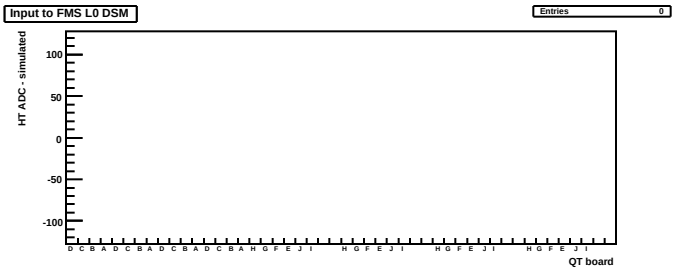

Input to FMS L0 DSM
Entries 0
QT8(2) sum
QT board

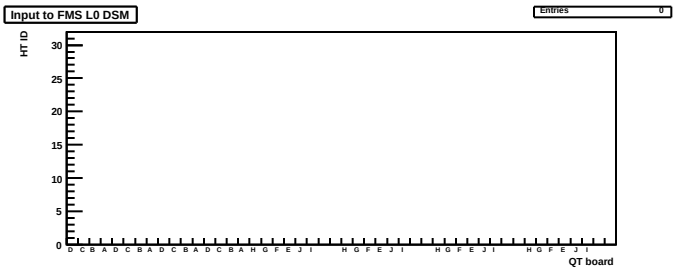

Input to FMS L0 DSM
Entries 0
QT8(2) sum - simulated
QT board

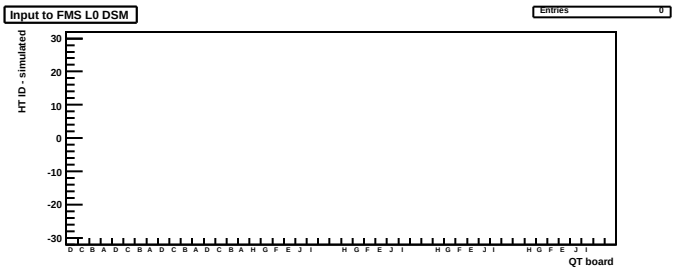

Input to FMS L0 DSM
Entries 0
QT8(3) sum
QT board

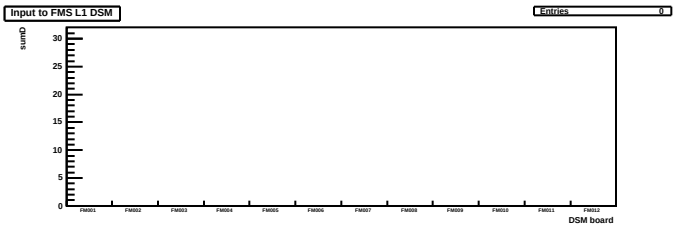

Input to FMS L0 DSM
Entries 0
QT8(3) sum - simulated
QT board

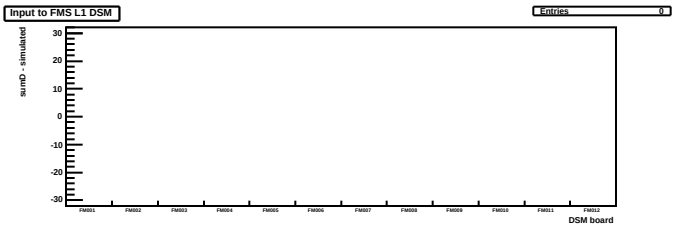

Input to FMS L0 DSM
Entries 0
HT ADC
QT board

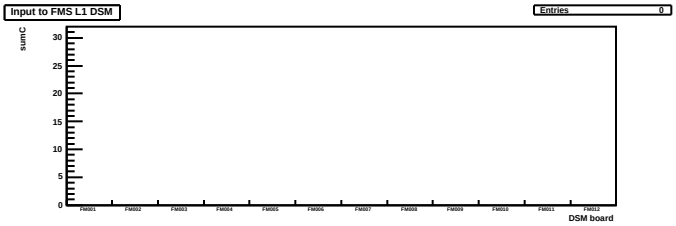

Input to FMS L0 DSM
Entries 0
HT ADC - simulated
QT board

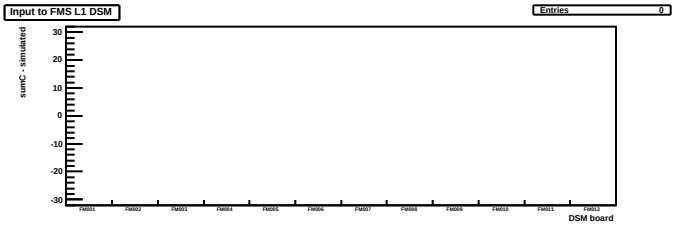

Input to FMS L0 DSM
Entries 0
HT ID
QT board

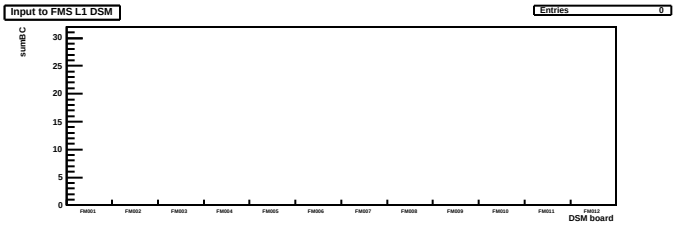

Input to FMS L0 DSM
Entries 0
HT ID - simulated
QT board

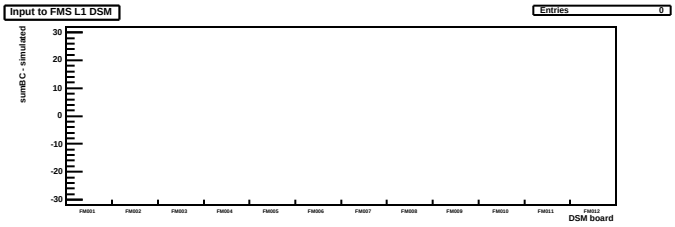

Input to FMS L1 DSM
Entries 0
sumD
DSM board

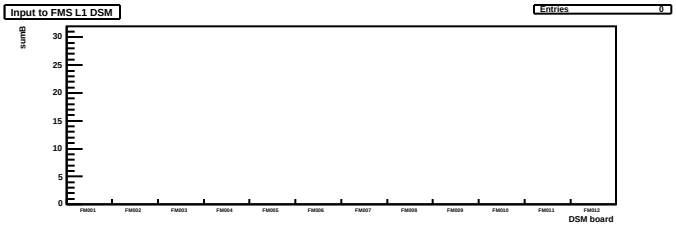

Input to FMS L1 DSM
Entries 0
sumD - simulated
DSM board

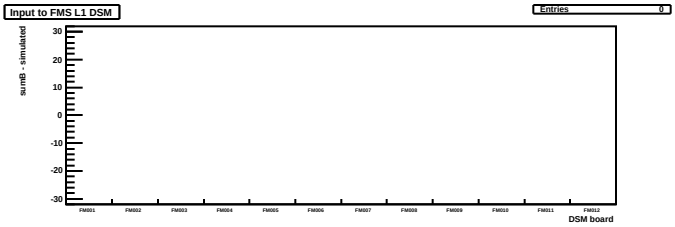

Input to FMS L1 DSM
Entries 0
sumC
DSM board

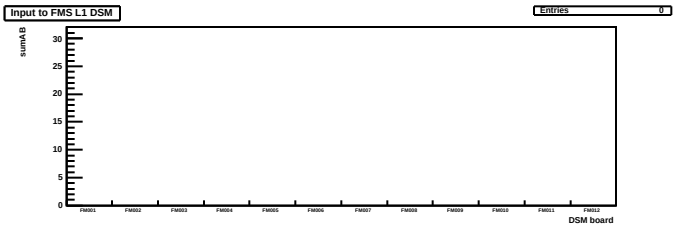

Input to FMS L1 DSM
Entries 0
sumC - simulated
DSM board

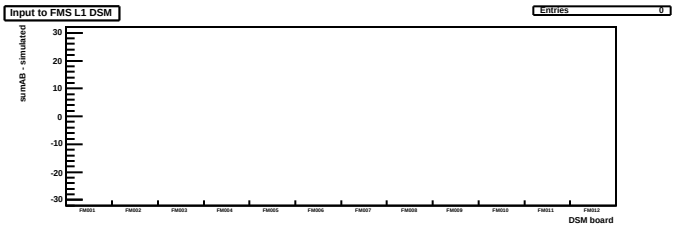

Input to FMS L1 DSM
Entries 0
sumBC
DSM board

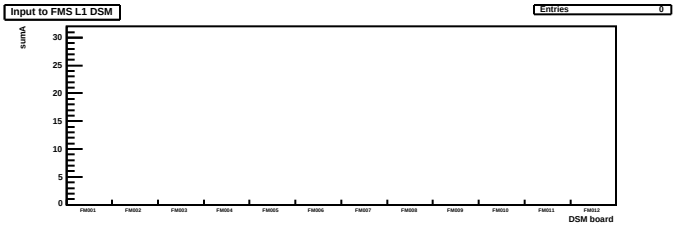

Input to FMS L1 DSM
Entries 0
sumBC - simulated
DSM board

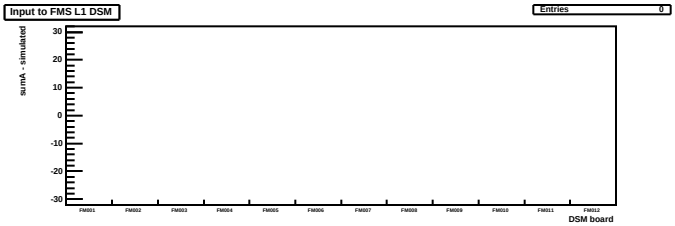

Input to FMS L1 DSM
Entries 0
sumB
DSM board

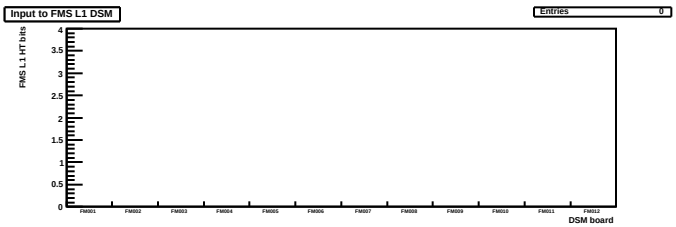

Input to FMS L1 DSM
Entries 0
sumB - simulated
DSM board

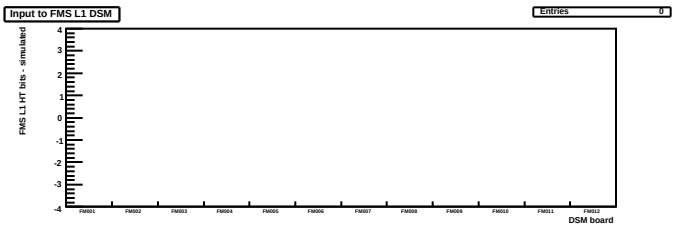

Input to FMS L1 DSM
Entries 0
sumAB
DSM board

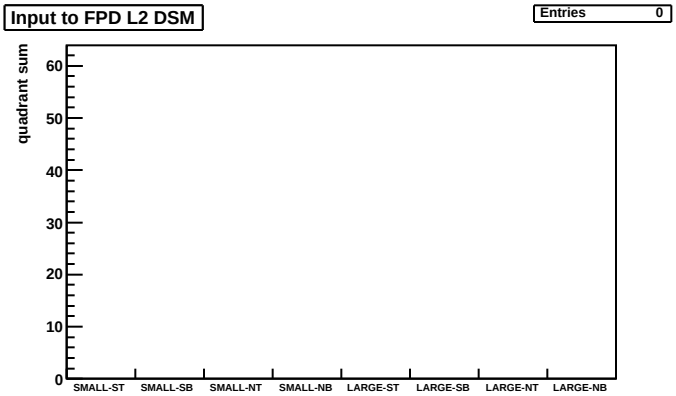

Input to FMS L1 DSM
Entries 0
sumAB - simulated
DSM board

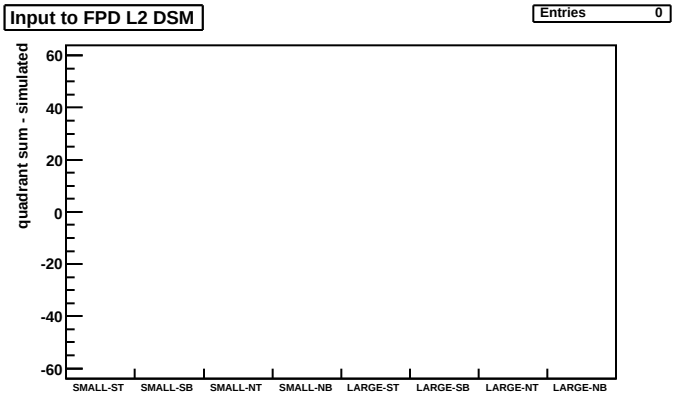

Input to FMS L1 DSM
Entries 0
sumA
DSM board

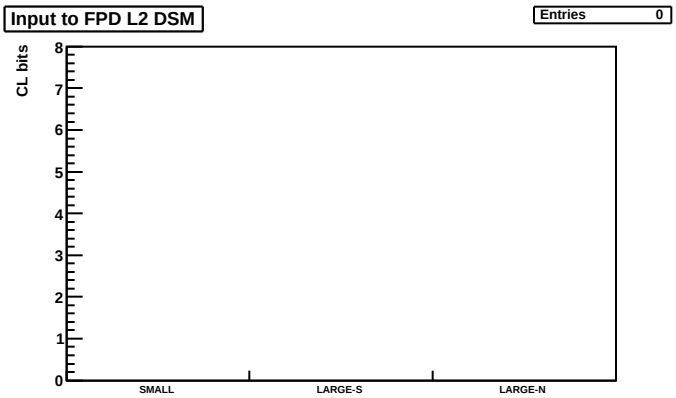

Input to FMS L1 DSM
Entries 0
sumA - simulated
DSM board

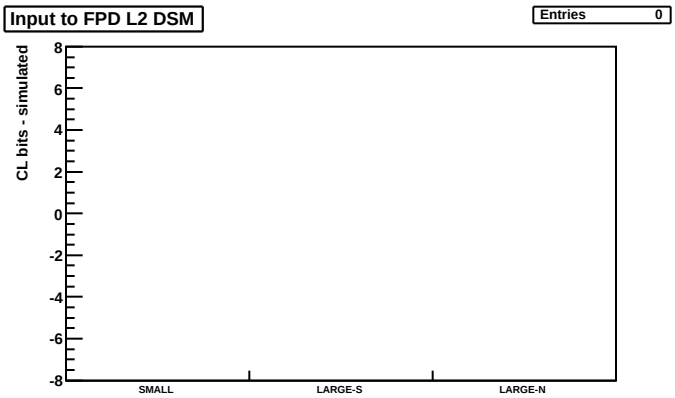

Input to FMS L1 DSM
Entries 0
FMS L1 HT bits
DSM board

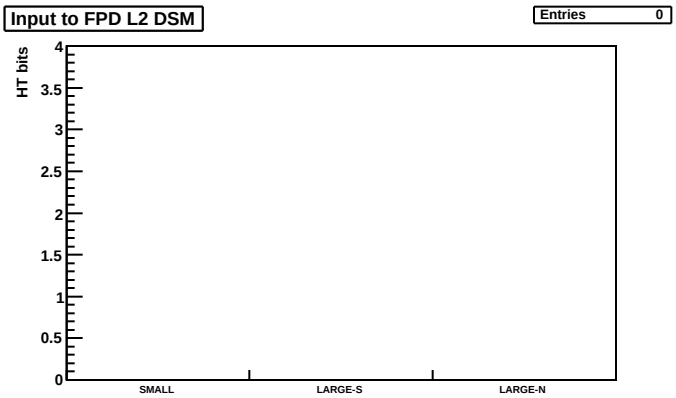

Input to FMS L1 DSM
Entries 0
FMS L1 HT bits - simulated
DSM board

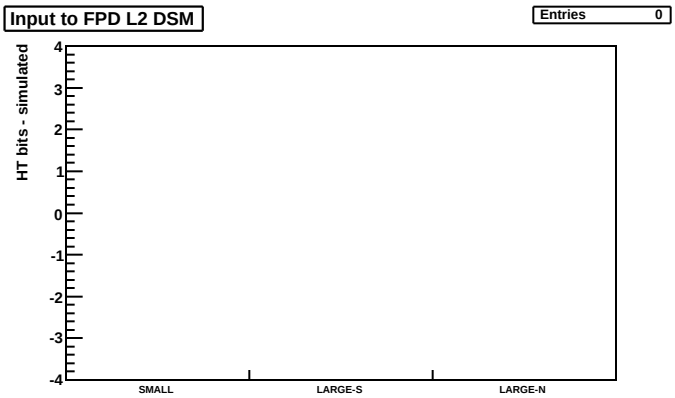

Input to FPD L2 DSM
Entries 0
quadrant sum
SMALL-ST
SMALL-SB
SMALL-NT
SMALL-NB
LARGE-ST
LARGE-SB
LARGE-NT
LARGE-NB

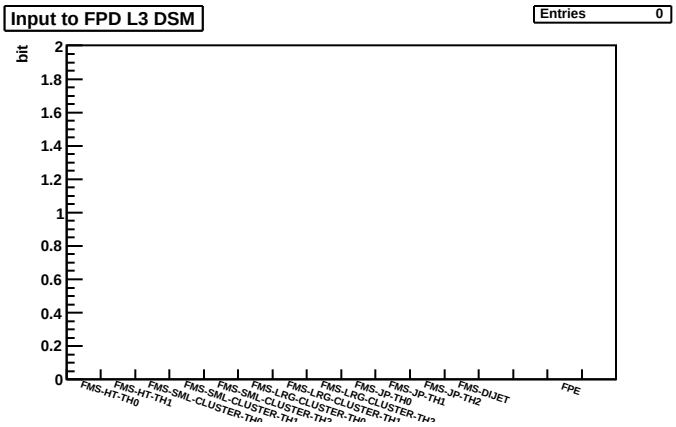

Input to FPD L2 DSM
Entries 0
quadrant sum - simulated
SMALL-ST
SMALL-SB
SMALL-NT
SMALL-NB
LARGE-ST
LARGE-SB
LARGE-NT
LARGE-NB

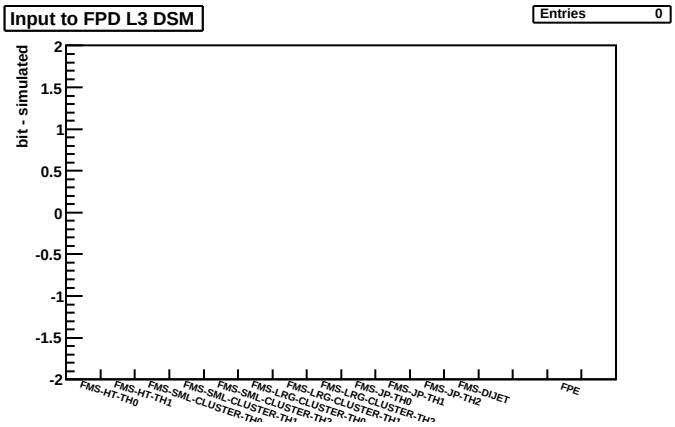

Input to FPD L2 DSM
Entries 0
CL bits
SMALL
LARGE-S
LARGE-N

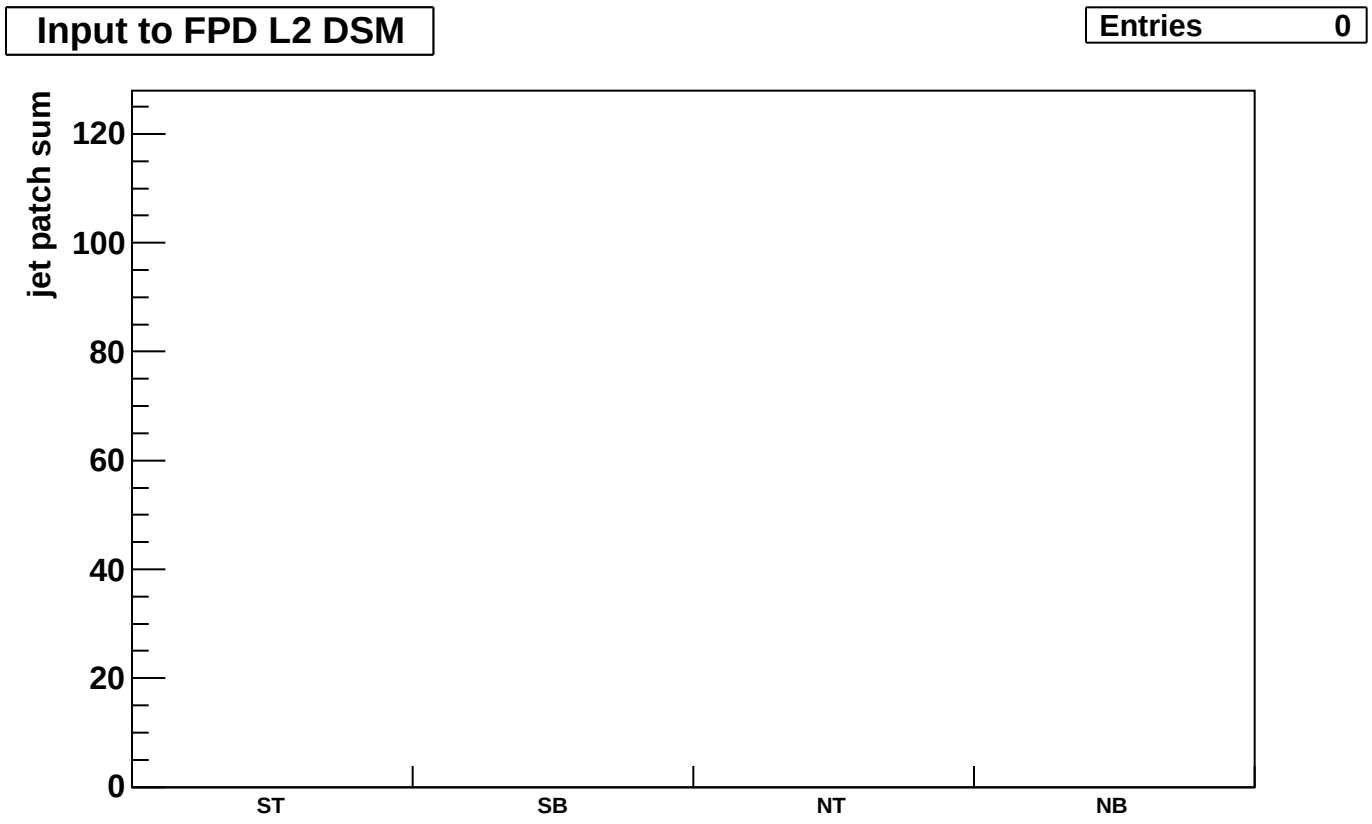

Input to FPD L2 DSM
Entries 0
CL bits - simulated
SMALL
LARGE-S
LARGE-N

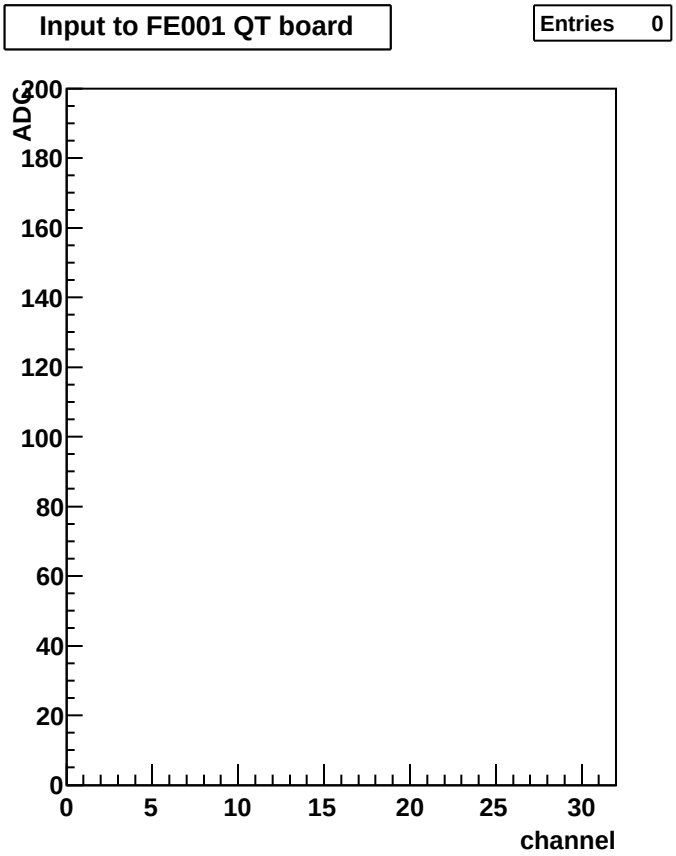

Input to FPD L2 DSM
Entries 0
HT bits
SMALL
LARGE-S
LARGE-N

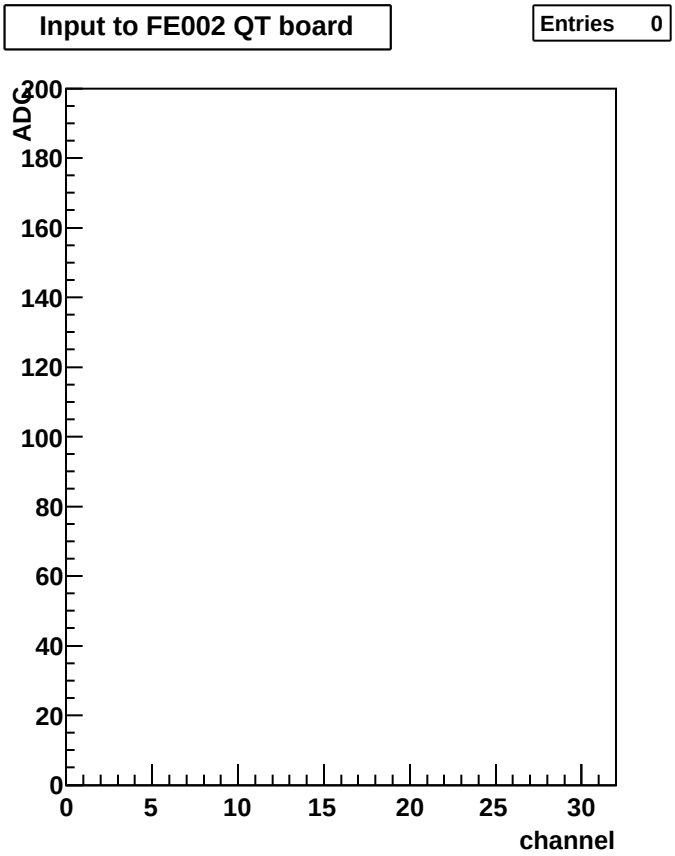

Input to FPD L2 DSM
Entries 0
HT bits - simulated
SMALL
LARGE-S
LARGE-N

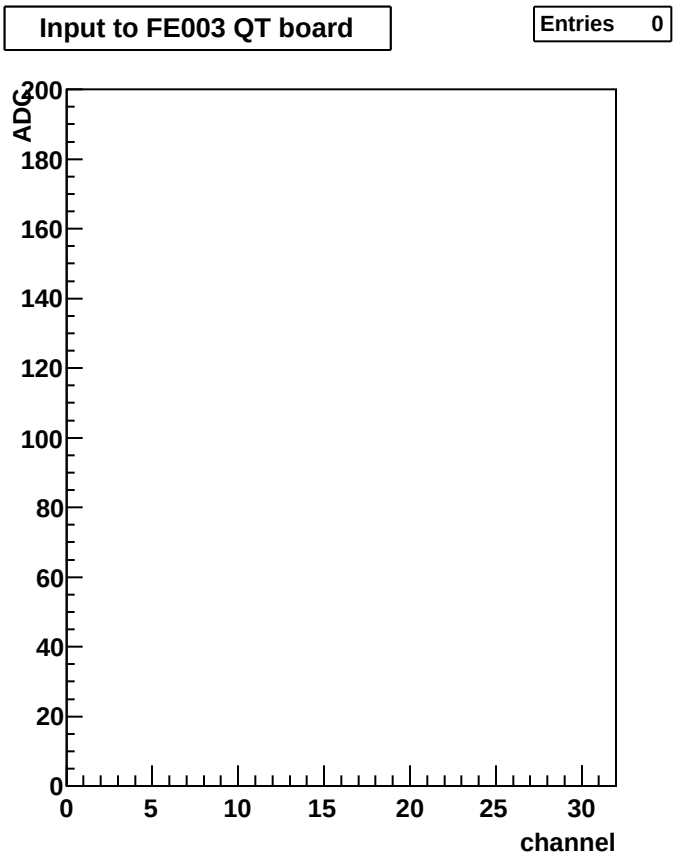

Input to FPD L3 DSM
Entries 0
bit
FMS-HT-TH0
FMS-HT-TH1
FMS-SML-CLUSTER-TH0
FMS-SML-CLUSTER-TH1
FMS-SML-CLUSTER-TH2
FMS-LRG-CLUSTER-TH0
FMS-LRG-CLUSTER-TH1
FMS-LRG-CLUSTER-TH2
FMS-JP-TH0
FMS-JP-TH1
FMS-JP-TH2
FMS-DIJET
FPE

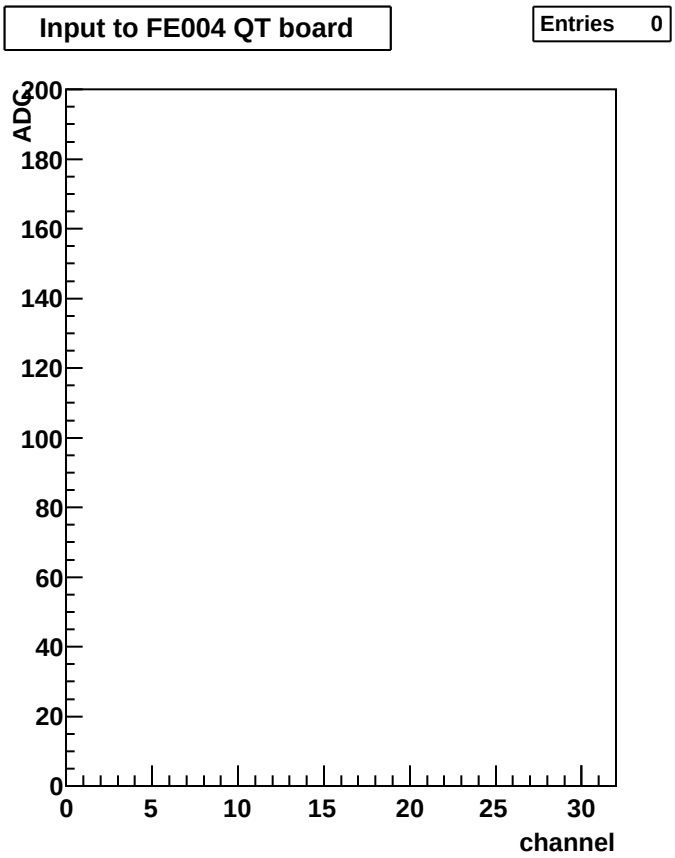

Input to FPD L3 DSM
Entries 0
bit - simulated
FMS-HT-TH0
FMS-HT-TH1
FMS-SML-CLUSTER-TH0
FMS-SML-CLUSTER-TH1
FMS-SML-CLUSTER-TH2
FMS-LRG-CLUSTER-TH0
FMS-LRG-CLUSTER-TH1
FMS-LRG-CLUSTER-TH2
FMS-JP-TH0
FMS-JP-TH1
FMS-JP-TH2
FMS-DIJET
FPE

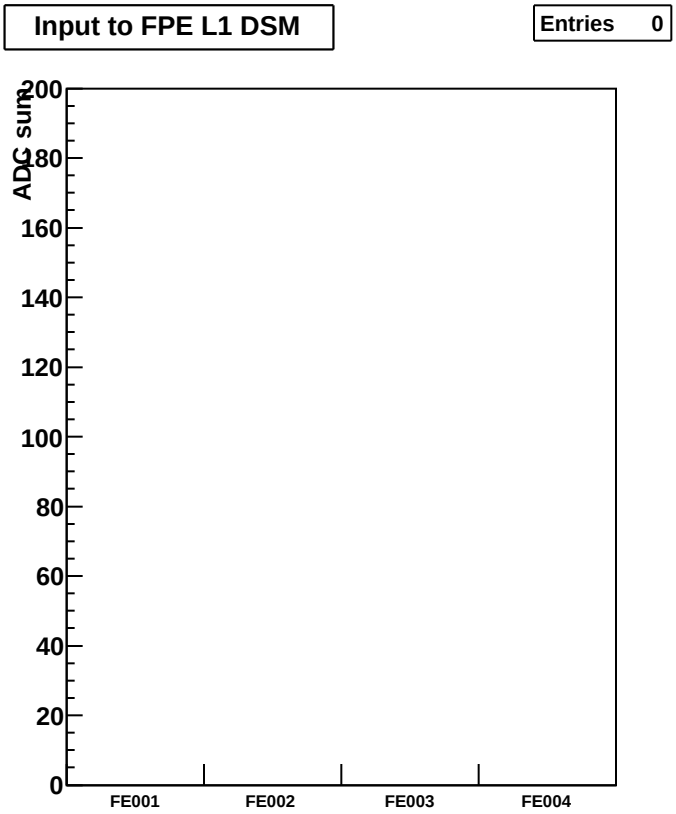

Input to FPD L2 DSM
Entries 0
jet patch sum
120
100
80
60
40
20
0
ST
SB
NT
NB

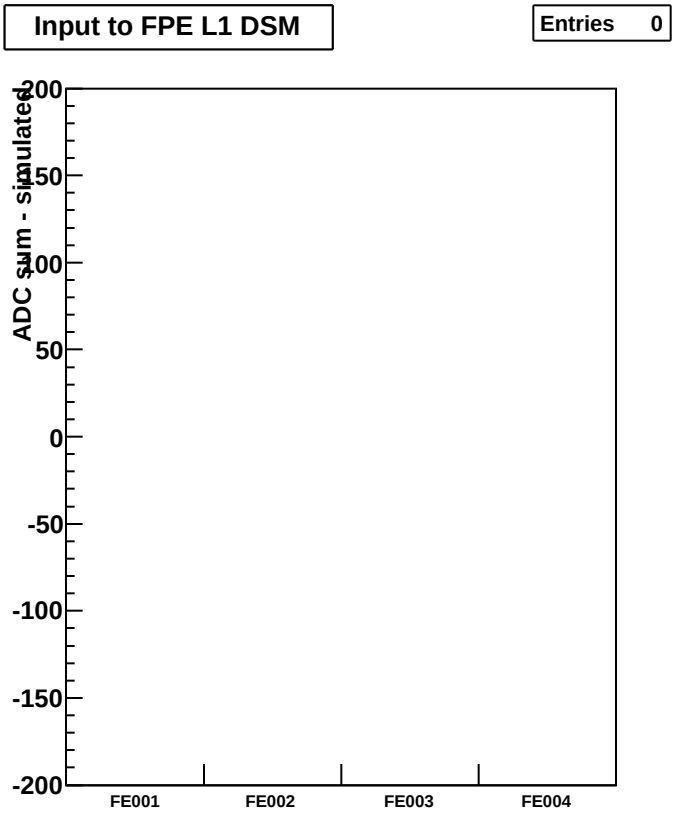

Input to FE001 QT board
Entries 0
ADC
200
180
160
140
120
100
80
60
40
20
0
0
5
10
15
20
25
30
channel

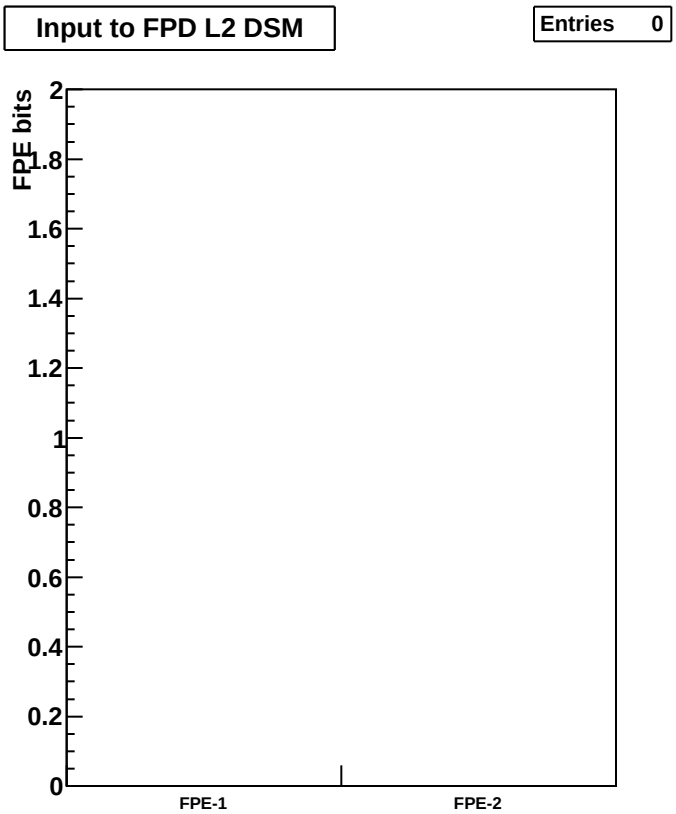

Input to FE002 QT board
Entries 0
ADC
200
180
160
140
120
100
80
60
40
20
0
0
5
10
15
20
25
30
channel

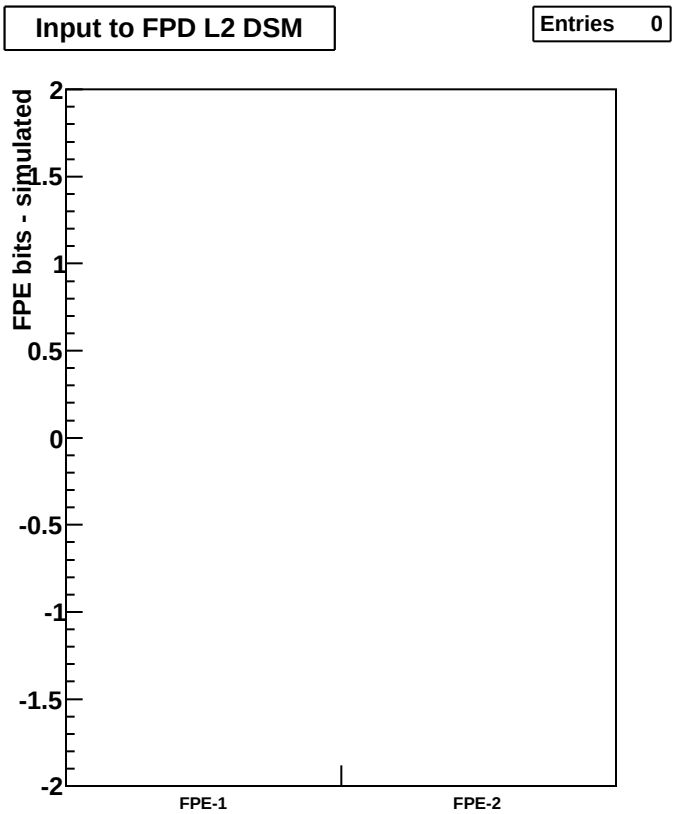

Input to FE003 QT board
Entries 0
ADC
200
180
160
140
120
100
80
60
40
20
0
0
5
10
15
20
25
30
channel


Input to FE004 QT board
Entries 0
ADC
200
180
160
140
120
100
80
60
40
20
0
0
5
10
15
20
25
30
channel


Input to FPE L1 DSM
Entries 0
ADC sum
200
180
160
140
120
100
80
60
40
20
0
FE001
FE002
FE003
FE004


Input to FPE L1 DSM
Entries 0
ADC sum - simulated
200
150
100
50
0
-50
-100
-150
-200
FE001
FE002
FE003
FE004


Input to FPD L2 DSM
Entries 0
FPE bits
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
FPE-1
FPE-2


Input to FPD L2 DSM
Entries 0
FPE bits - simulated
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
FPE-1
FPE-2