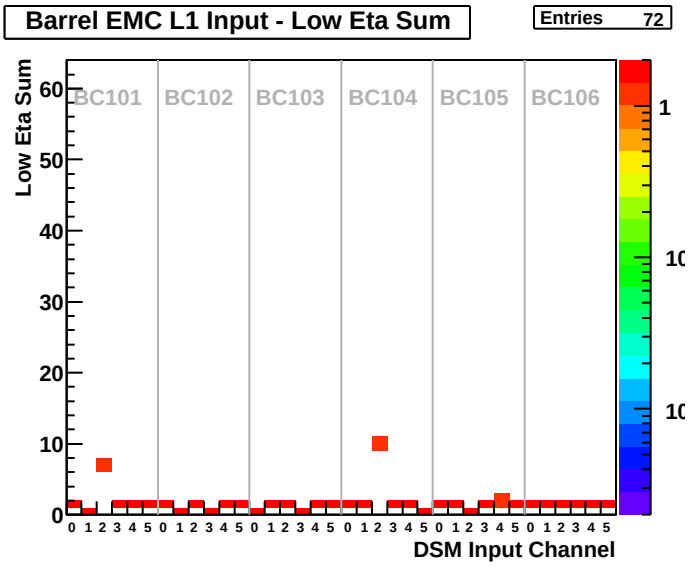
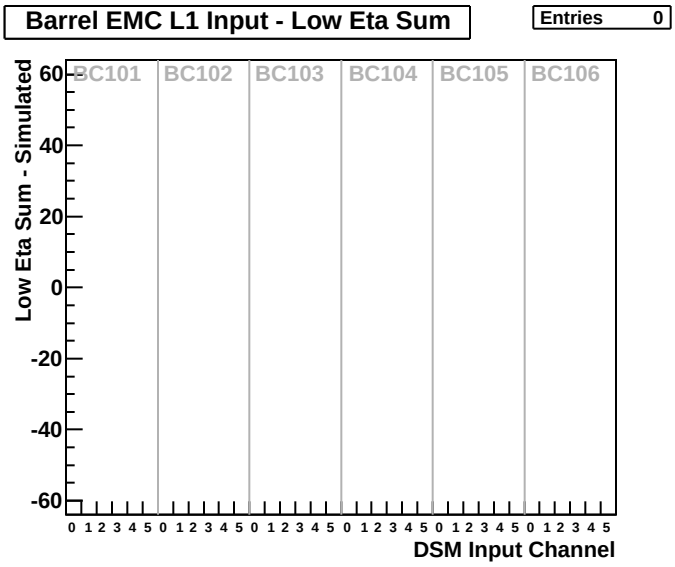
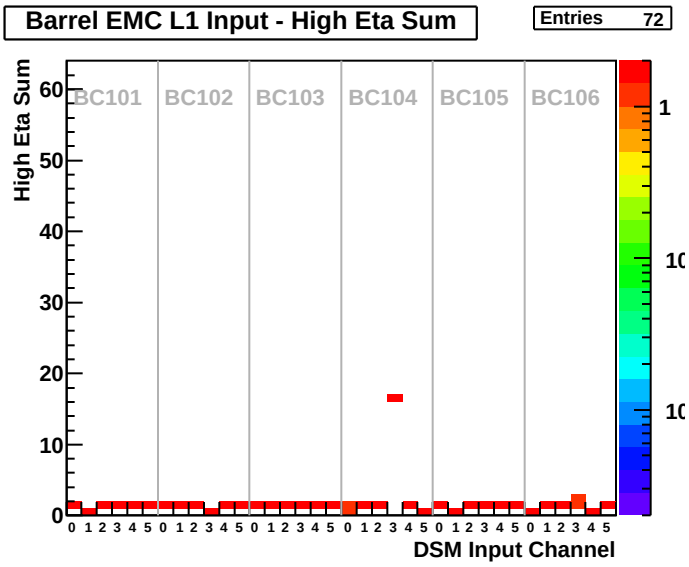
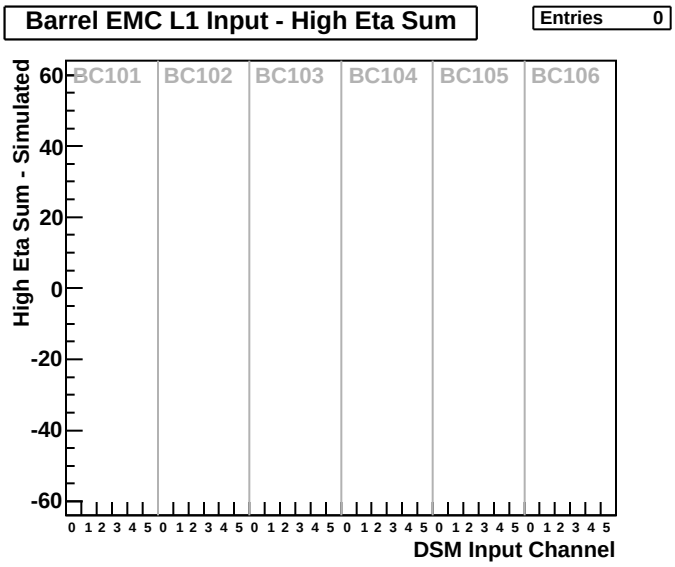
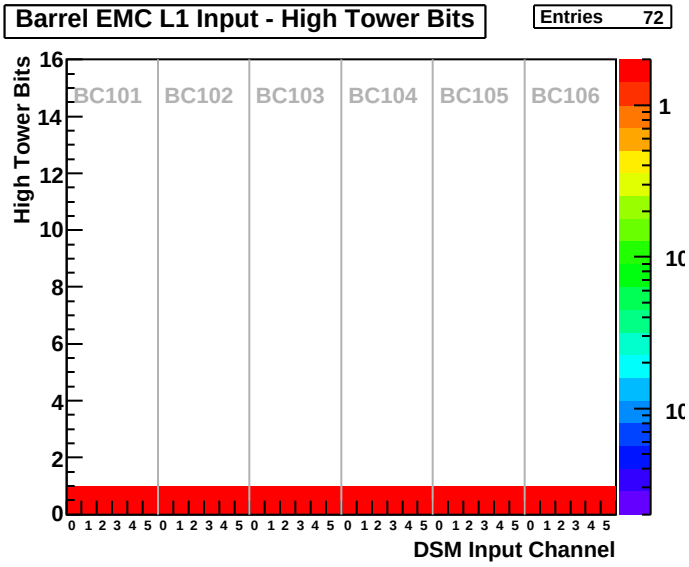
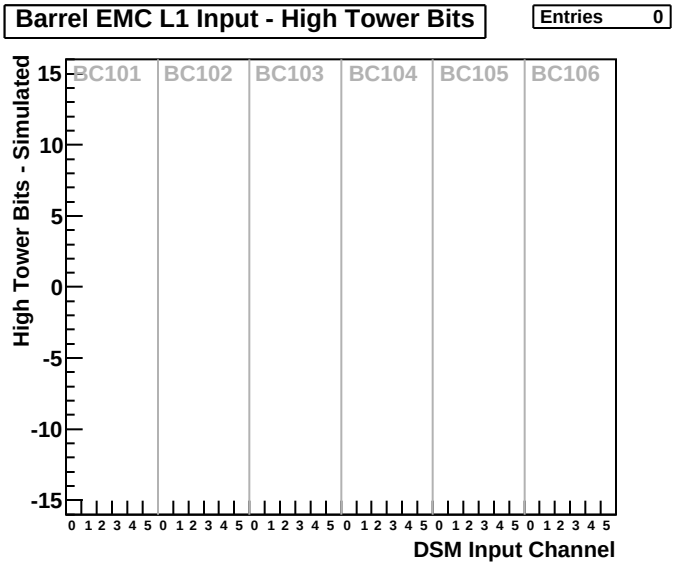

Barrel EMC L1 Input - Low Eta Sum
Entries 72
Low Eta Sum
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

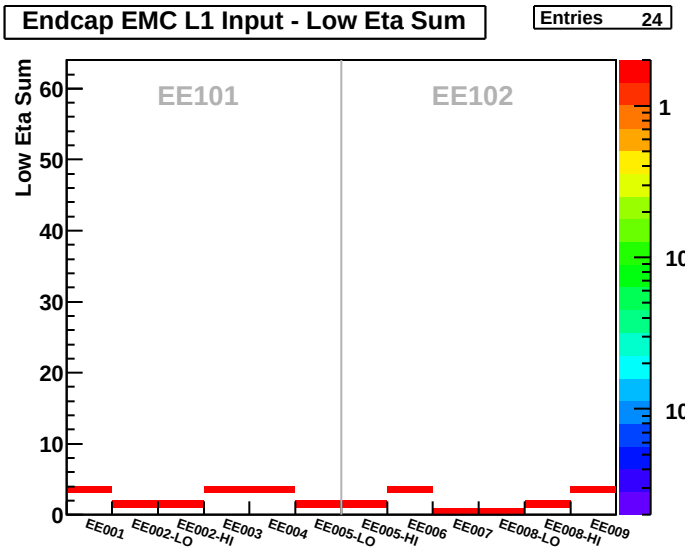

Barrel EMC L1 Input - Low Eta Sum
Entries 0
Low Eta Sum - Simulated
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

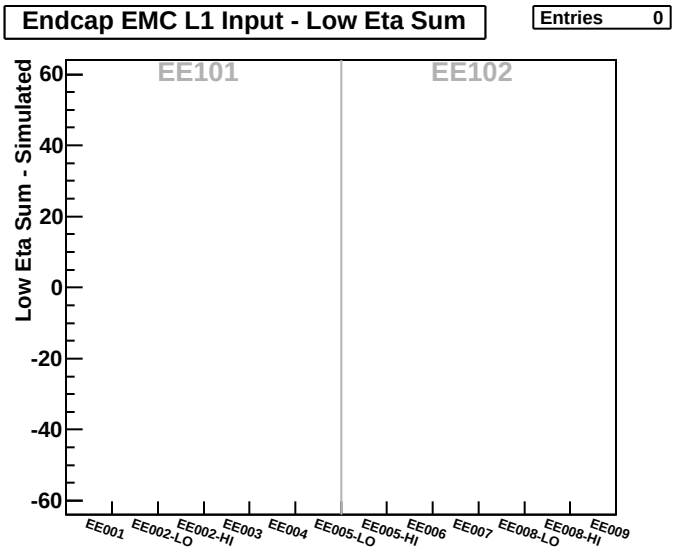

Barrel EMC L1 Input - High Eta Sum
Entries 72
High Eta Sum
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

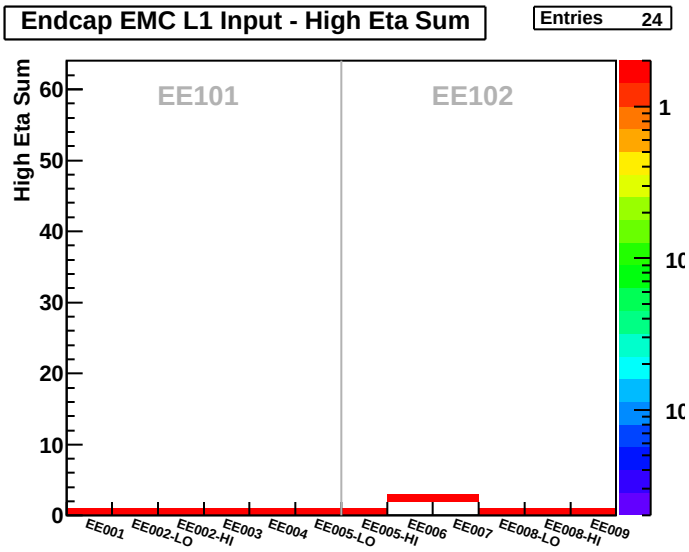

Barrel EMC L1 Input - High Eta Sum
Entries 0
High Eta Sum - Simulated
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

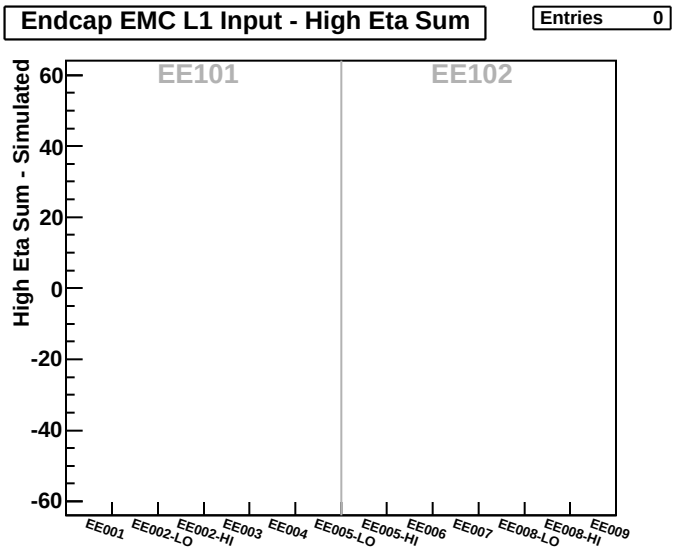

Barrel EMC L1 Input - High Tower Bits
Entries 72
High Tower Bits
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

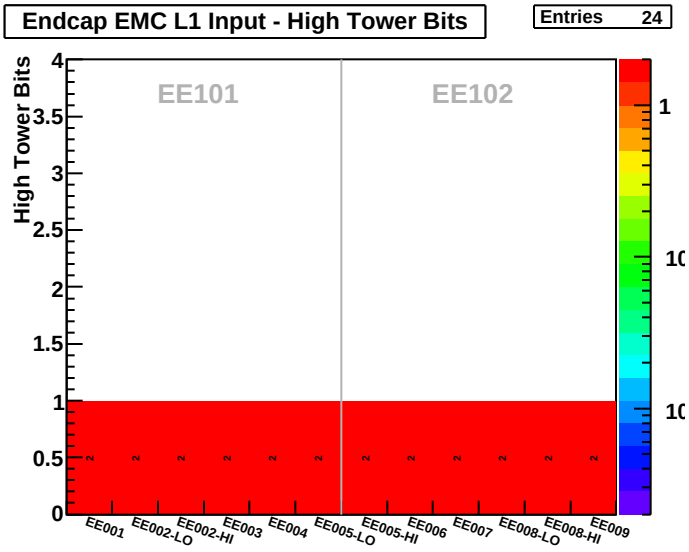

Barrel EMC L1 Input - High Tower Bits
Entries 0
High Tower Bits - Simulated
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

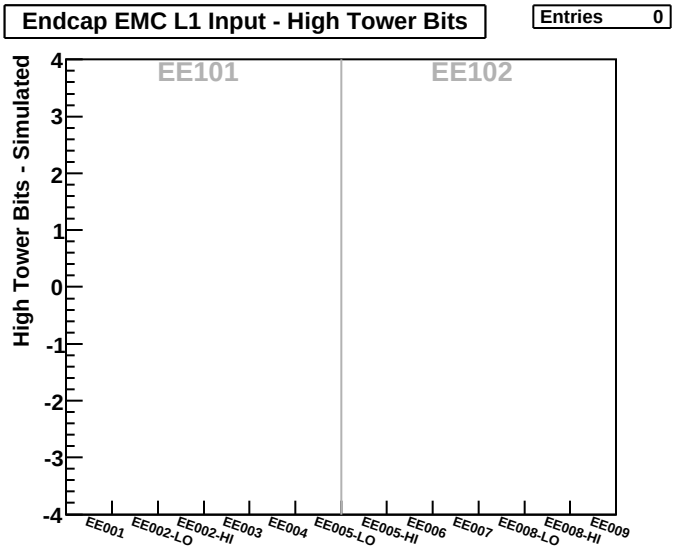

Endcap EMC L1 Input - Low Eta Sum
Entries 24
Low Eta Sum
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

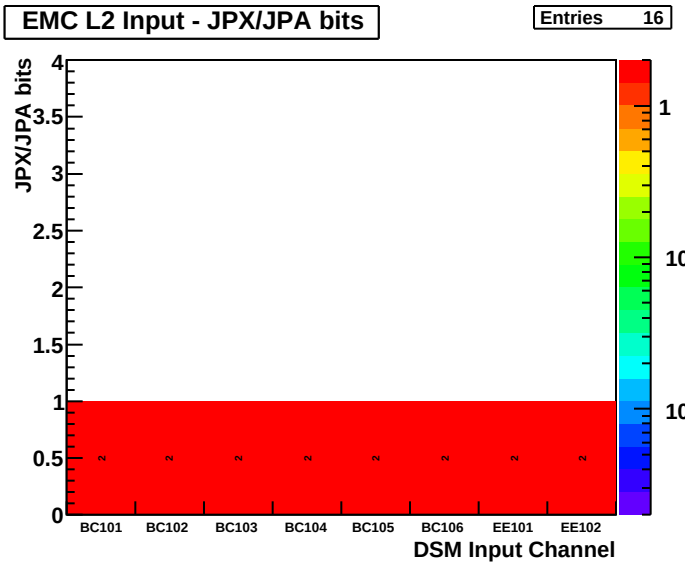

Endcap EMC L1 Input - Low Eta Sum
Entries 0
Low Eta Sum - Simulated
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

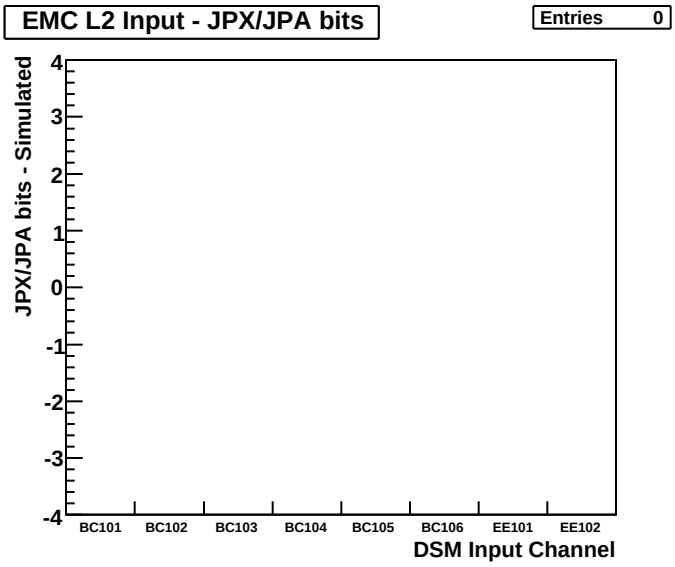

Endcap EMC L1 Input - High Eta Sum
Entries 24
High Eta Sum
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

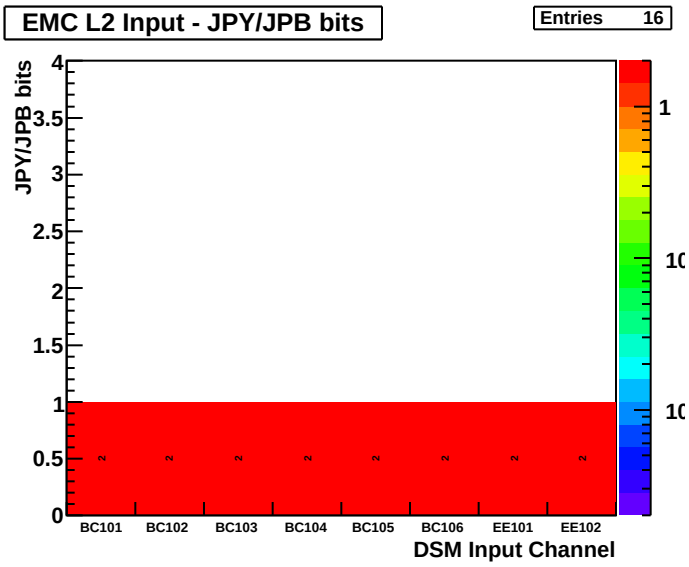

Endcap EMC L1 Input - High Eta Sum
Entries 0
High Eta Sum - Simulated
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

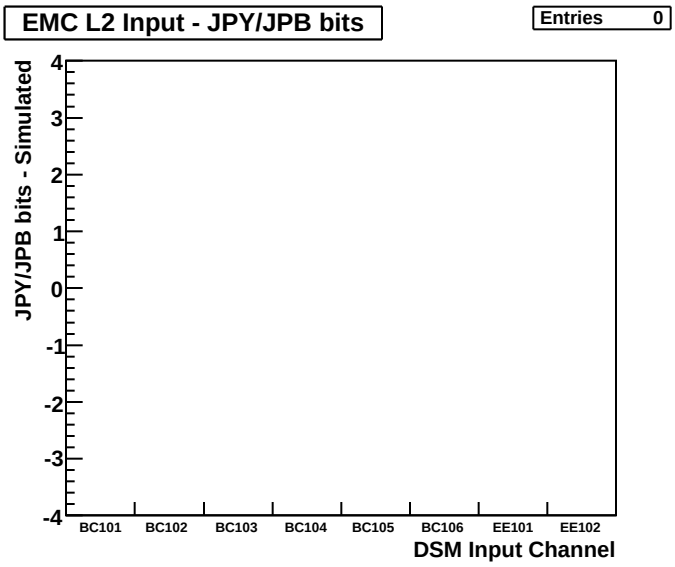

Endcap EMC L1 Input - High Tower Bits
Entries 24
High Tower Bits
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

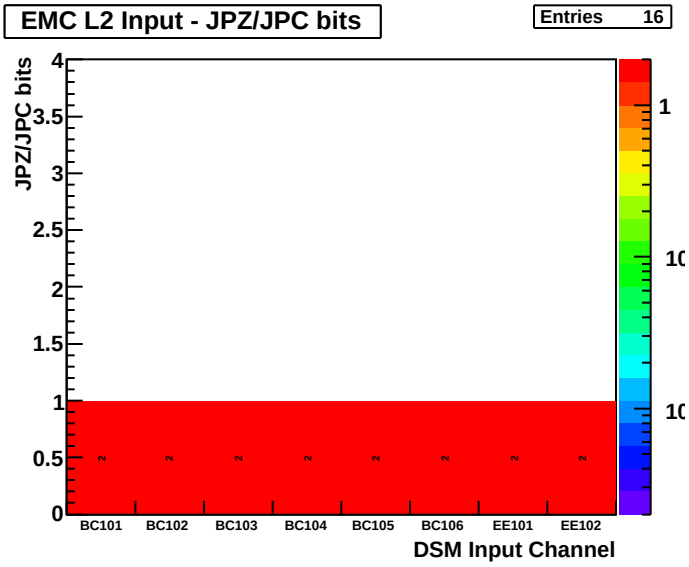

Endcap EMC L1 Input - High Tower Bits
Entries 0
High Tower Bits - Simulated
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

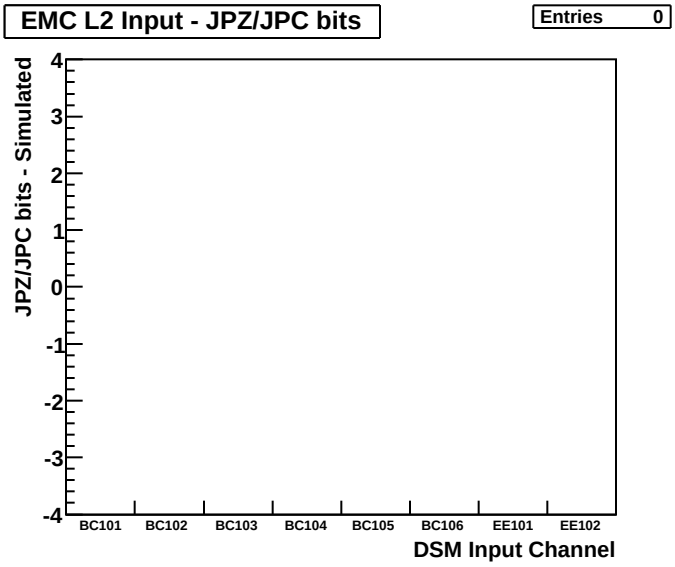

EMC L2 Input - JPX/JPA bits
Entries 16
JPX/JPA bits
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

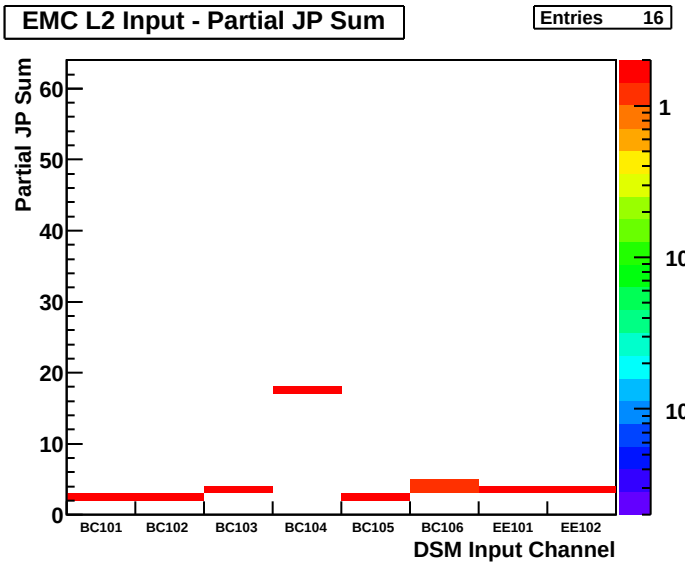

EMC L2 Input - JPX/JPA bits
Entries 0
JPX/JPA bits - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

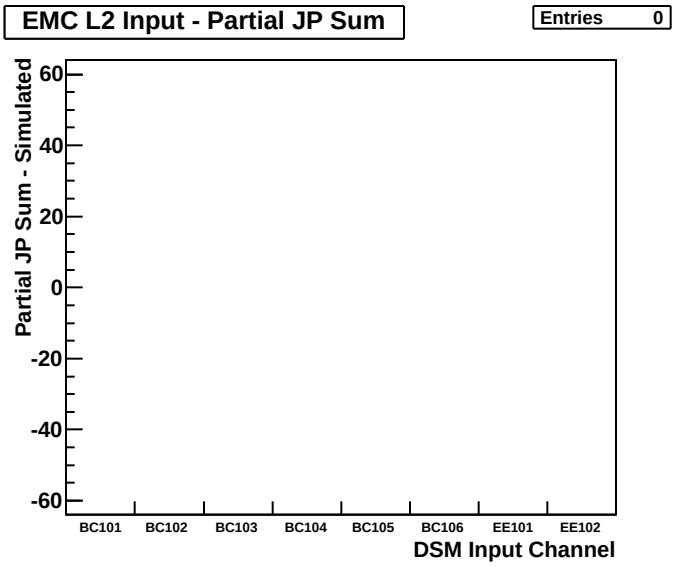

EMC L2 Input - JPY/JPB bits
Entries 16
JPY/JPB bits
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

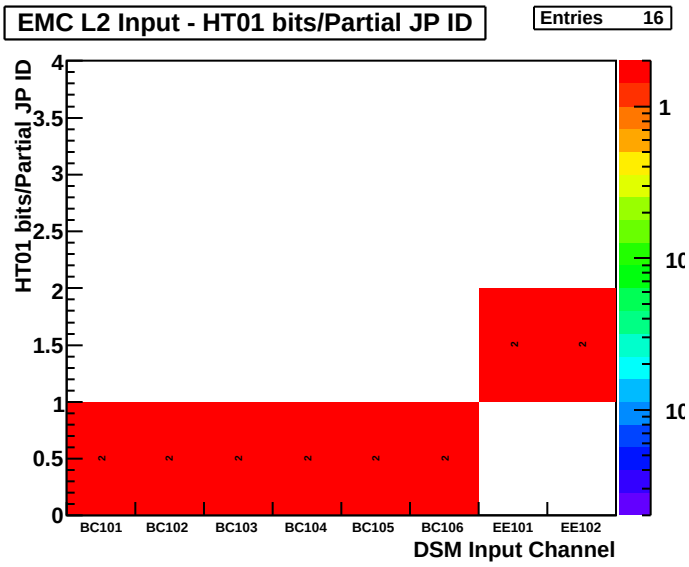

EMC L2 Input - JPY/JPB bits
Entries 0
JPY/JPB bits - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

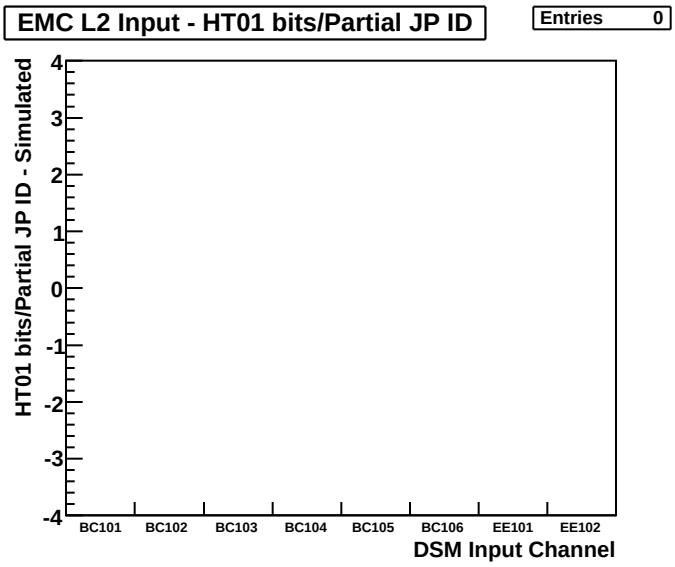

EMC L2 Input - JPZ/JPC bits
Entries 16
JPZ/JPC bits
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

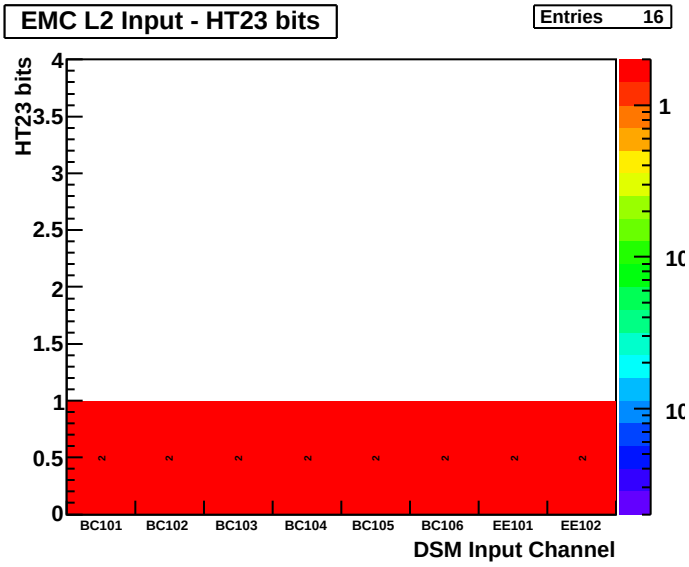

EMC L2 Input - JPZ/JPC bits
Entries 0
JPZ/JPC bits - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

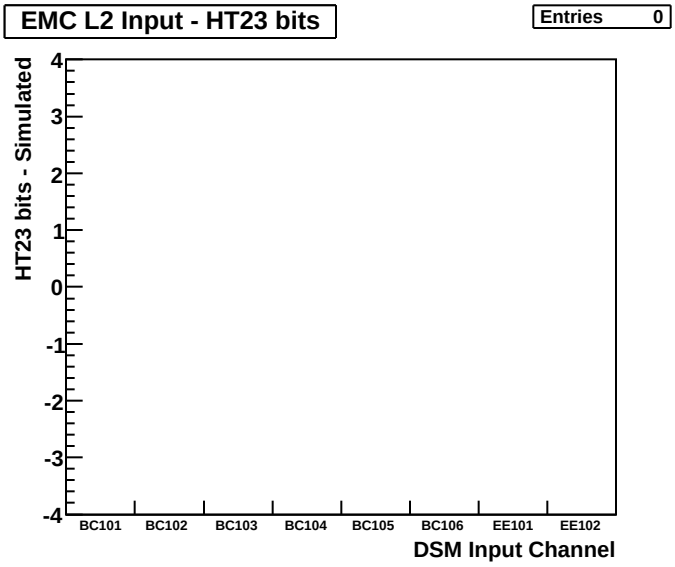

EMC L2 Input - Partial JP Sum
Entries 16
Partial JP Sum
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

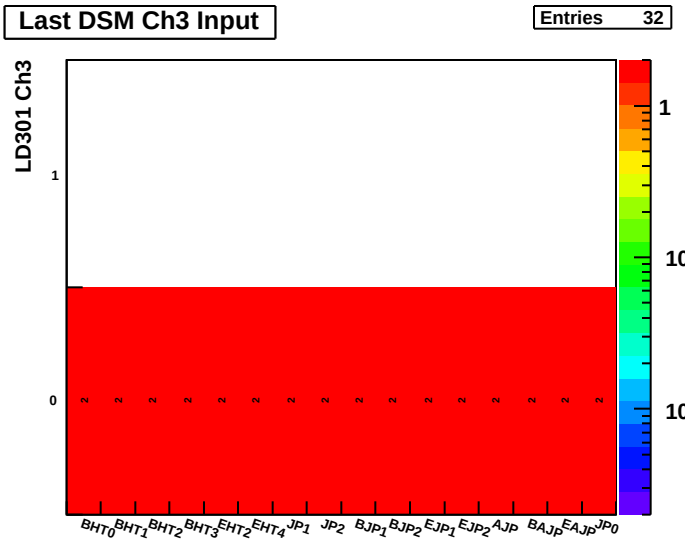

EMC L2 Input - Partial JP Sum
Entries 0
Partial JP Sum - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

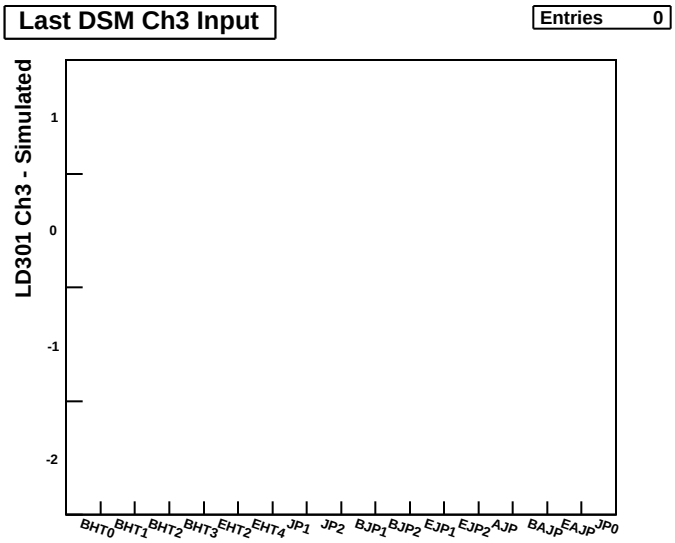

EMC L2 Input - HT01 bits/Partial JP ID
Entries 16
HT01 bits/Partial JP ID
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

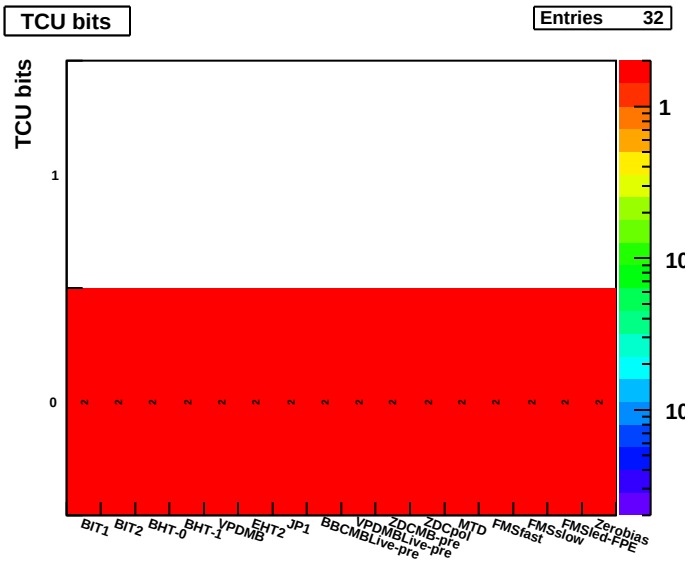

EMC L2 Input - HT01 bits/Partial JP ID
Entries 0
HT01 bits/Partial JP ID - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

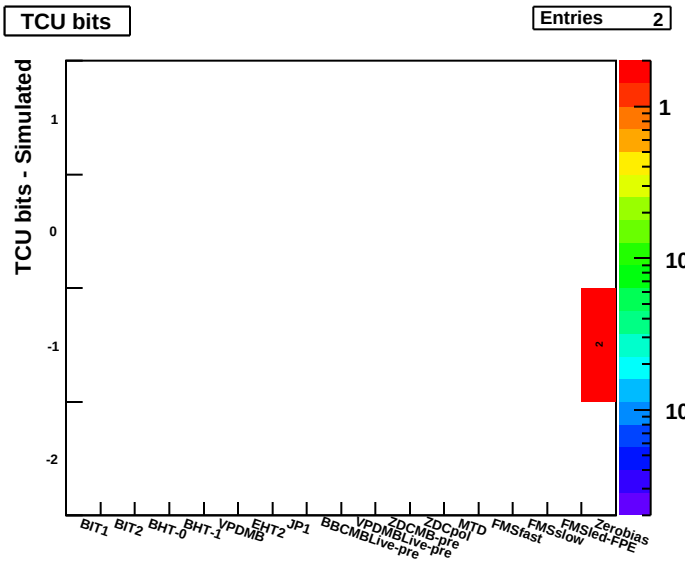

EMC L2 Input - HT23 bits
Entries 16
HT23 bits
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

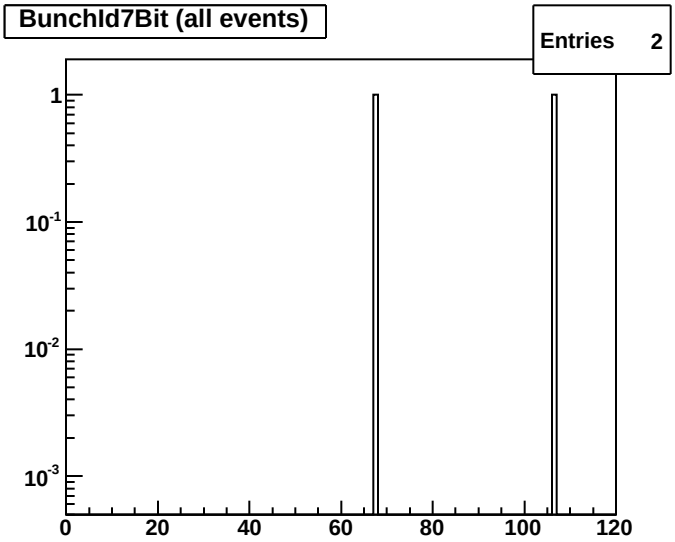

EMC L2 Input - HT23 bits
Entries 0
HT23 bits - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

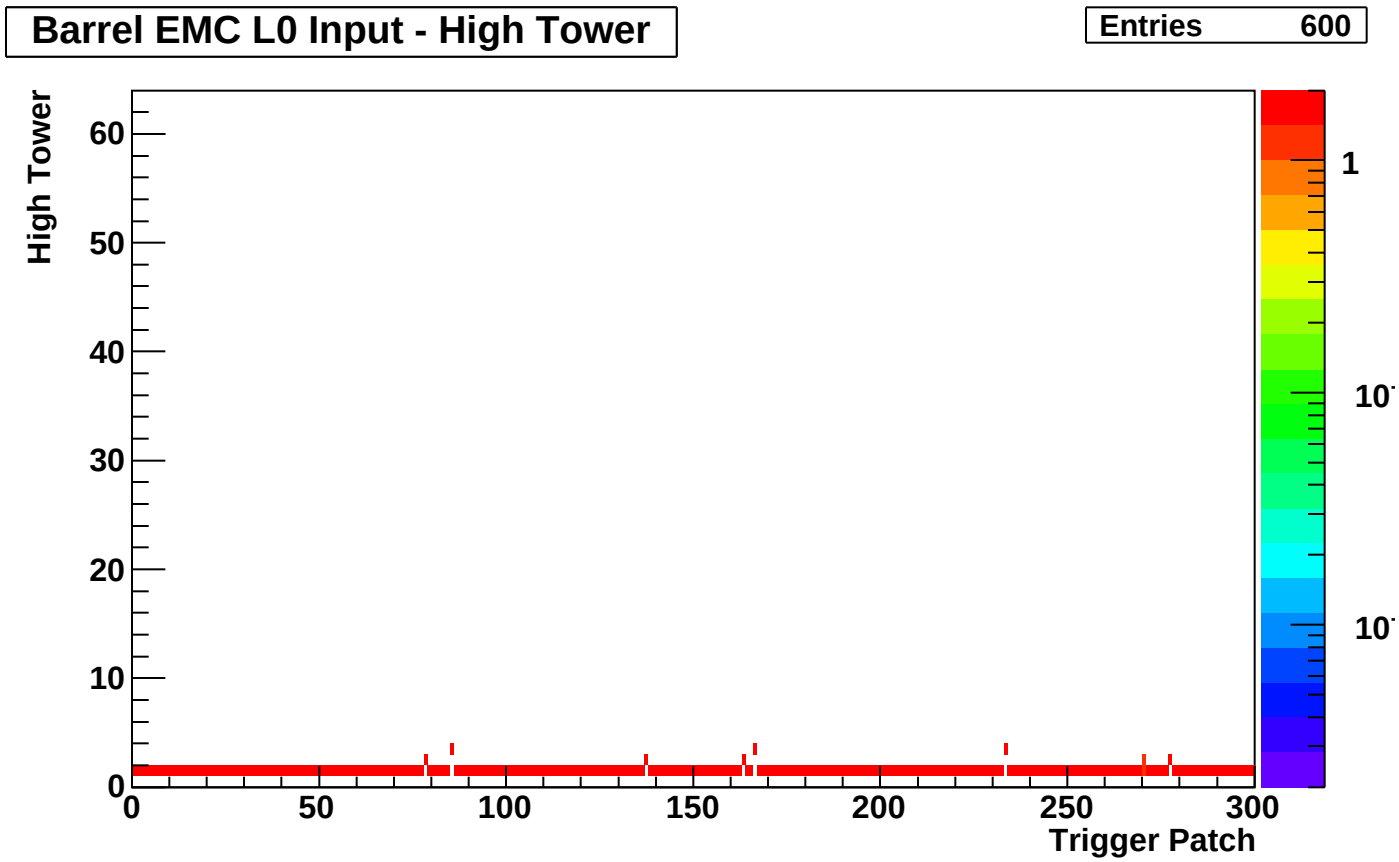

Last DSM Ch3 Input
Entries 32
LD301 Ch3
BHT0 BHT1 BHT2 BHT3 EHT2 EHT4 JP1 JP2 BJP1 BJP2 EJP1 EJP2 AJP BAJP EAJP JP0

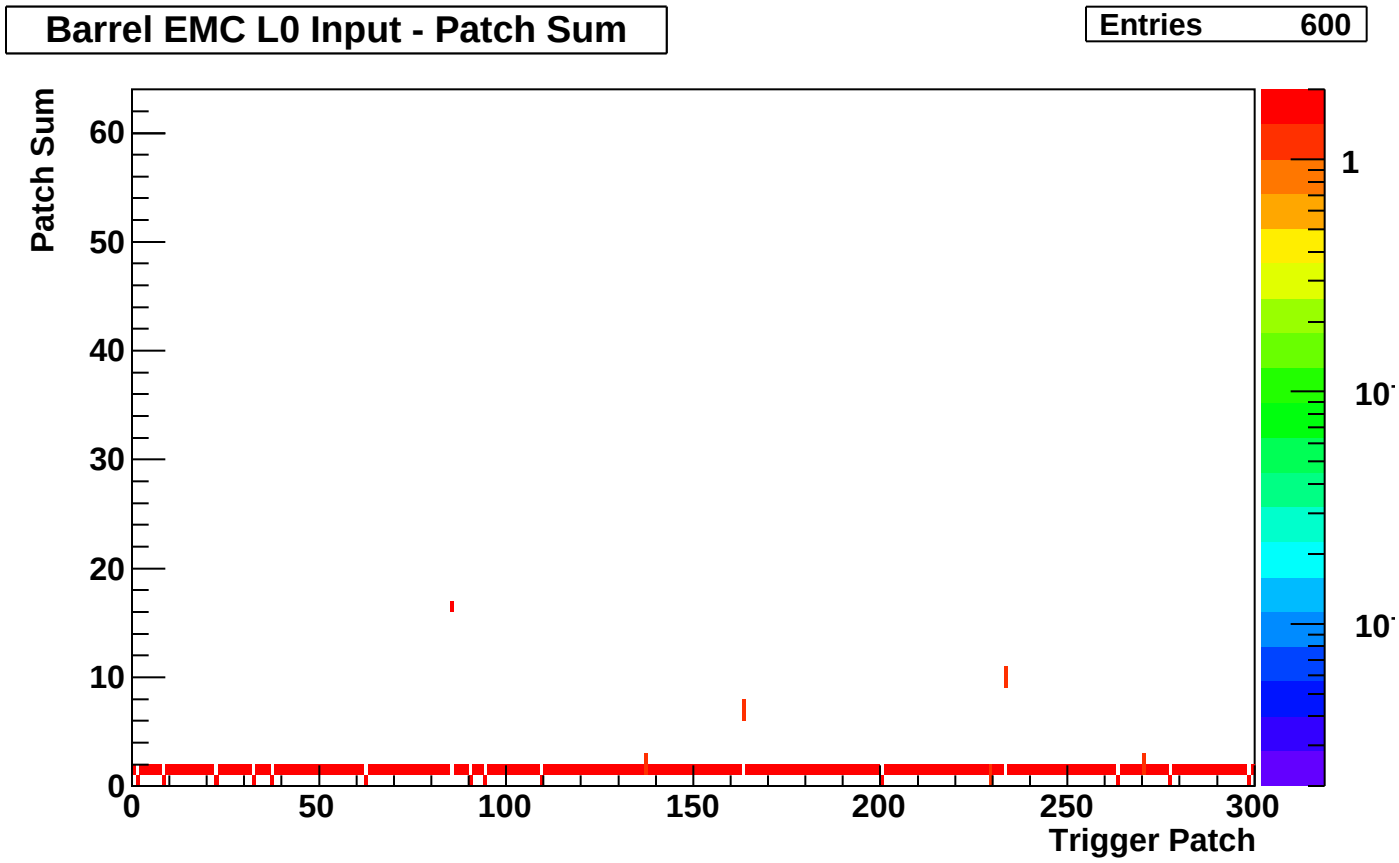

Last DSM Ch3 Input
Entries 0
LD301 Ch3 - Simulated
BHT0 BHT1 BHT2 BHT3 EHT2 EHT4 JP1 JP2 BJP1 BJP2 EJP1 EJP2 AJP BAJP EAJP JP0

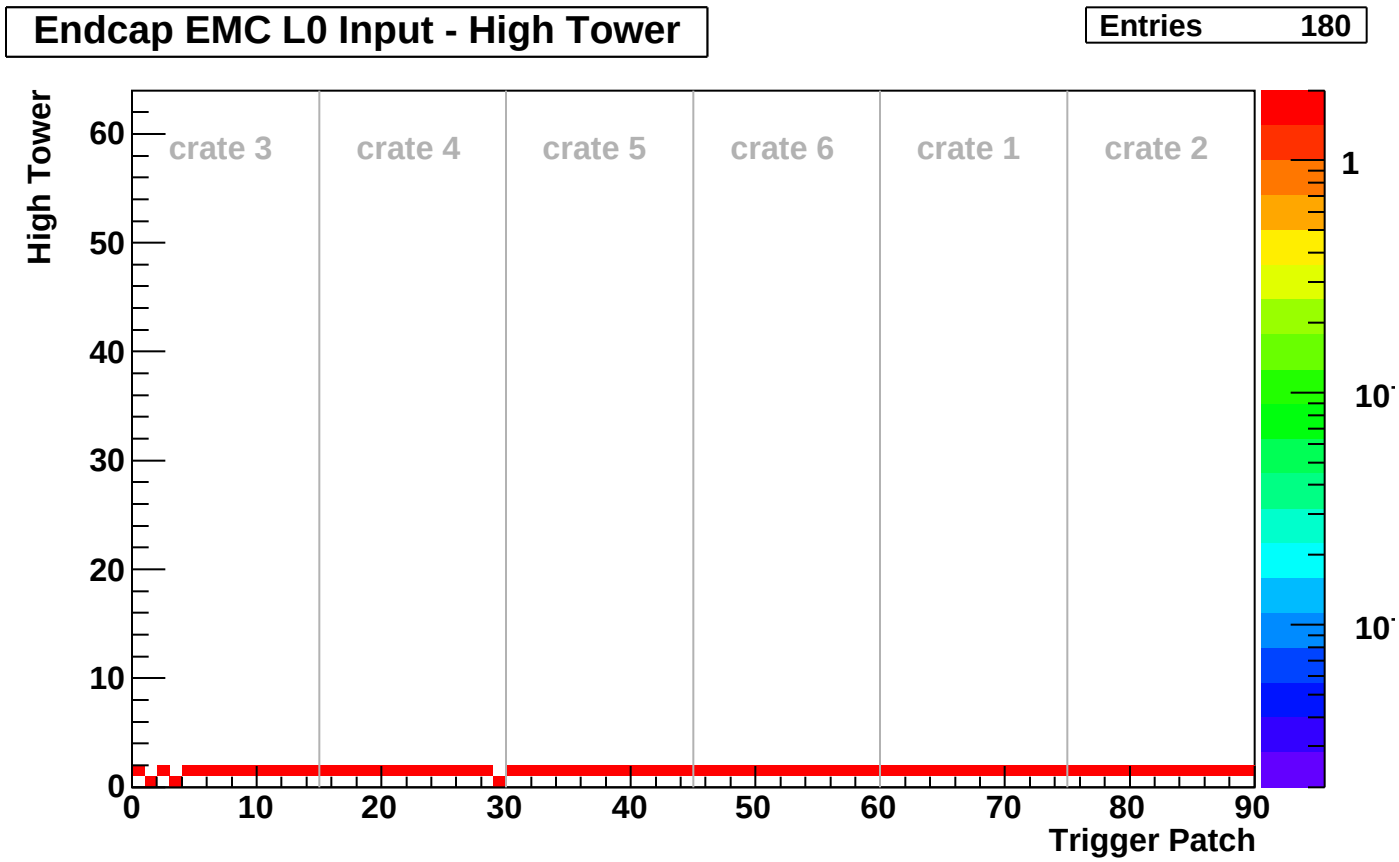

TCU bits
Entries 32
TCU bits
BIT1 BIT2 BHT-0 BHT-1 VPDMB EHT2 JP1 BBCMBLive-pre VPDMBLive-pre ZDCMB-pre ZDCpol MTD FMSfast FMSslow FMSled-FPE Zerobias

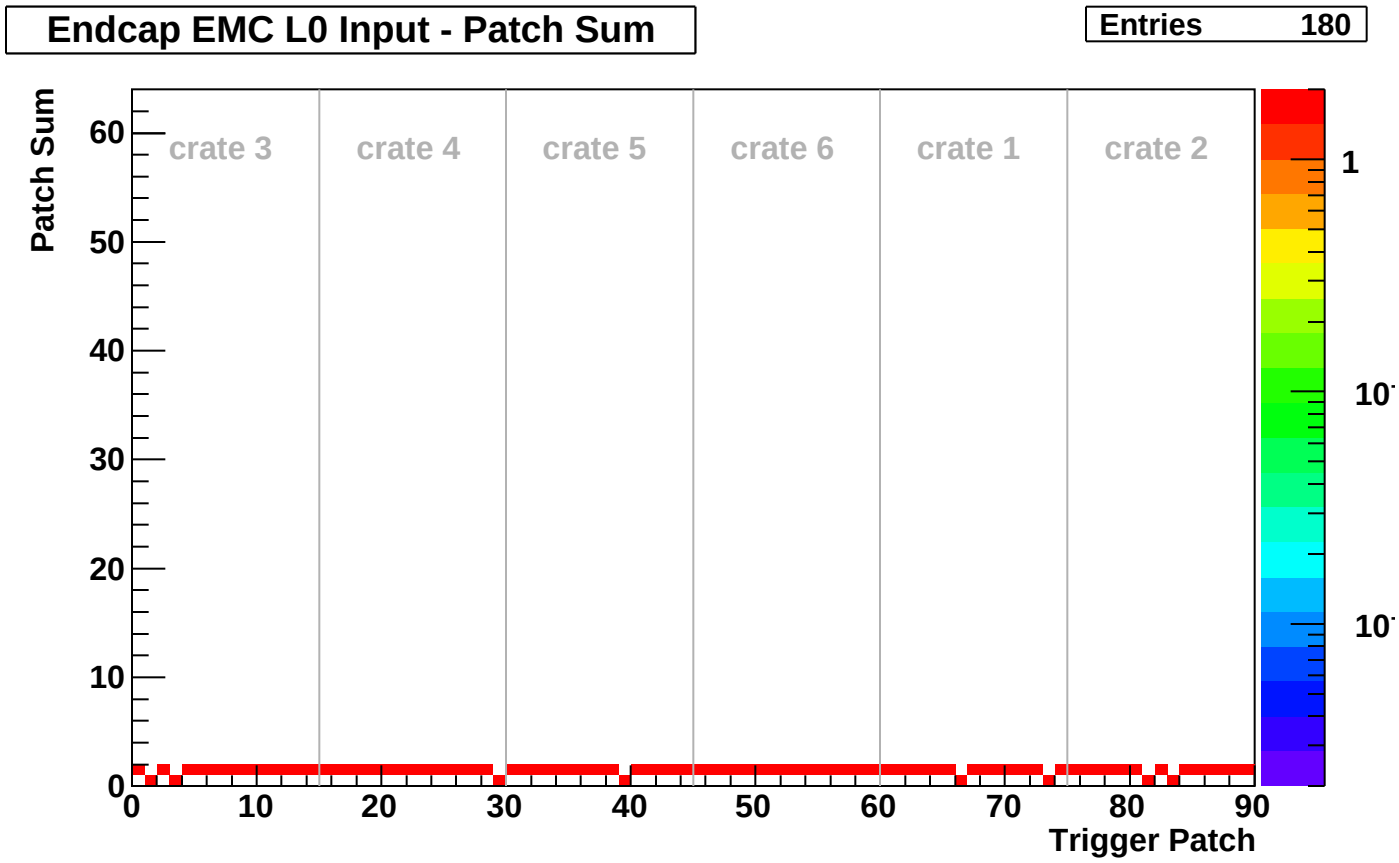

TCU bits
Entries 2
TCU bits - Simulated
BIT1 BIT2 BHT-0 BHT-1 VPDMB EHT2 JP1 BBCMBLive-pre VPDMBLive-pre ZDCMB-pre ZDCpol MTD FMSfast FMSslow FMSled-FPE Zerobias

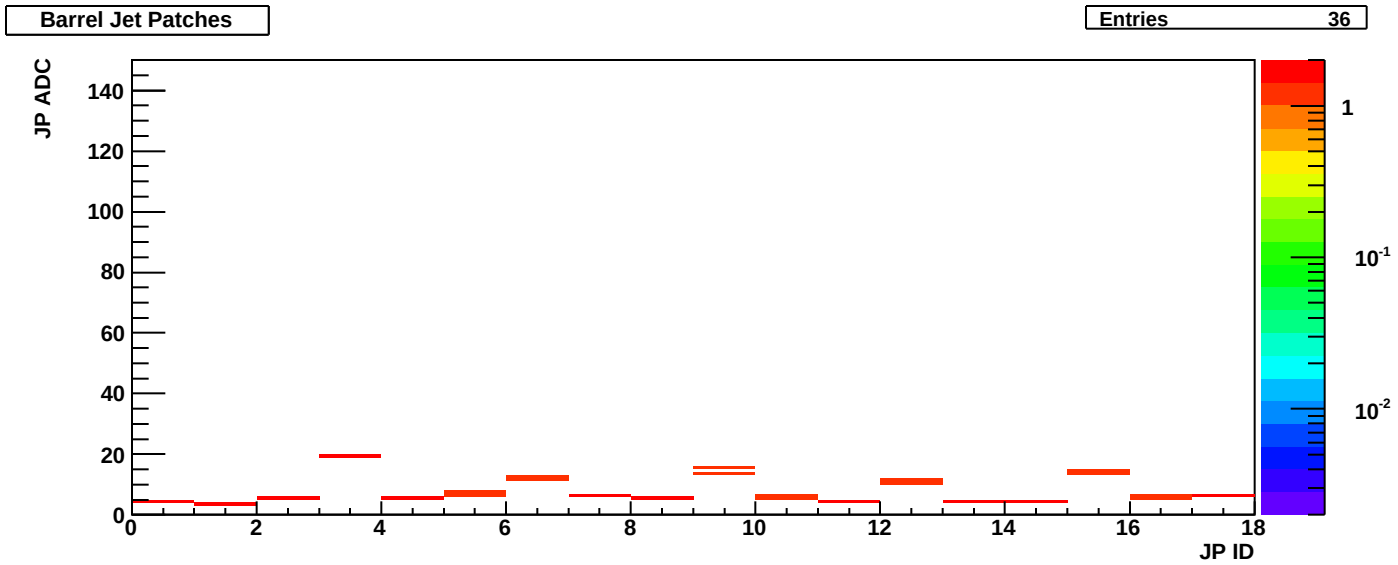

BunchId7Bit (all events)
Entries 2
0 20 40 60 80 100 120

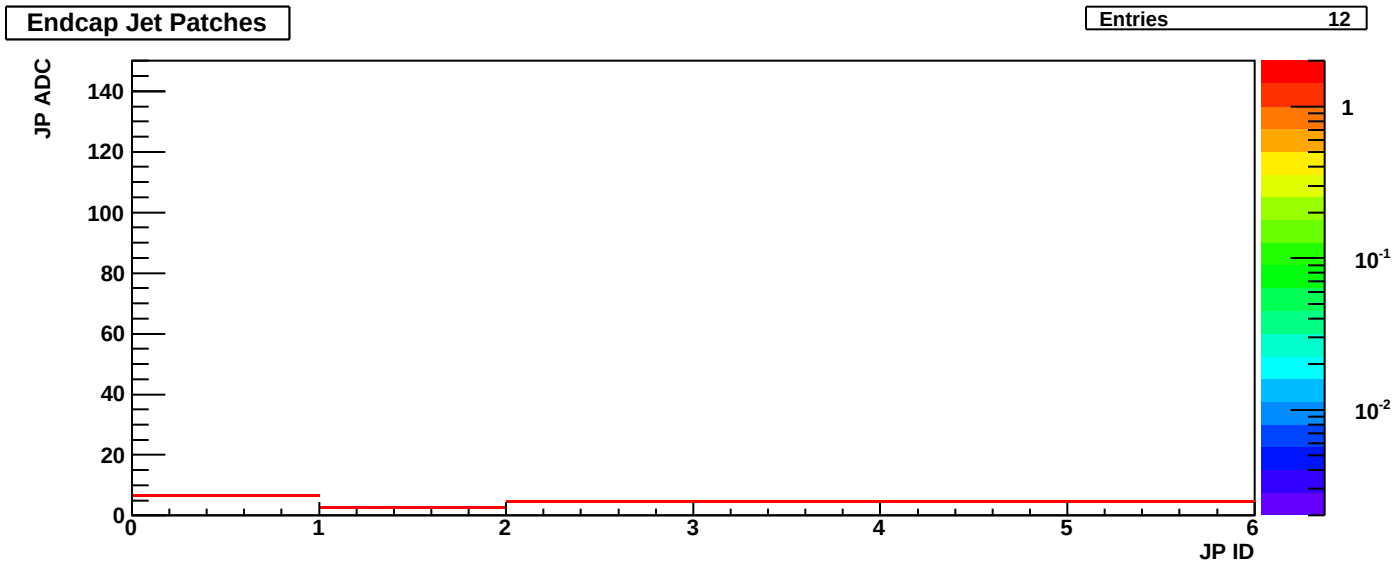

Barrel EMC L0 Input - High Tower
Entries 600
High Tower
Trigger Patch
0
10
20
30
40
50
60
0
50
100
150
200
250
300
1

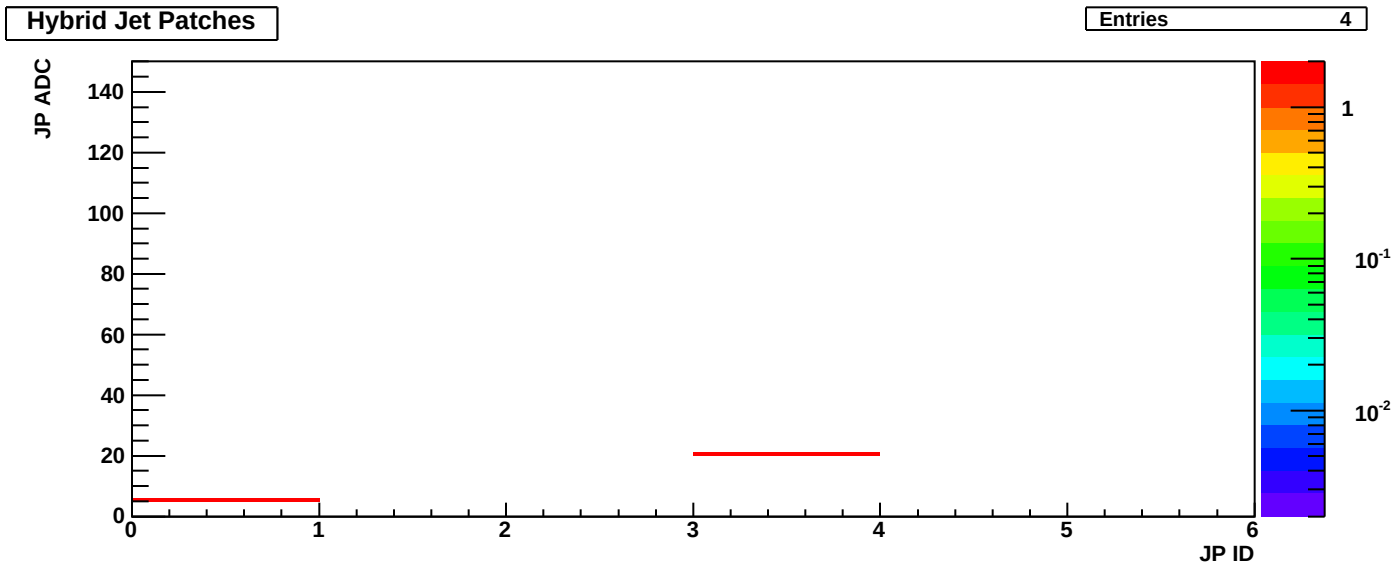

Barrel EMC L0 Input - Patch Sum
Entries 600
Patch Sum
Trigger Patch
0
10
20
30
40
50
60
0
50
100
150
200
250
300
1

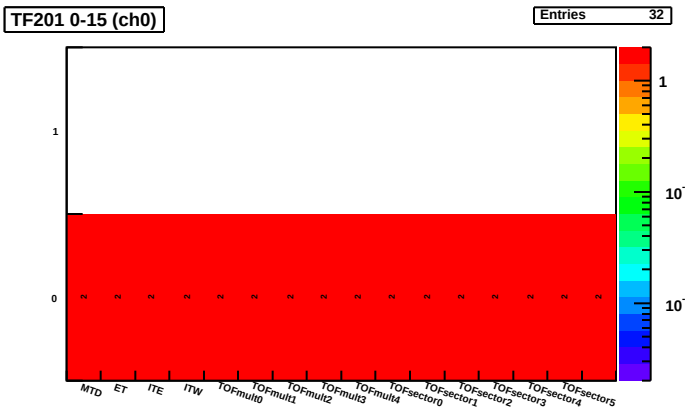

Endcap EMC L0 Input - High Tower
Entries 180
High Tower
crate 3
crate 4
crate 5
crate 6
crate 1
crate 2
Trigger Patch

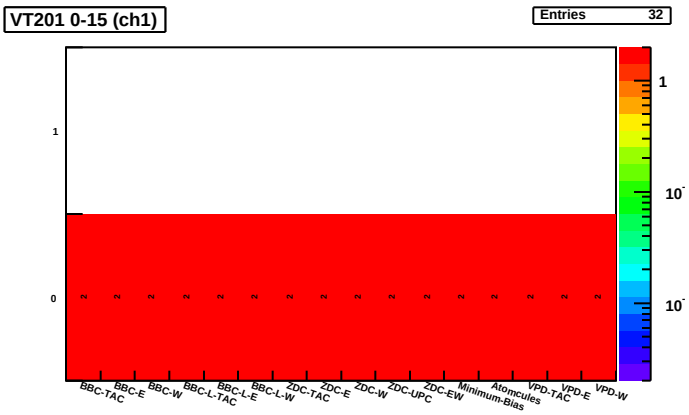

Endcap EMC L0 Input - Patch Sum
Entries 180
Patch Sum
crate 3
crate 4
crate 5
crate 6
crate 1
crate 2
Trigger Patch

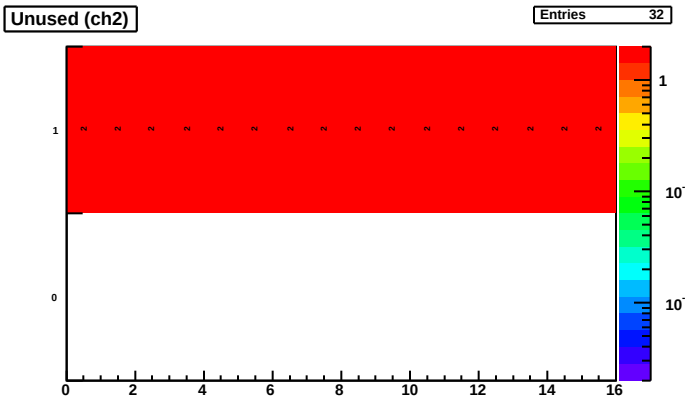

Barrel Jet Patches
Entries 36
JP ADC
JP ID

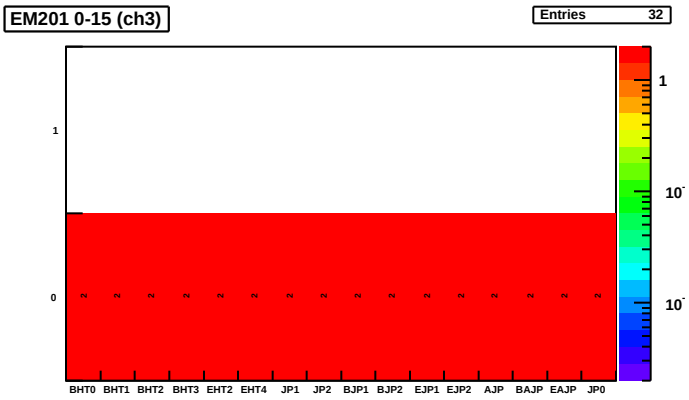

Endcap Jet Patches
Entries 12
JP ADC
JP ID

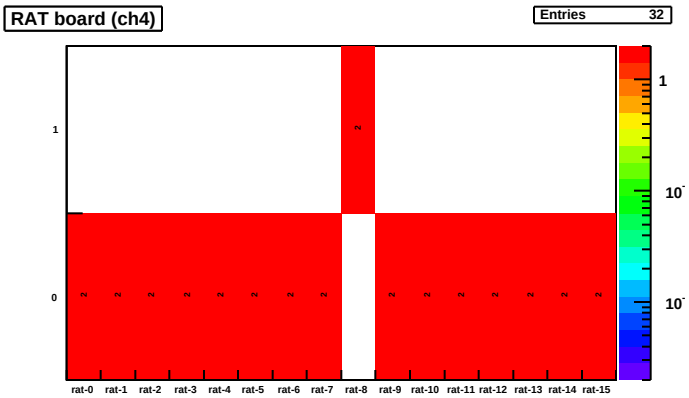

Hybrid Jet Patches
Entries 4
JP ADC
JP ID

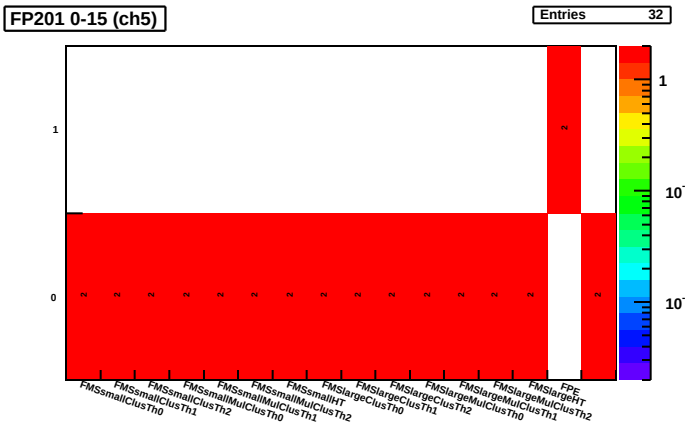

TF201 0-15 (ch0)
Entries 32
MTD ET ITE ITW TOFmult0 TOFmult1 TOFmult2 TOFmult3 TOFmult4 TOFsector0 TOFsector1 TOFsector2 TOFsector3 TOFsector4 TOFsector5

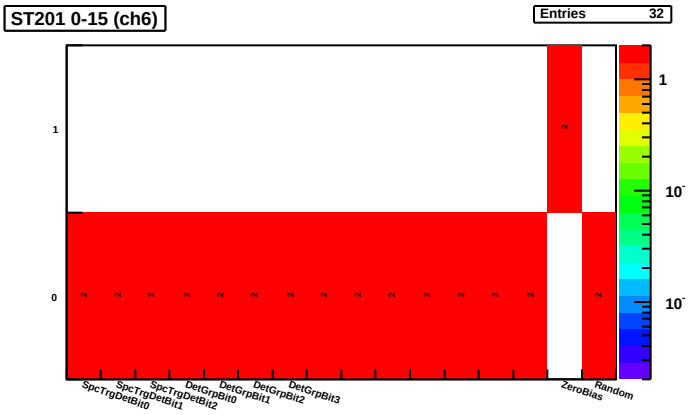

VT201 0-15 (ch1)
Entries 32
BBC-TAC BBC-E BBC-W BBC-L-TAC BBC-L-E BBC-L-W ZDC-TAC ZDC-E ZDC-W ZDC-UPC ZDC-EW Minimum-Bias Atomcules VPD-TAC VPD-E VPD-W

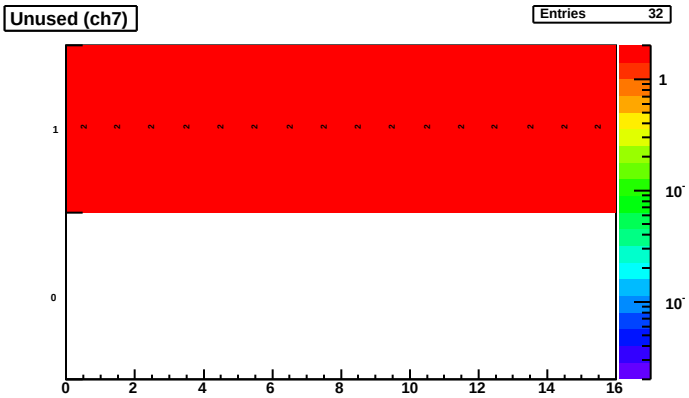

Unused (ch2)
Entries 32

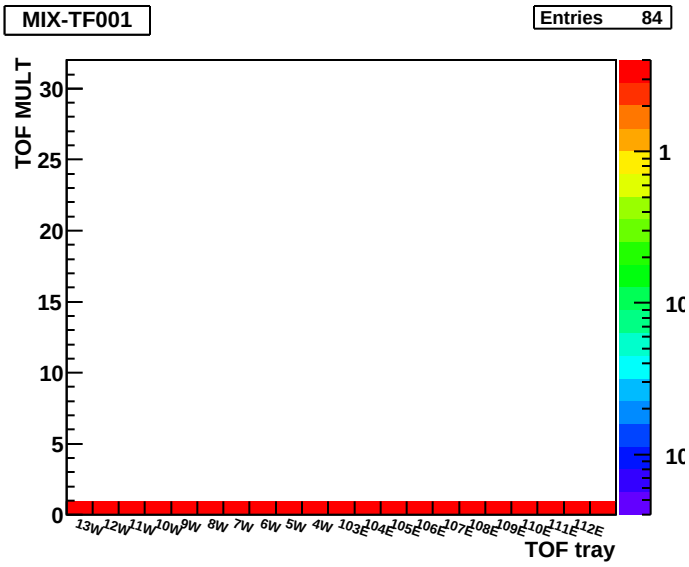

EM201 0-15 (ch3)
Entries 32
BHT0 BHT1 BHT2 BHT3 EHT2 EHT4 JP1 JP2 BJP1 BJP2 EJP1 EJP2 AJP BAJP EAJP JP0

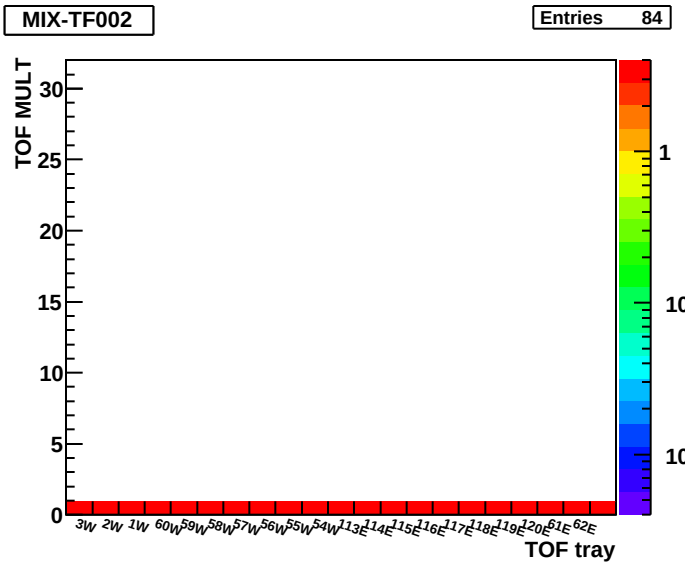

RAT board (ch4)
Entries 32
rat-0 rat-1 rat-2 rat-3 rat-4 rat-5 rat-6 rat-7 rat-8 rat-9 rat-10 rat-11 rat-12 rat-13 rat-14 rat-15

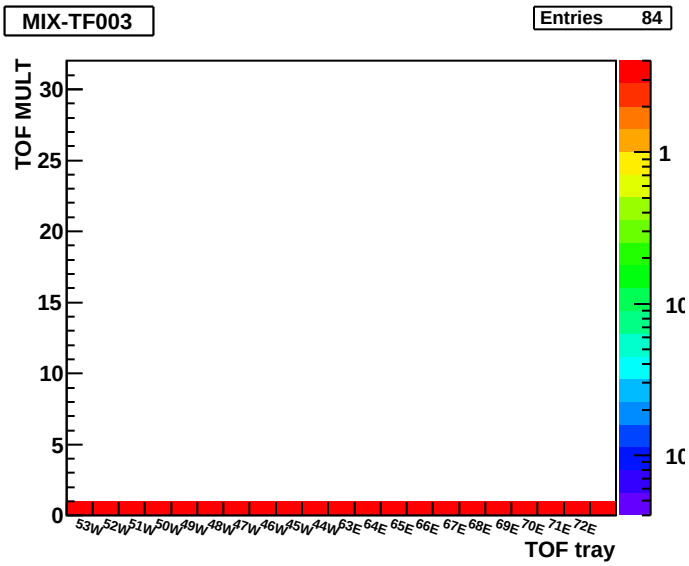

FP201 0-15 (ch5)
Entries 32
FMSsmallClusTh0 FMSsmallClusTh1 FMSsmallClusTh2 FMSsmallMulClusTh0 FMSsmallMulClusTh1 FMSsmallMulClusTh2 FMSsmallHT FMSlargeClusTh0 FMSlargeClusTh1 FMSlargeClusTh2 FMSlargeMulClusTh0 FMSlargeMulClusTh1 FMSlargeMulClusTh2 FMSlargeHT FPE

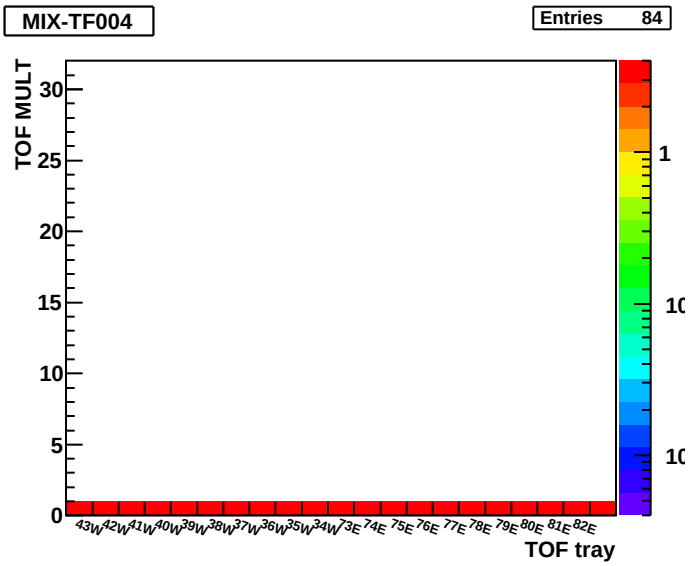

ST201 0-15 (ch6)
Entries 32
SpcTrgDetBit0 SpcTrgDetBit1 SpcTrgDetBit2 DetGrpBit0 DetGrpBit1 DetGrpBit2 DetGrpBit3 ZeroBias Random

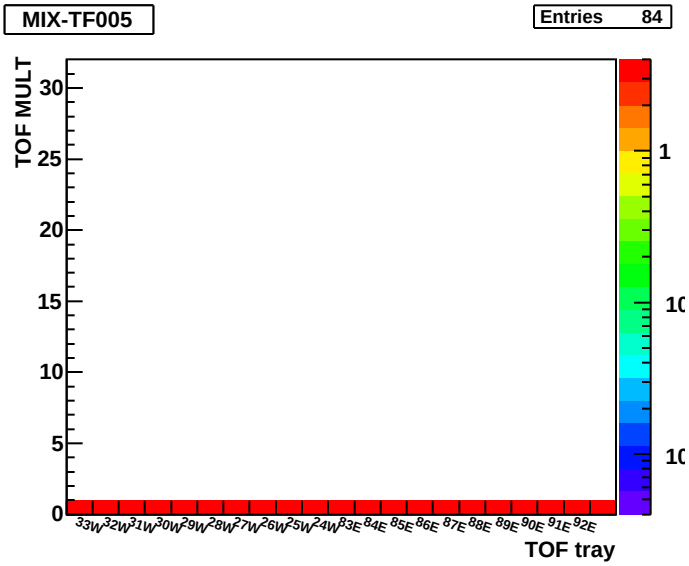

Unused (ch7)
Entries 32

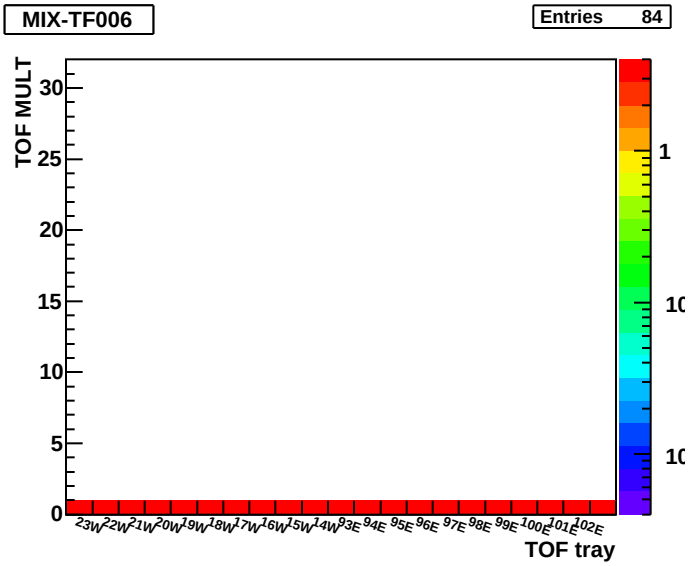

MIX-TF001
Entries 84
TOF MULT
TOF tray

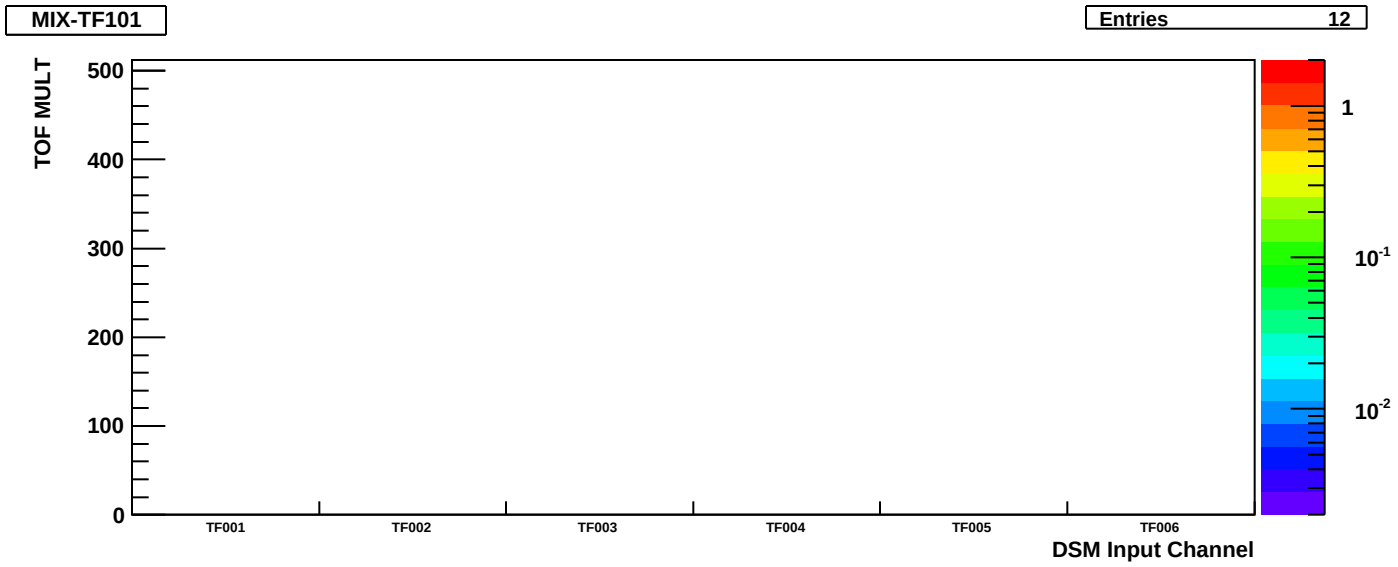

MIX-TF002
Entries 84
TOF MULT
TOF tray

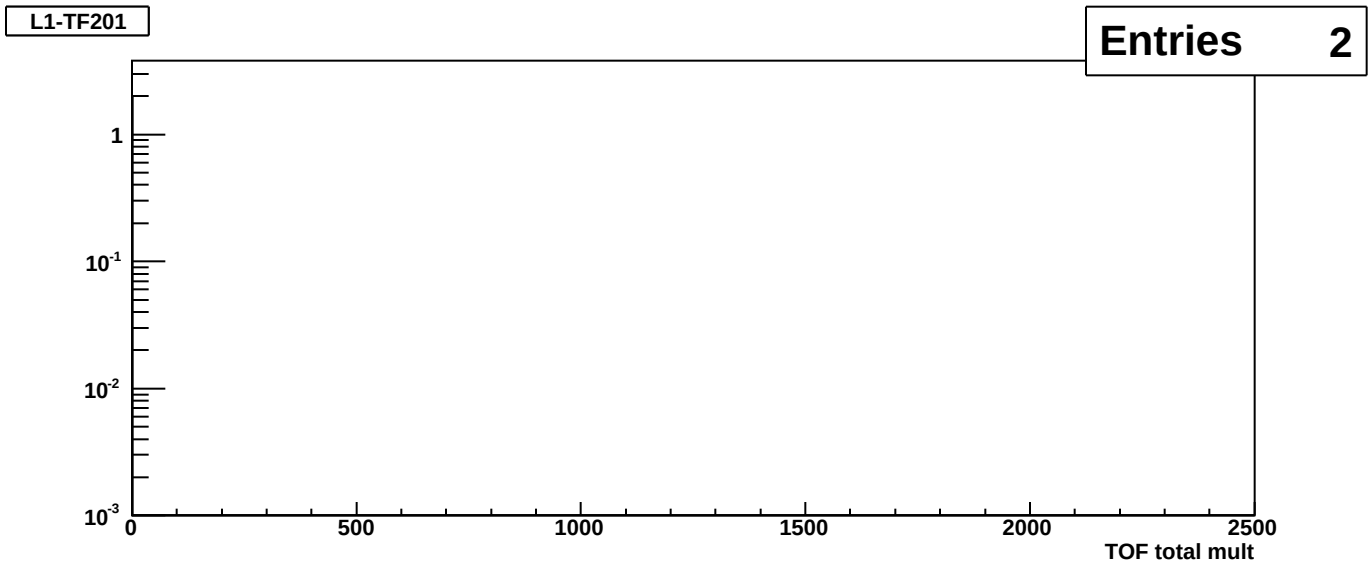

MIX-TF003
Entries 84
TOF MULT
TOF tray

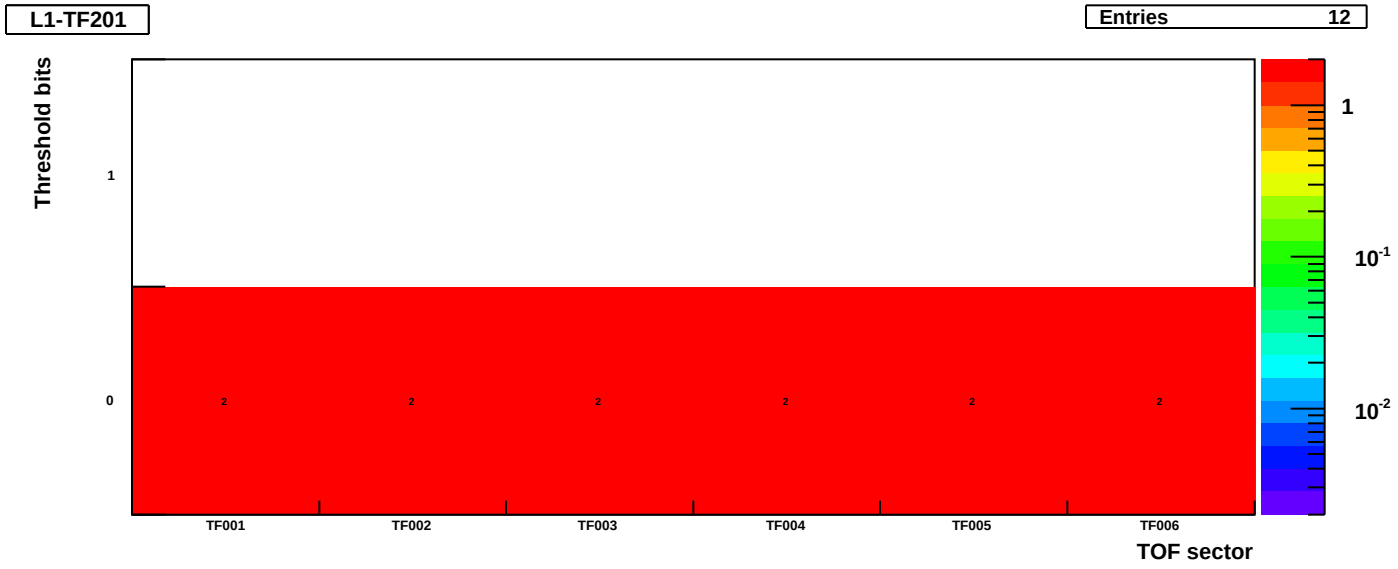

MIX-TF004
Entries 84
TOF MULT
TOF tray

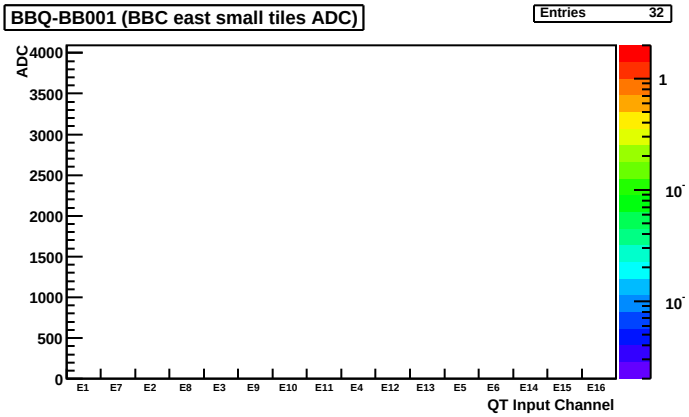

MIX-TF005
Entries 84
TOF MULT
TOF tray

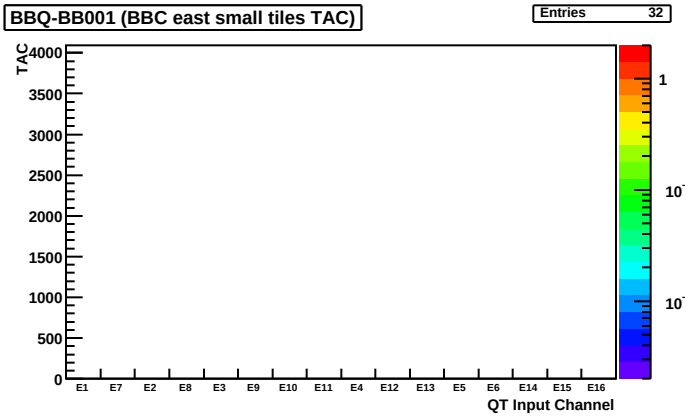

MIX-TF006
Entries 84
TOF MULT
TOF tray

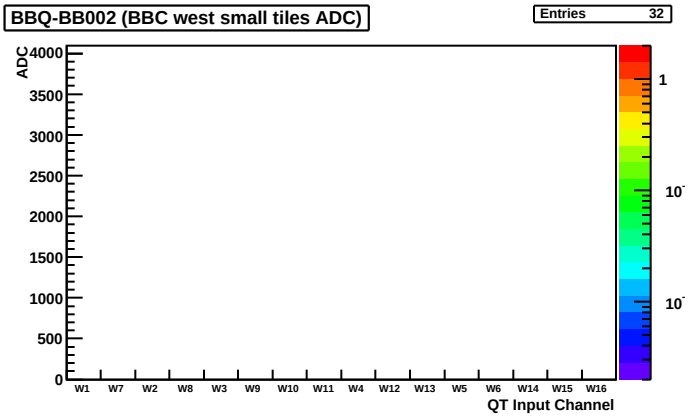

MIX-TF101
Entries 12
TOF MULT
500
400
300
200
100
0
TF001
TF002
TF003
TF004
TF005
TF006
DSM Input Channel
1
10-1
10-2

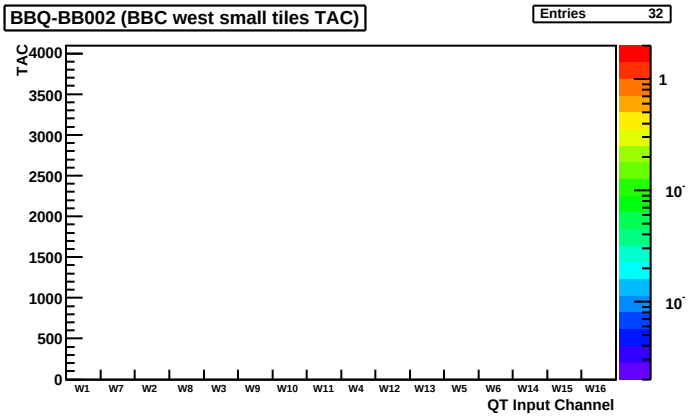

L1-TF201
Entries 2
1
10-1
10-2
10-3
0
500
1000
1500
2000
2500
TOF total mult

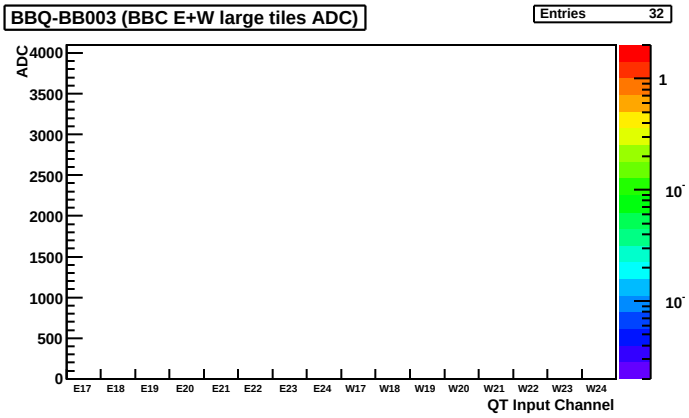

L1-TF201
Entries 12
Threshold bits
1
0
2
TF001
TF002
TF003
TF004
TF005
TF006
TOF sector
1
10-1
10-2

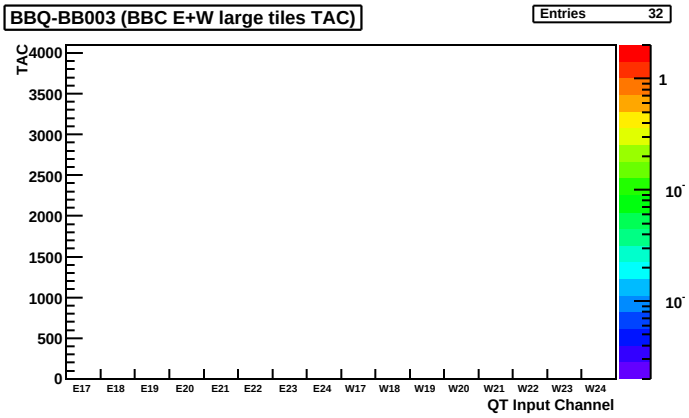

BBQ-BB001 (BBC east small tiles ADC)
Entries 32
ADC
QT Input Channel

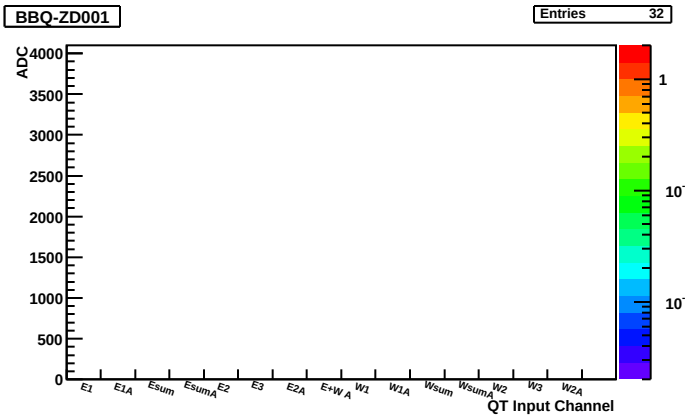

BBQ-BB001 (BBC east small tiles TAC)
Entries 32
TAC
QT Input Channel

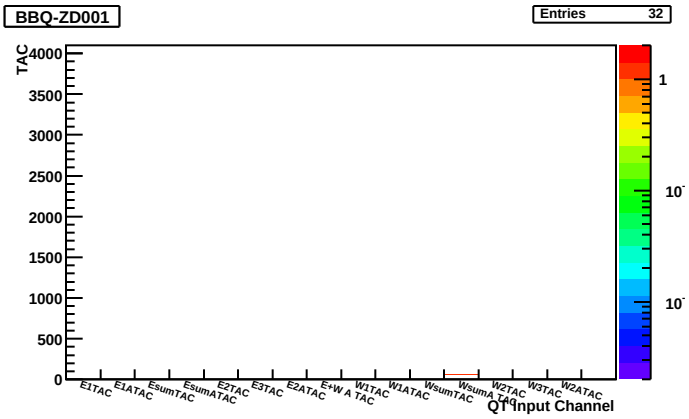

BBQ-BB002 (BBC west small tiles ADC)
Entries 32
ADC
QT Input Channel

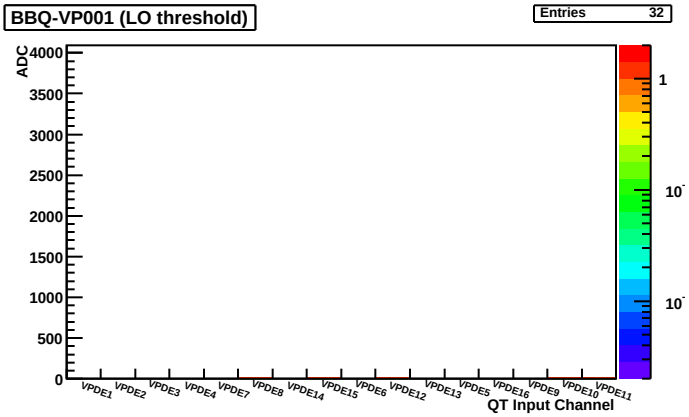

BBQ-BB002 (BBC west small tiles TAC)
Entries 32
TAC
QT Input Channel

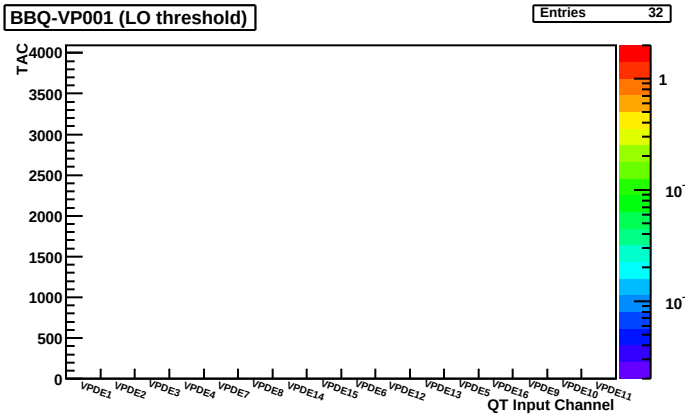

BBQ-BB003 (BBC E+W large tiles ADC)
Entries 32
ADC
QT Input Channel

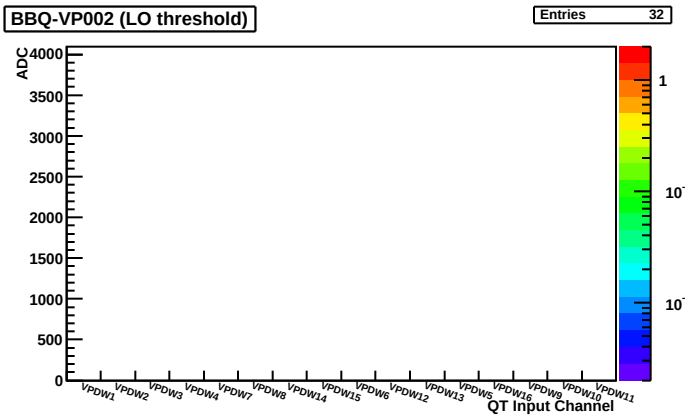

BBQ-BB003 (BBC E+W large tiles TAC)
Entries 32
TAC
QT Input Channel

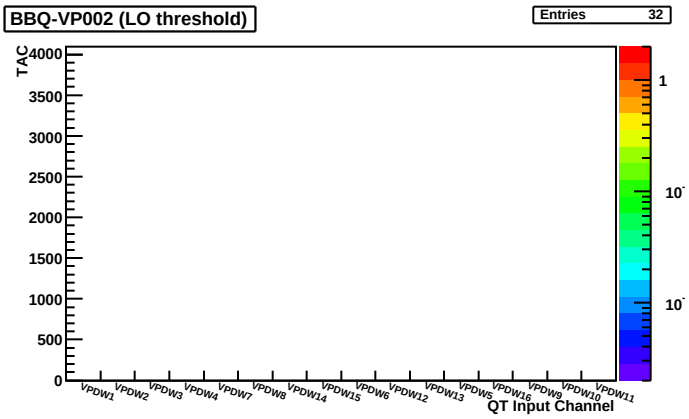

BBQ-ZD001
Entries 32
ADC
QT Input Channel

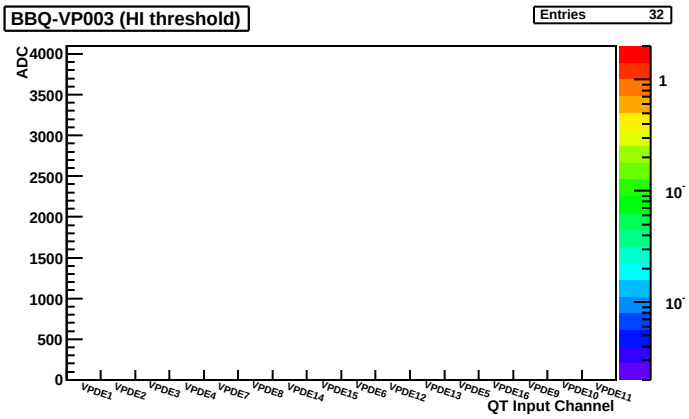

BBQ-ZD001
Entries 32
TAC
QT Input Channel

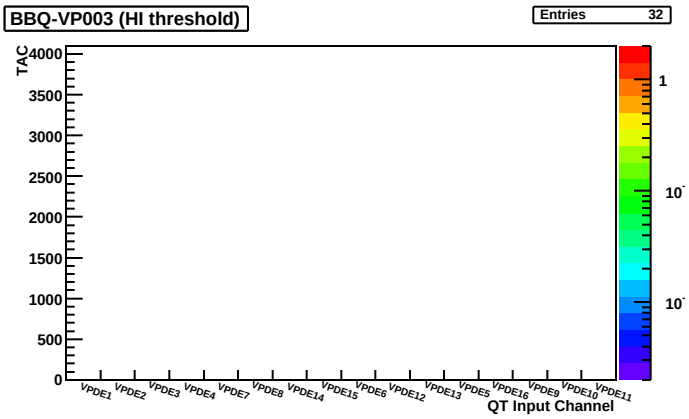

BBQ-VP001 (LO threshold)
Entries 32
ADC
QT Input Channel

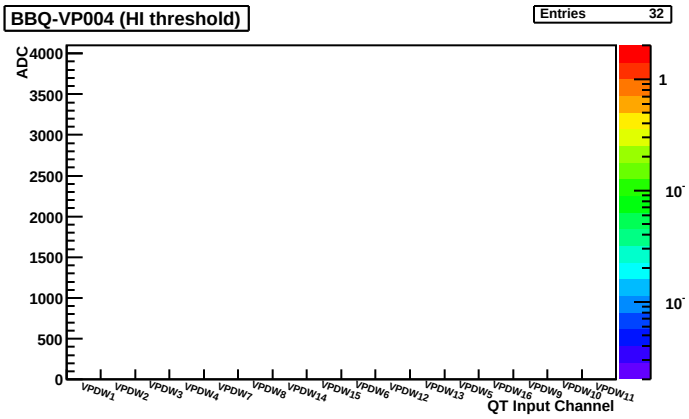

BBQ-VP001 (LO threshold)
Entries 32
TAC
QT Input Channel

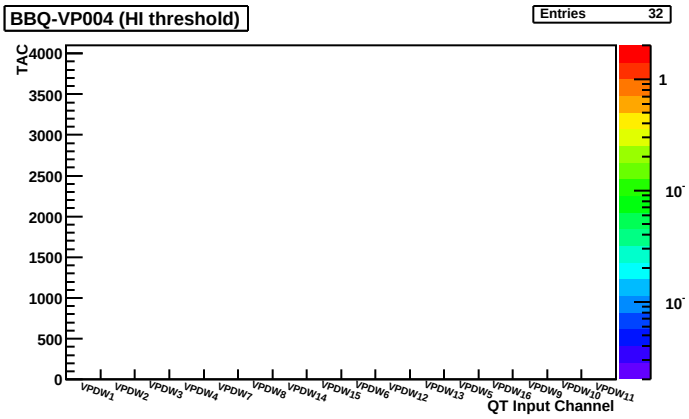

BBQ-VP002 (LO threshold)
Entries 32
ADC
QT Input Channel

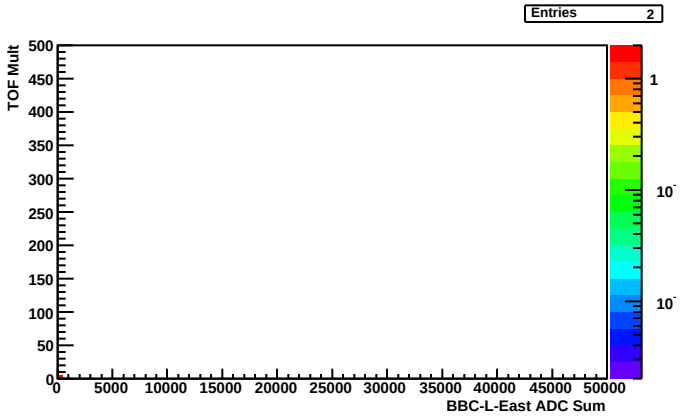

BBQ-VP002 (LO threshold)
Entries 32
TAC
QT Input Channel

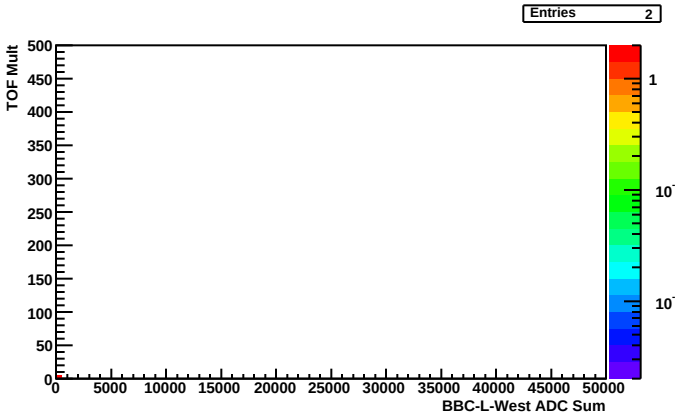

BBQ-VP003 (HI threshold)
Entries 32
ADC
QT Input Channel

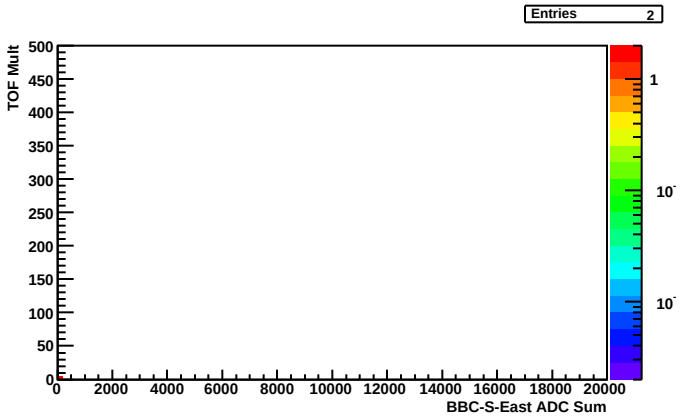

BBQ-VP003 (HI threshold)
Entries 32
TAC
QT Input Channel

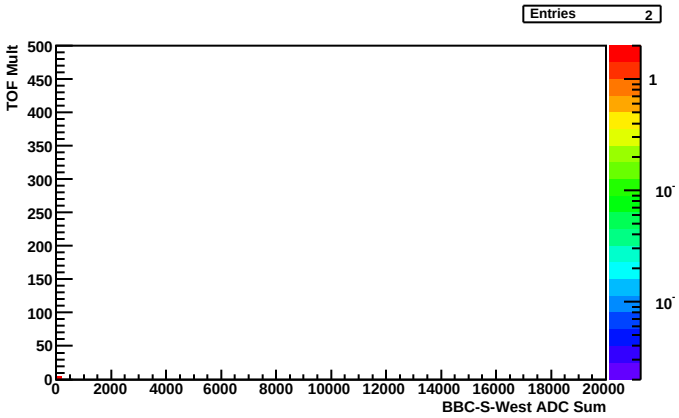

BBQ-VP004 (HI threshold)
Entries 32
ADC
QT Input Channel

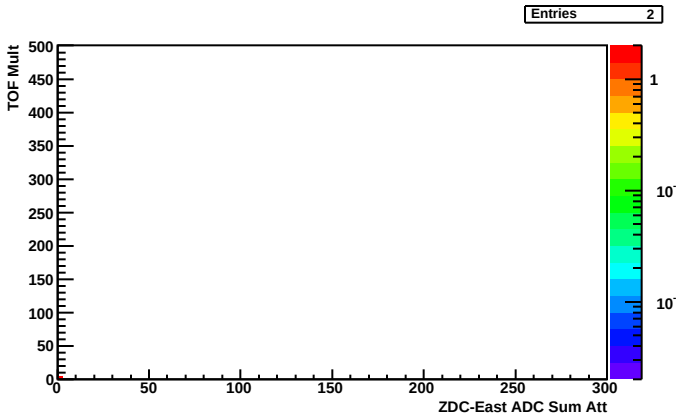

BBQ-VP004 (HI threshold)
Entries 32
TAC
QT Input Channel

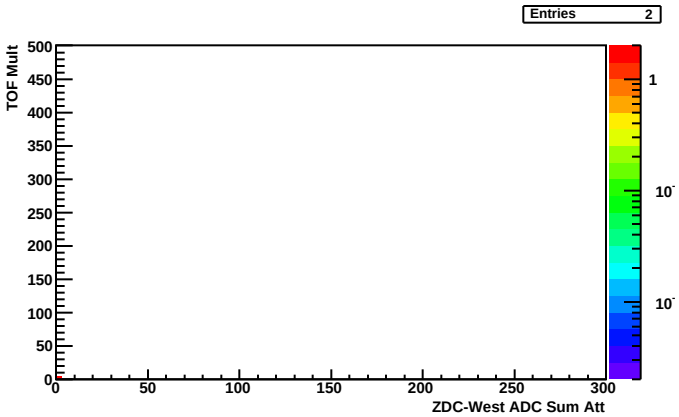

Entries 2
TOF Mult
BBC-L-East ADC Sum

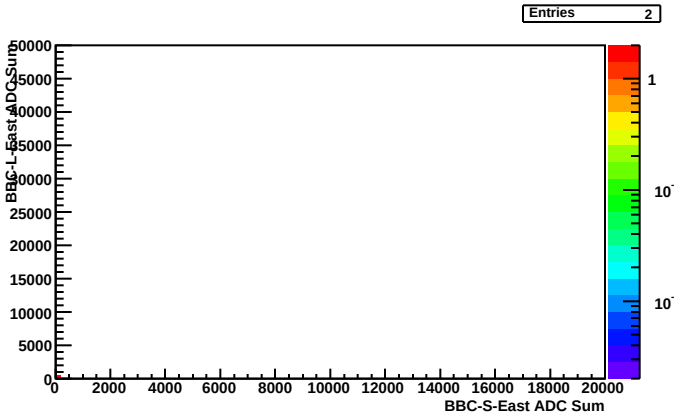

Entries 2
TOF Mult
BBC-L-West ADC Sum

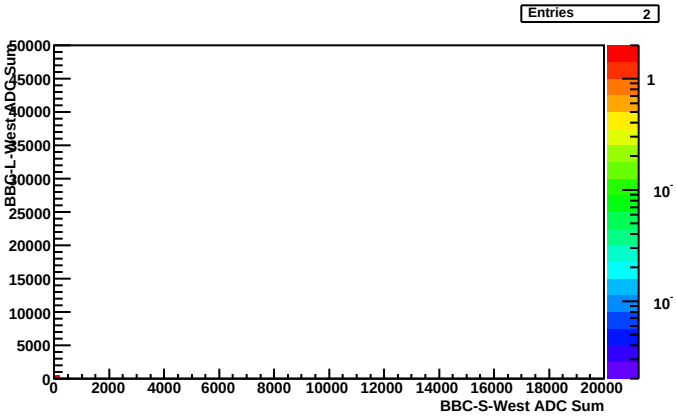

Entries 2
TOF Mult
BBC-S-East ADC Sum

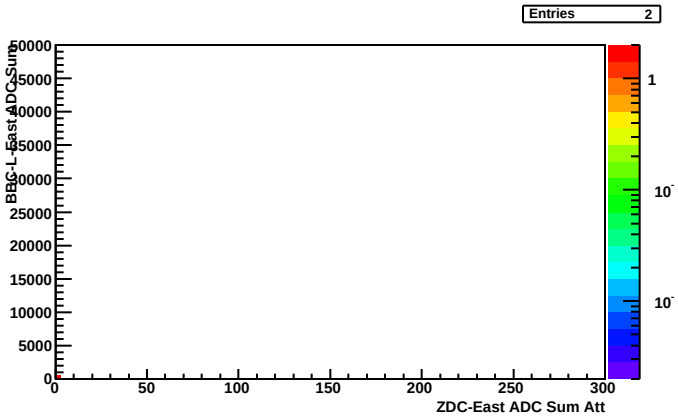

Entries 2
TOF Mult
BBC-S-West ADC Sum

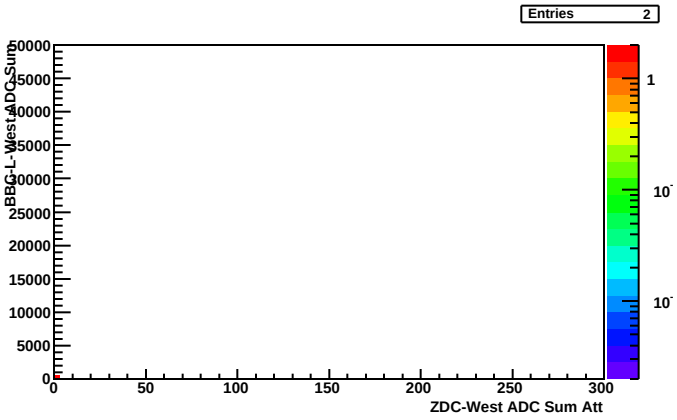

Entries 2
TOF Mult
ZDC-East ADC Sum Att

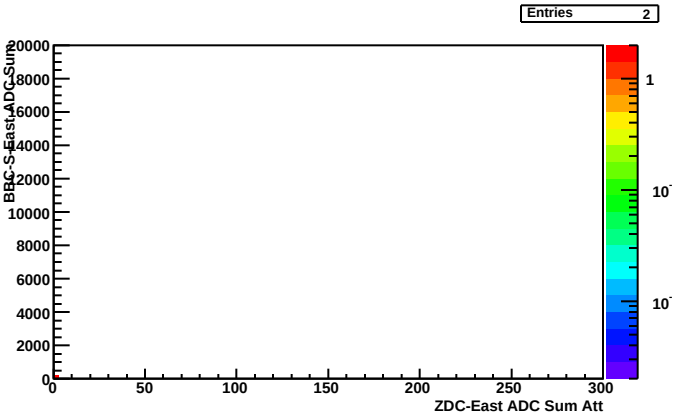

Entries 2
TOF Mult
ZDC-West ADC Sum Att

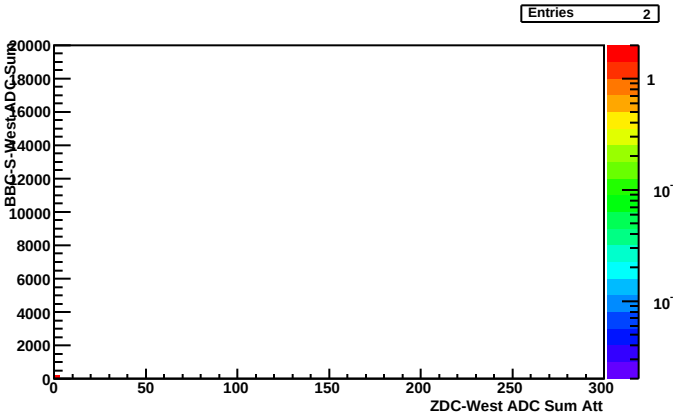

Entries 2
BBC-L-East ADC Sum
BBC-S-East ADC Sum

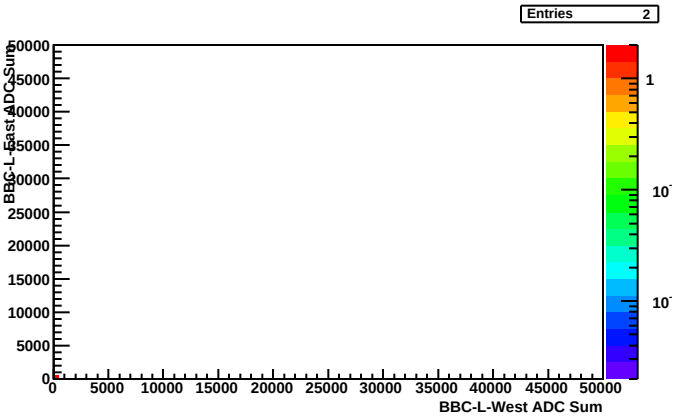

Entries 2
BBC-L-West ADC Sum
BBC-S-West ADC Sum

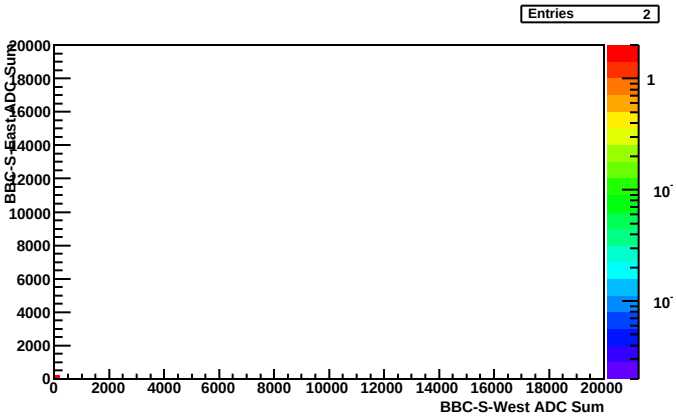

Entries 2
BBC-L-East ADC Sum
ZDC-East ADC Sum Att

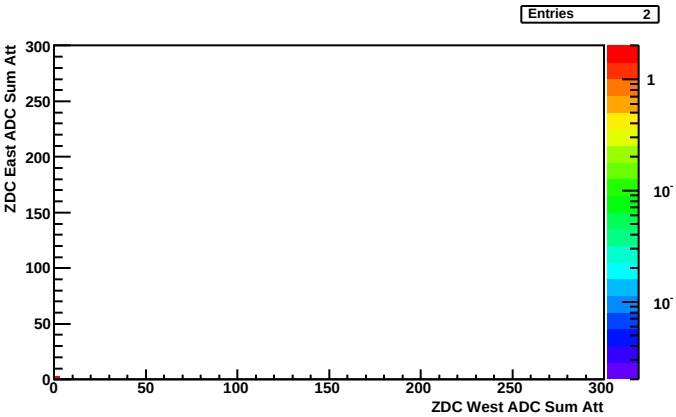

Entries 2
BBC-L-West ADC Sum
ZDC-West ADC Sum Att

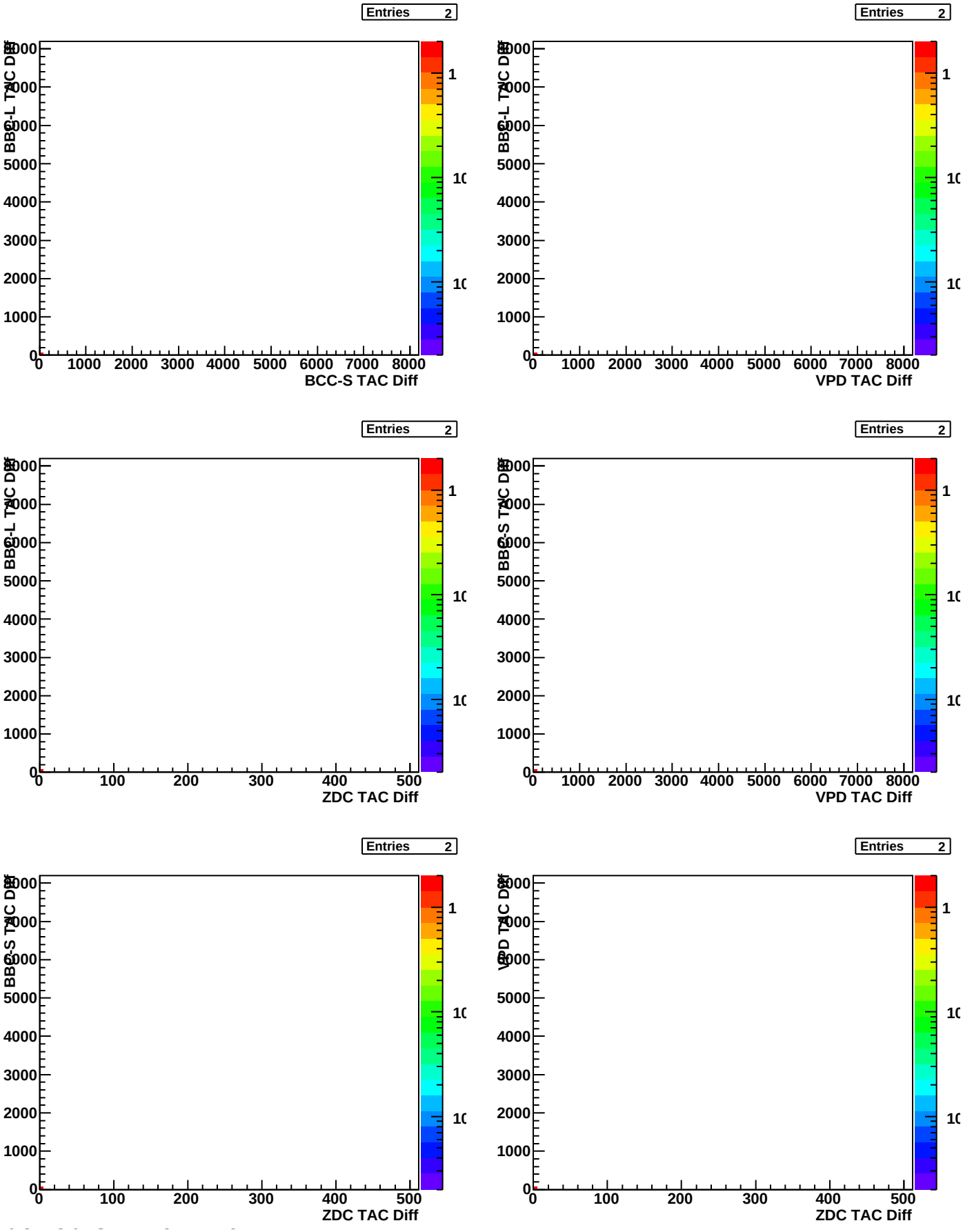

Entries 2
BBC-S-East ADC Sum
ZDC-East ADC Sum Att

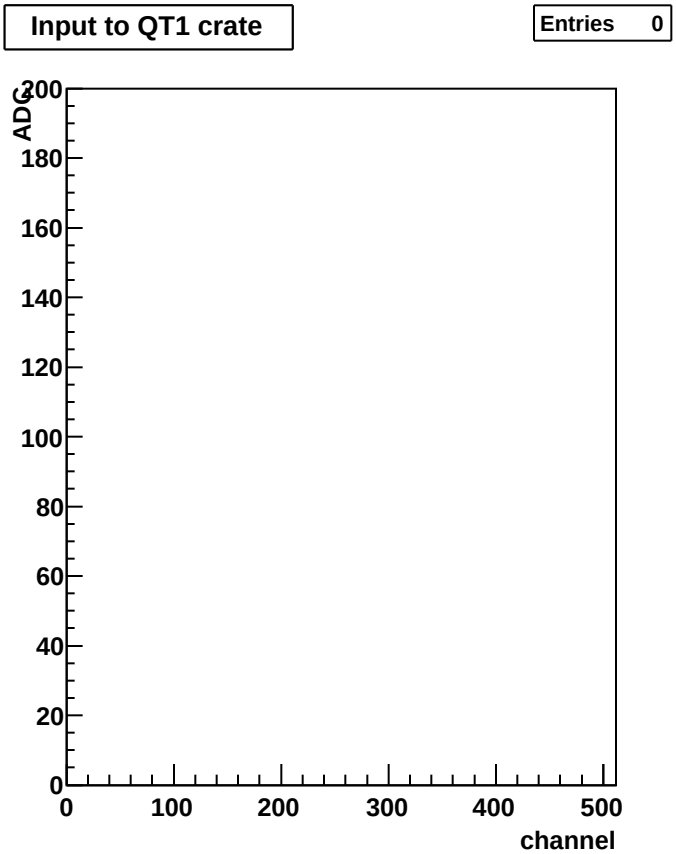

Entries 2
BBC-S-West ADC Sum
ZDC-West ADC Sum Att

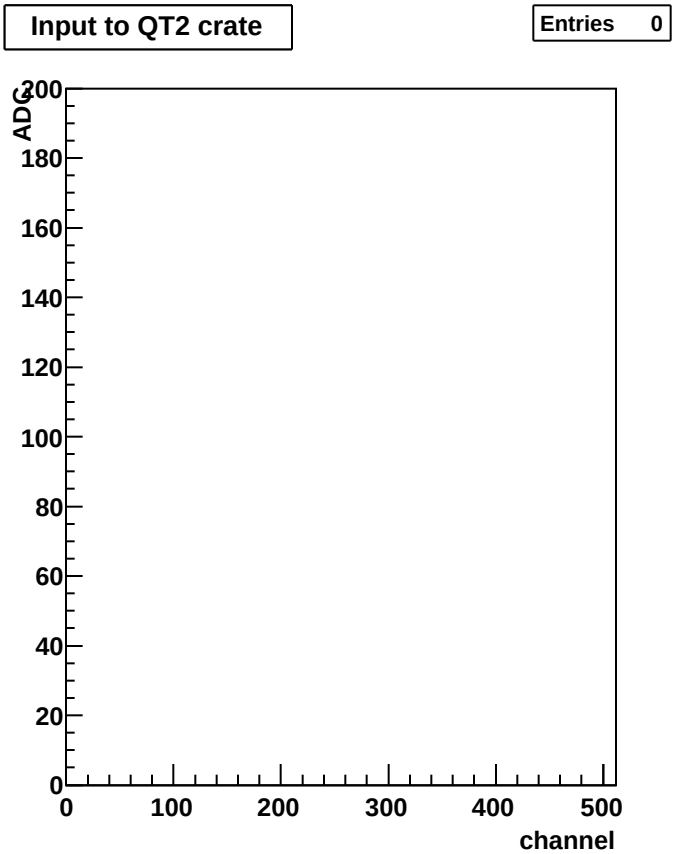

Entries 2
BBC-L-East ADC Sum
BBC-L-West ADC Sum

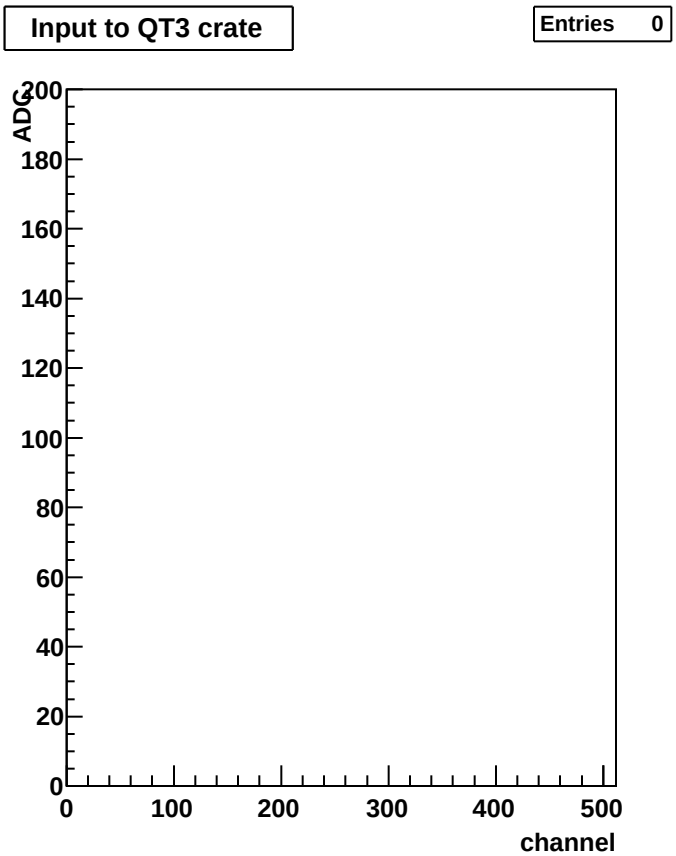

Entries 2
BBC-S-East ADC Sum
BBC-S-West ADC Sum

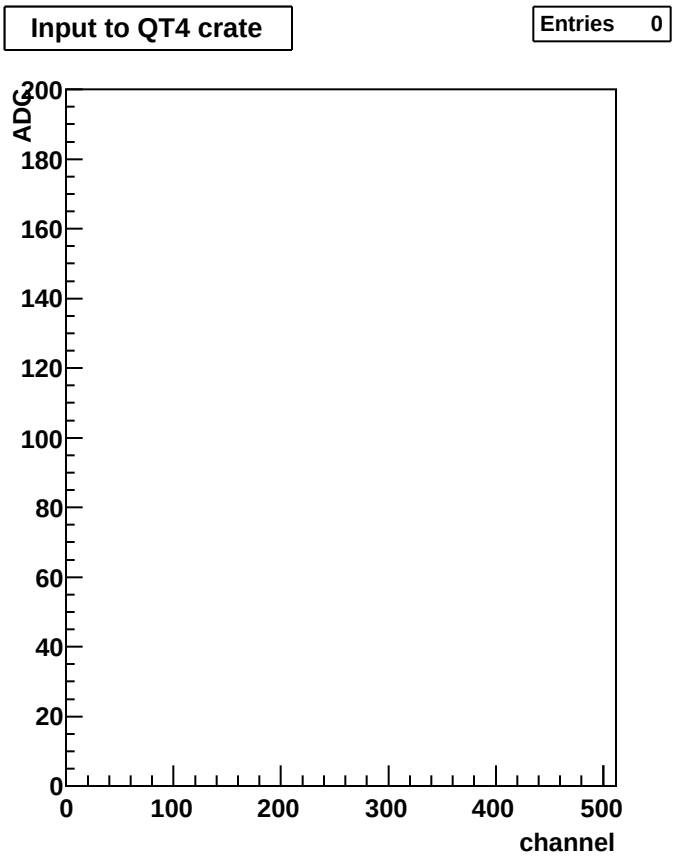

Entries 2
ZDC East ADC Sum Att
ZDC West ADC Sum Att

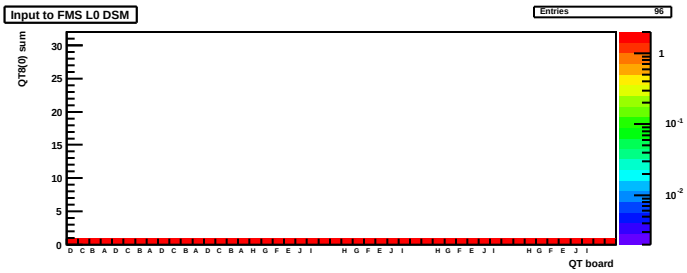

Entries 2
BBC-L TAC Diff
BCC-S TAC Diff
Entries 2
BBC-L TAC Diff
VPD TAC Diff
Entries 2
BBC-L TAC Diff
ZDC TAC Diff
Entries 2
BBC-S TAC Diff
VPD TAC Diff
Entries 2
BBC-S TAC Diff
ZDC TAC Diff
Entries 2
VPD TAC Diff
ZDC TAC Diff

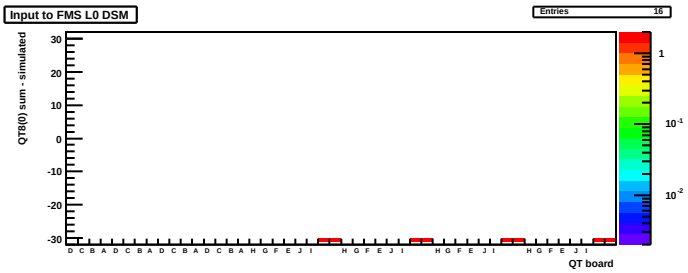

Input to QT1 crate
Entries 0
ADC
200
180
160
140
120
100
80
60
40
20
0
0
100
200
300
400
500
channel

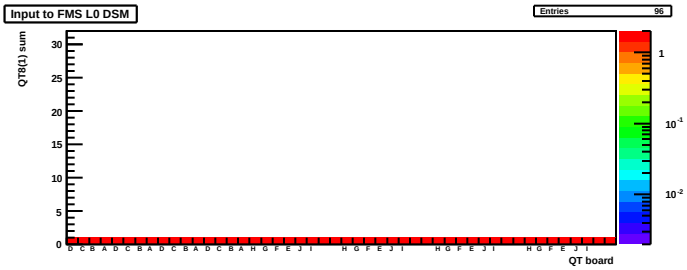

Input to QT2 crate
Entries 0
ADC
200
180
160
140
120
100
80
60
40
20
0
0
100
200
300
400
500
channel

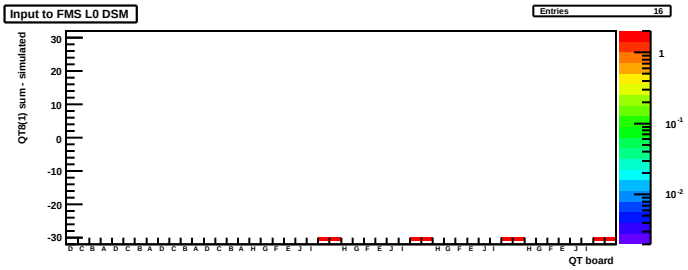

Input to QT3 crate
Entries 0
ADC
200
180
160
140
120
100
80
60
40
20
0
0
100
200
300
400
500
channel

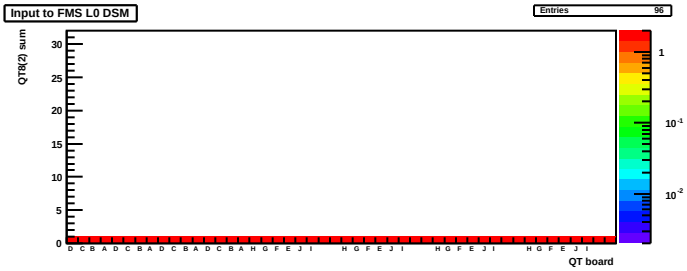

Input to QT4 crate
Entries 0
ADC
200
180
160
140
120
100
80
60
40
20
0
0
100
200
300
400
500
channel

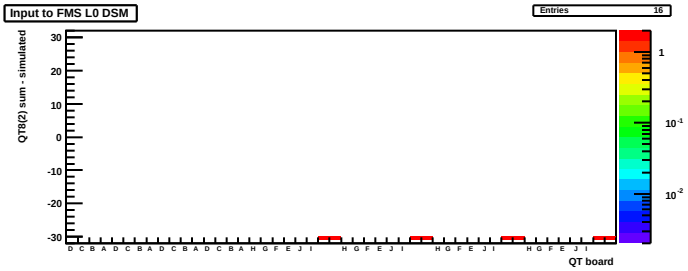

Input to FMS L0 DSM
Entries 96
QT8(0) sum
QT board

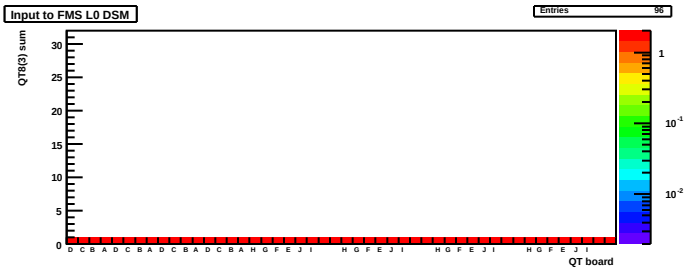

Input to FMS L0 DSM
Entries 16
QT8(0) sum - simulated
QT board

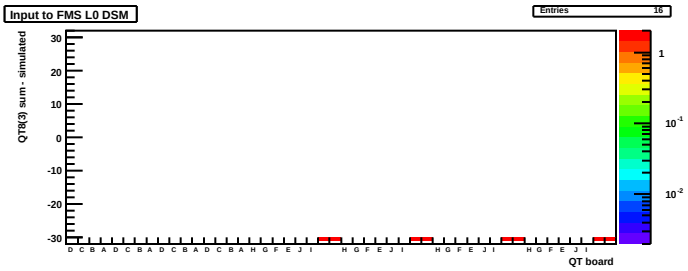

Input to FMS L0 DSM
Entries 96
QT8(1) sum
QT board

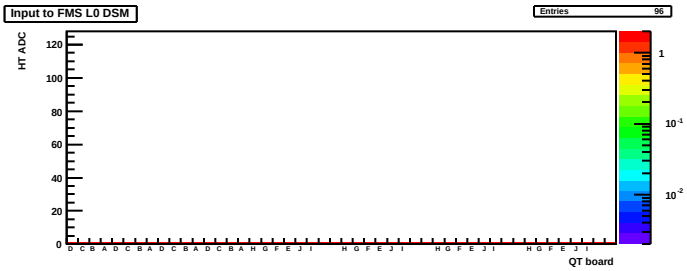

Input to FMS L0 DSM
Entries 16
QT8(1) sum - simulated
QT board

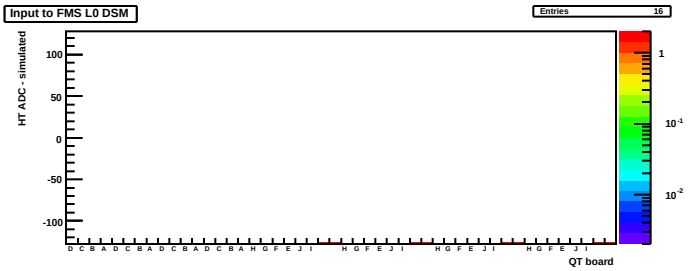

Input to FMS L0 DSM
Entries 96
QT8(2) sum
QT board

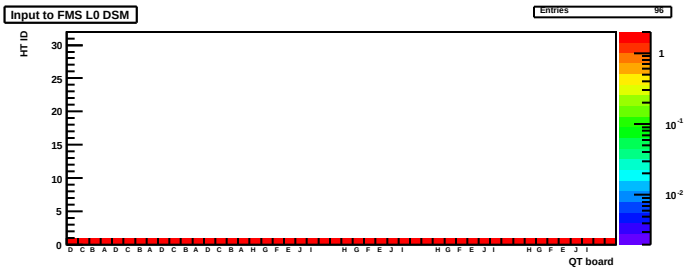

Input to FMS L0 DSM
Entries 16
QT8(2) sum - simulated
QT board

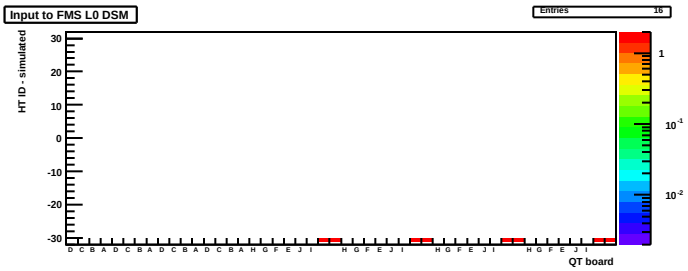

Input to FMS L0 DSM
Entries 96
QT8(3) sum
QT board

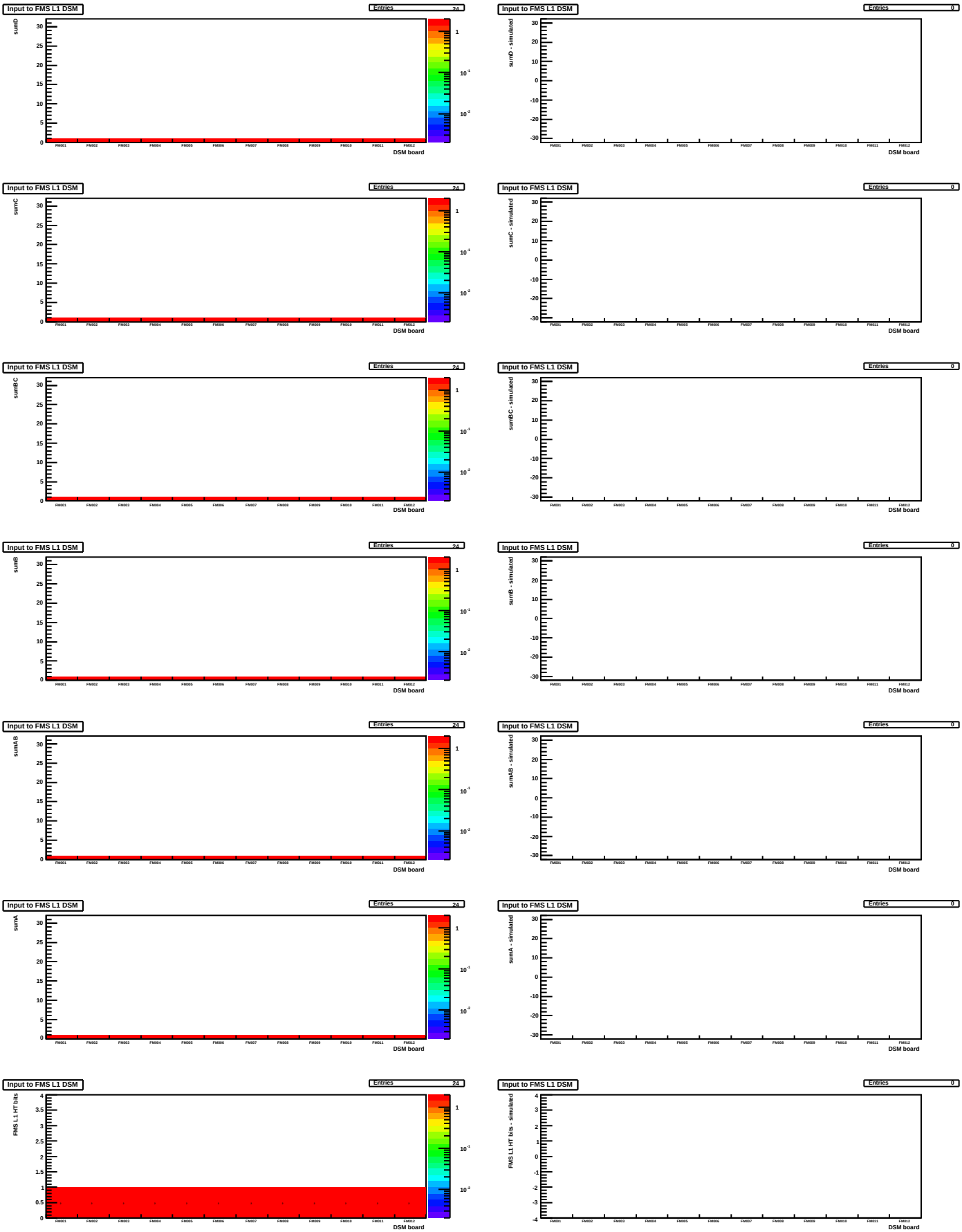

Input to FMS L0 DSM
Entries 16
QT8(3) sum - simulated
QT board

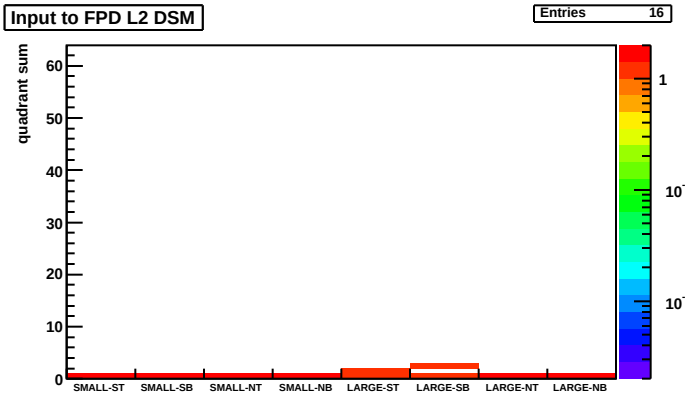

Input to FMS L0 DSM
Entries 96
HT ADC
QT board

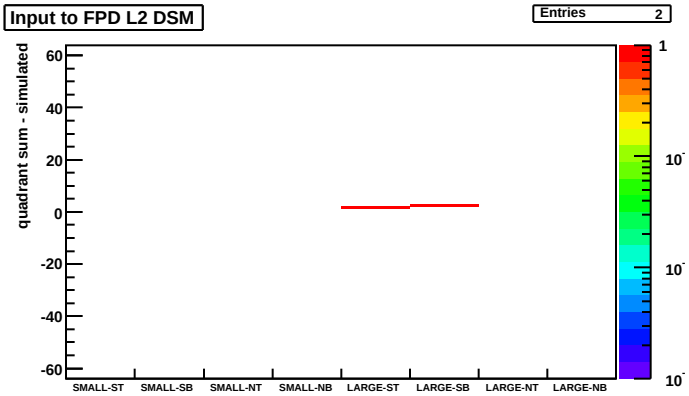

Input to FMS L0 DSM
Entries 16
HT ADC - simulated
QT board

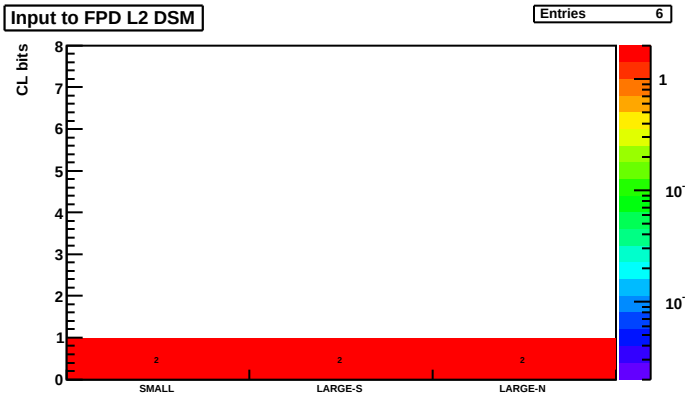

Input to FMS L0 DSM
Entries 96
HT ID
QT board

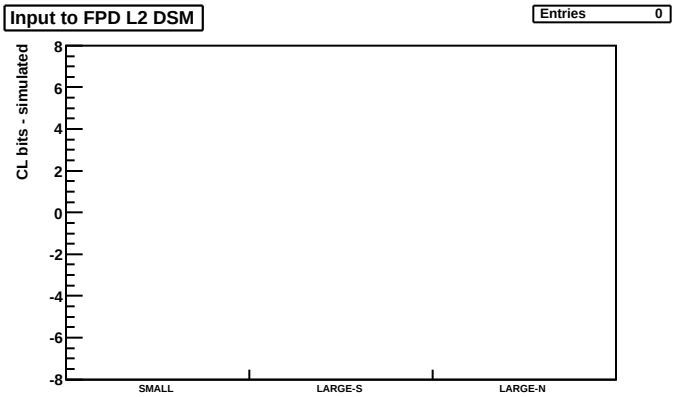

Input to FMS L0 DSM
Entries 16
HT ID - simulated
QT board

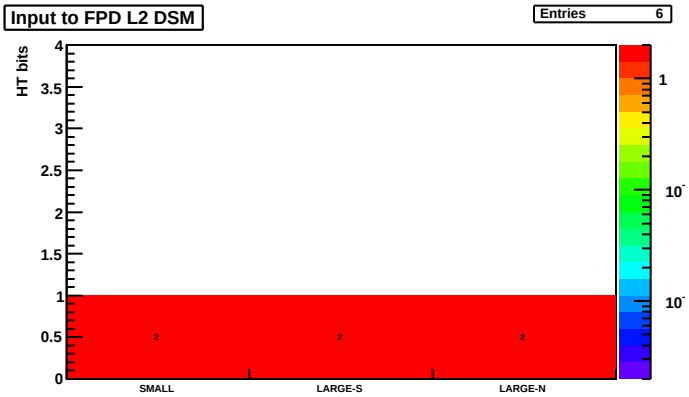

Input to FMS L1 DSM
Entries 24
sumD
sumD - simulated
sumC
sumC - simulated
sumBC
sumBC - simulated
sumB
sumB - simulated
sumAB
sumAB - simulated
sumA
sumA - simulated
FMS L1 HT bits
FMS L1 HT bits - simulated
Entries 0
DSM board

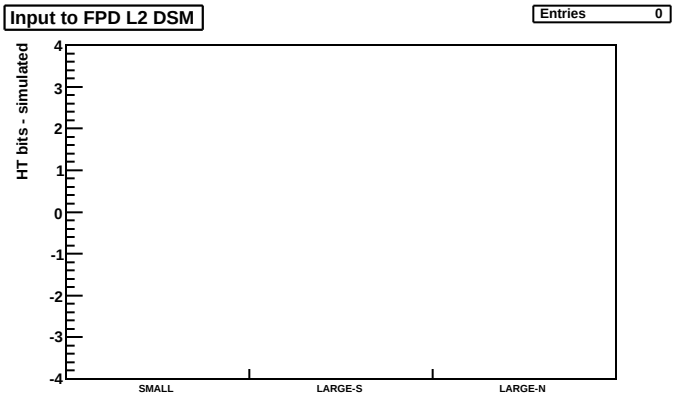

Input to FPD L2 DSM
Entries 16
quadrant sum
SMALL-ST
SMALL-SB
SMALL-NT
SMALL-NB
LARGE-ST
LARGE-SB
LARGE-NT
LARGE-NB

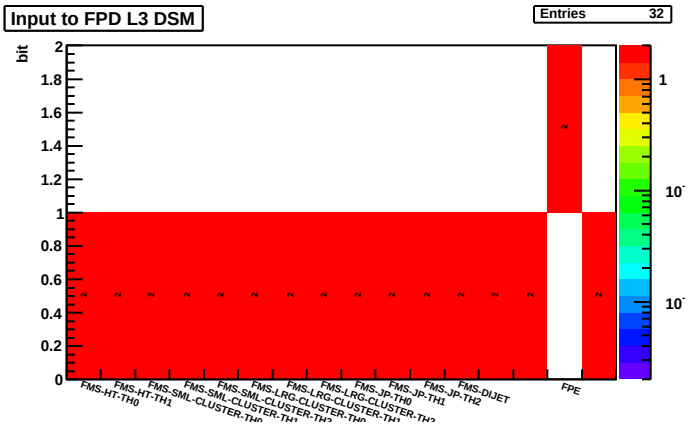

Input to FPD L2 DSM
Entries 2
quadrant sum - simulated
SMALL-ST
SMALL-SB
SMALL-NT
SMALL-NB
LARGE-ST
LARGE-SB
LARGE-NT
LARGE-NB

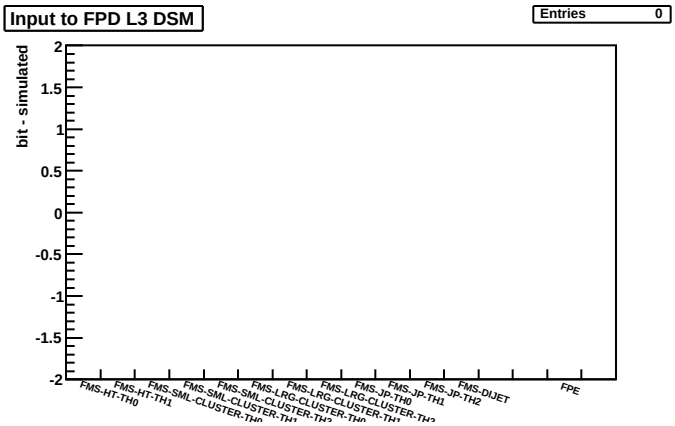

Input to FPD L2 DSM
Entries 6
CL bits
SMALL
LARGE-S
LARGE-N

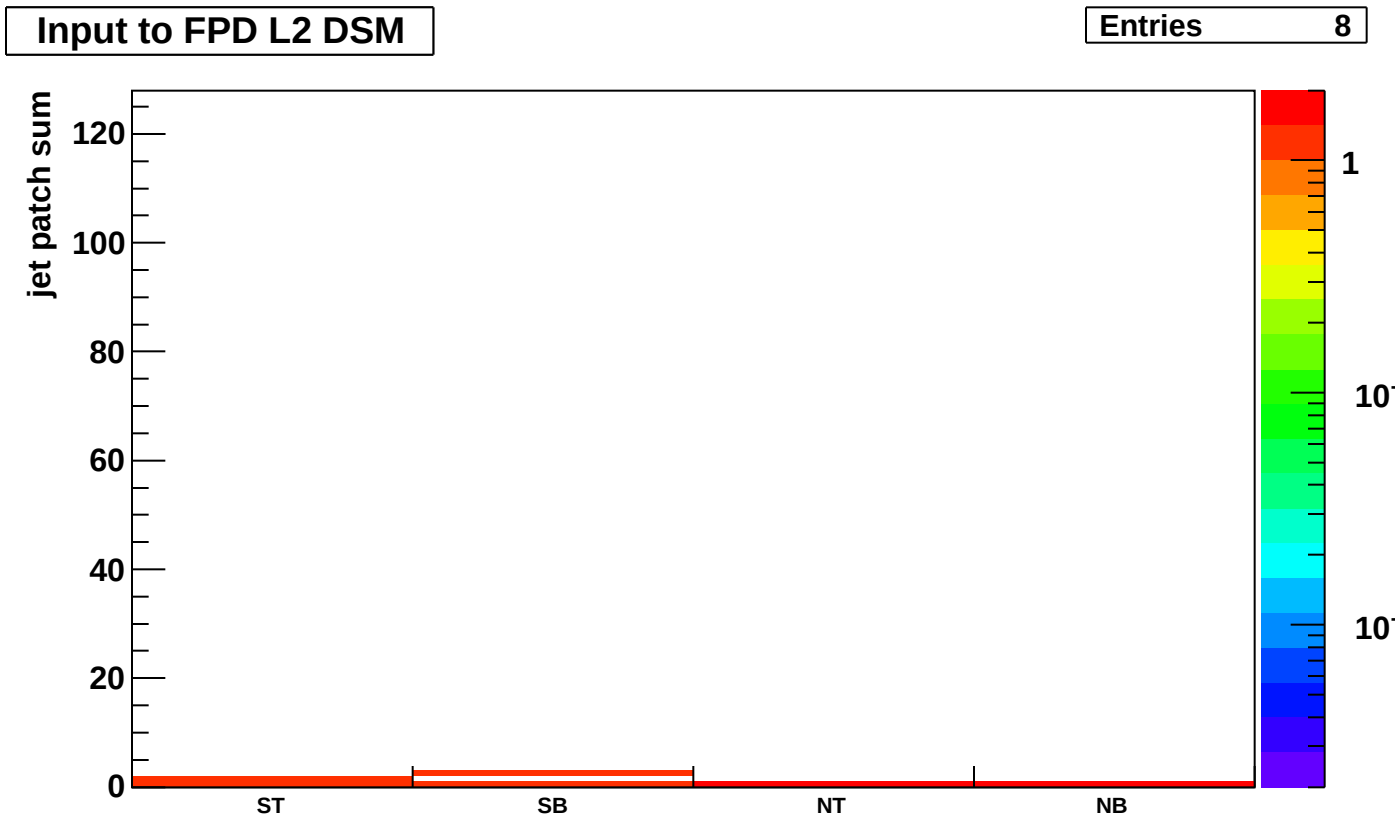

Input to FPD L2 DSM
Entries 0
CL bits - simulated
SMALL
LARGE-S
LARGE-N

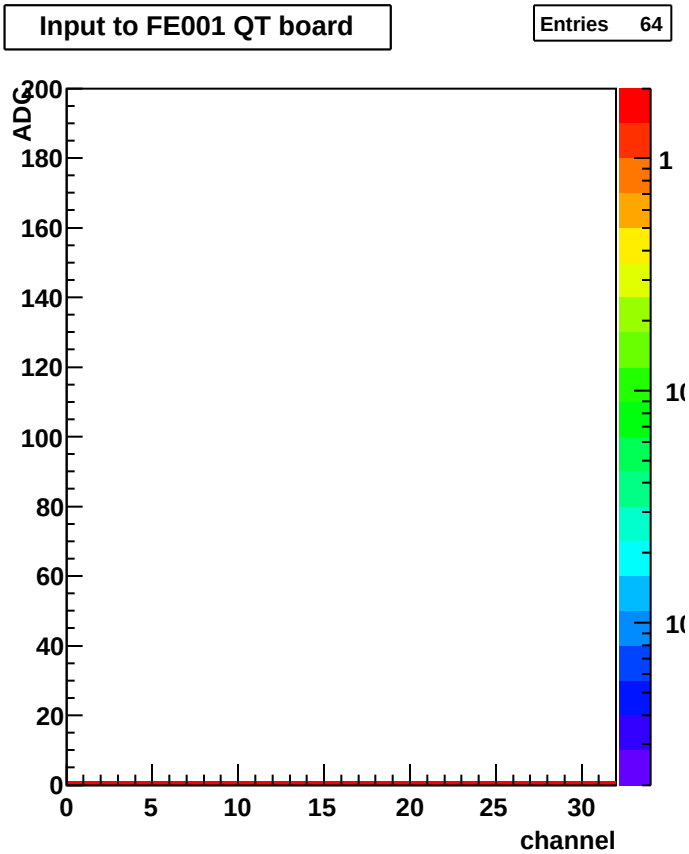

Input to FPD L2 DSM
Entries 6
HT bits
SMALL
LARGE-S
LARGE-N

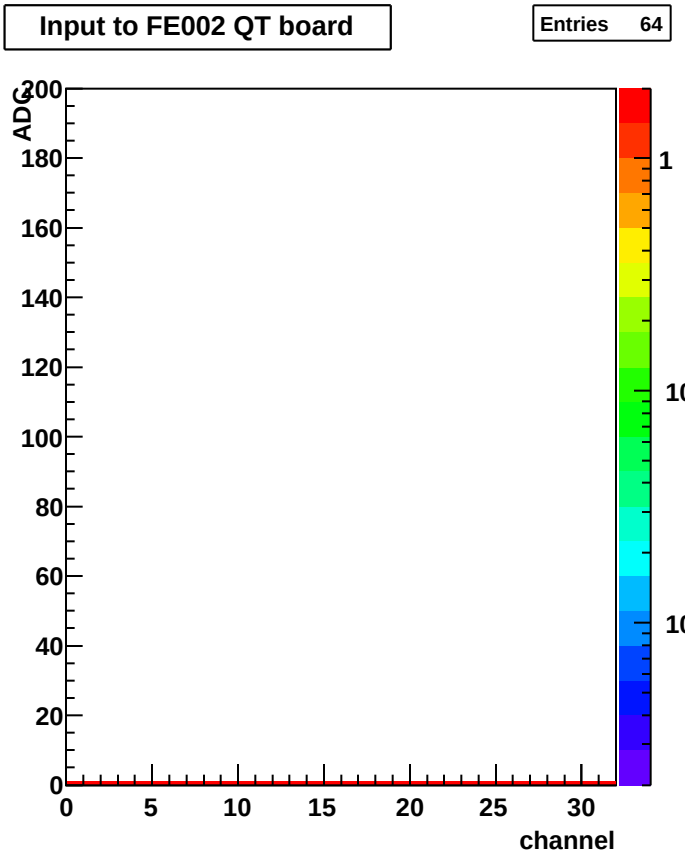

Input to FPD L2 DSM
Entries 0
HT bits - simulated
SMALL
LARGE-S
LARGE-N

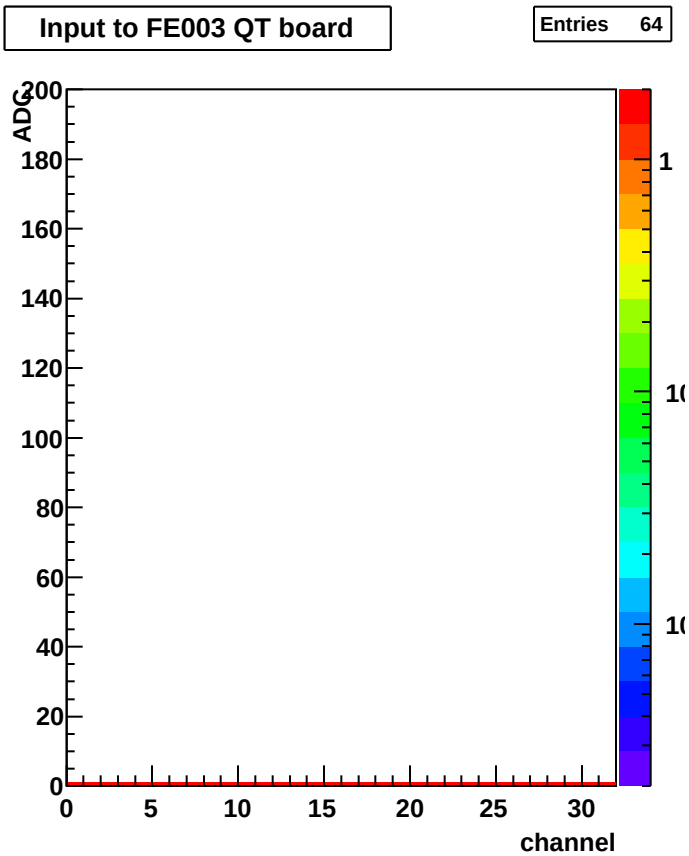

Input to FPD L3 DSM
Entries 32
bit
FMS-HT-TH0
FMS-HT-TH1
FMS-SML-CLUSTER-TH0
FMS-SML-CLUSTER-TH1
FMS-SML-CLUSTER-TH2
FMS-LRG-CLUSTER-TH0
FMS-LRG-CLUSTER-TH1
FMS-LRG-CLUSTER-TH2
FMS-JP-TH0
FMS-JP-TH1
FMS-JP-TH2
FMS-DIJET
FPE

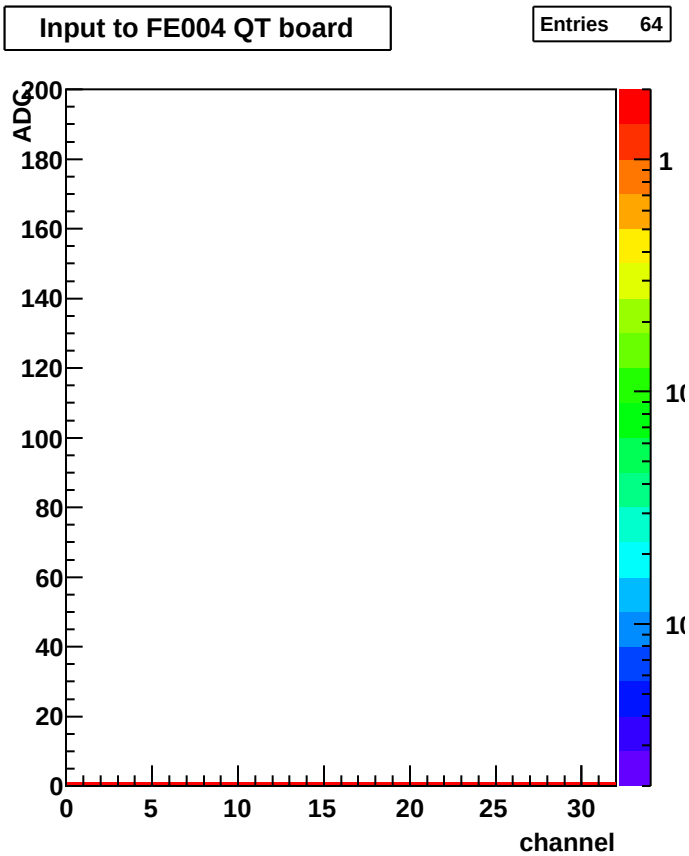

Input to FPD L3 DSM
Entries 0
bit - simulated
FMS-HT-TH0
FMS-HT-TH1
FMS-SML-CLUSTER-TH0
FMS-SML-CLUSTER-TH1
FMS-SML-CLUSTER-TH2
FMS-LRG-CLUSTER-TH0
FMS-LRG-CLUSTER-TH1
FMS-LRG-CLUSTER-TH2
FMS-JP-TH0
FMS-JP-TH1
FMS-JP-TH2
FMS-DIJET
FPE

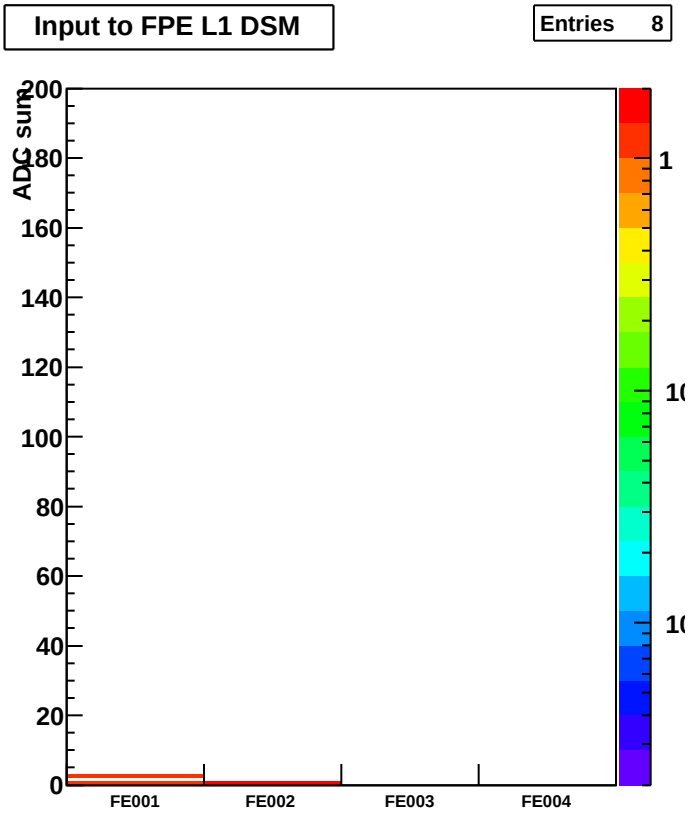

Input to FPD L2 DSM
Entries 8
jet patch sum
120
100
80
60
40
20
0
ST
SB
NT
NB
1

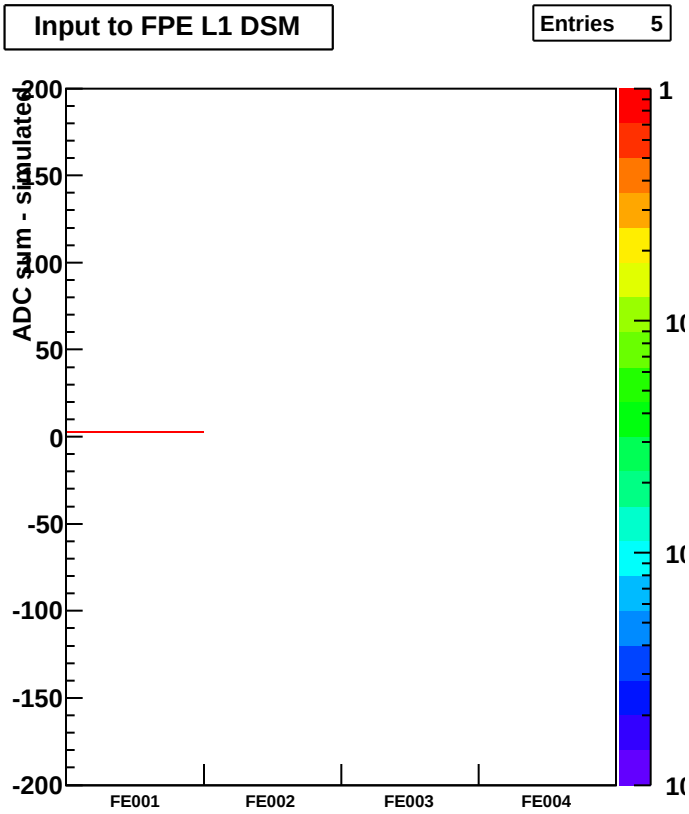

Input to FE001 QT board
Entries 64
ADC
channel

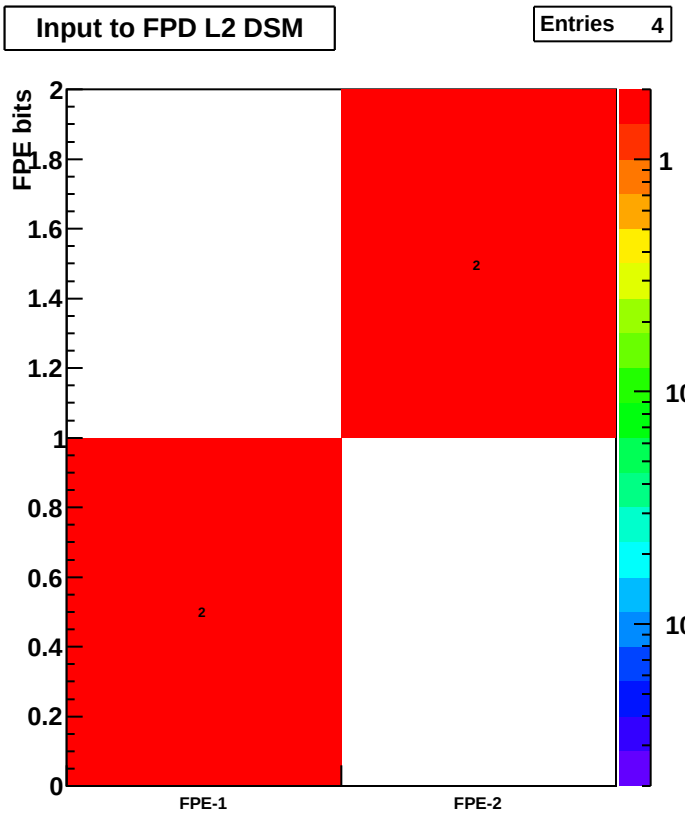

Input to FE002 QT board
Entries 64
ADC
channel

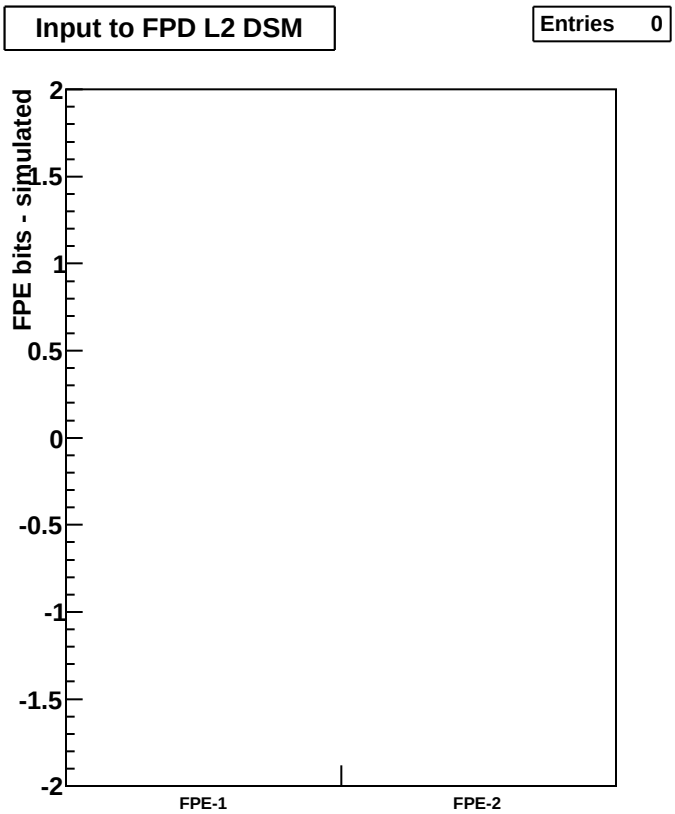

Input to FE003 QT board
Entries 64
ADC
channel


Input to FE004 QT board
Entries 64
ADC
channel


Input to FPE L1 DSM
Entries 8
ADC sum
200
180
160
140
120
100
80
60
40
20
0
FE001
FE002
FE003
FE004


Input to FPE L1 DSM
Entries 5
ADC sum - simulated
200
150
100
50
0
-50
-100
-150
-200
FE001
FE002
FE003
FE004


Input to FPD L2 DSM
Entries 4
FPE bits
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
FPE-1
FPE-2


Input to FPD L2 DSM
Entries 0
FPE bits - simulated
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
FPE-1
FPE-2