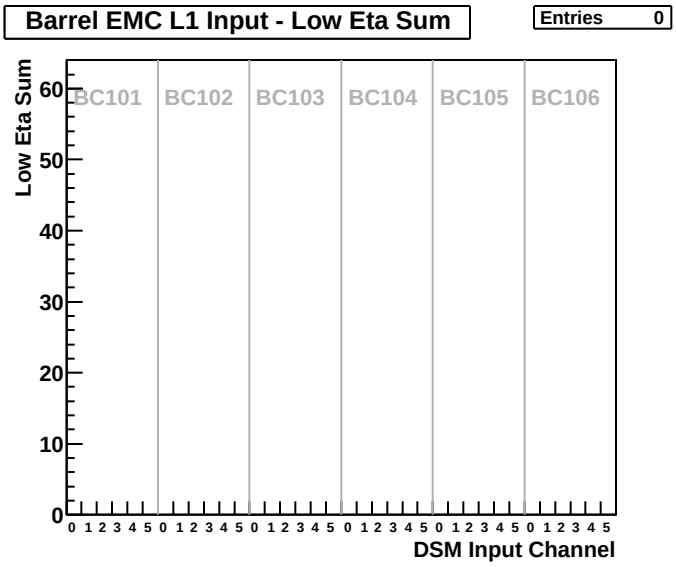
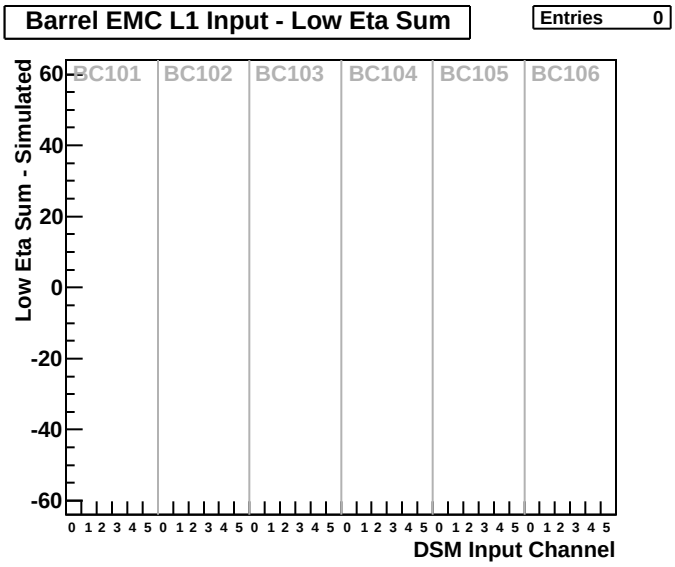
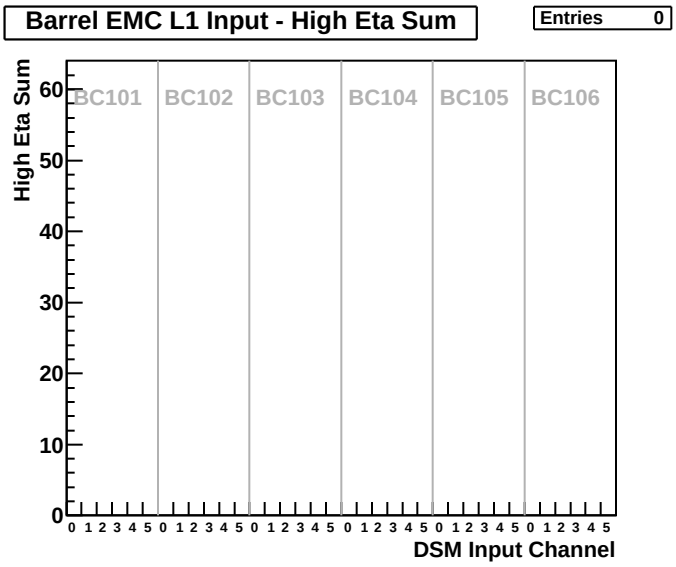
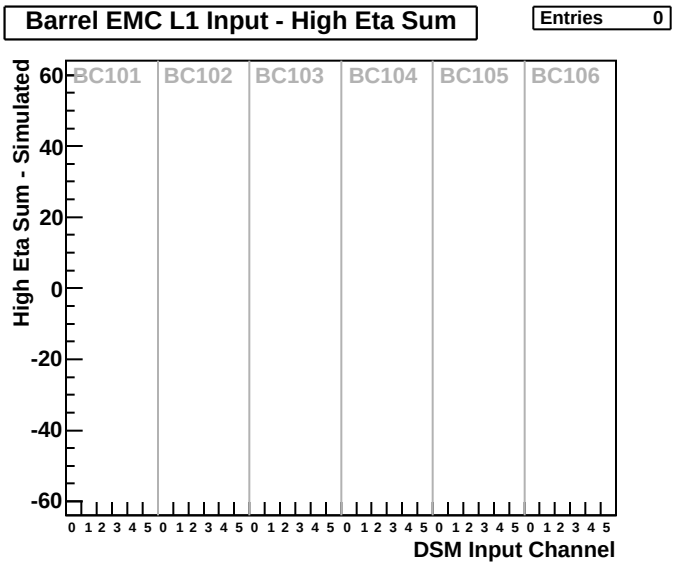
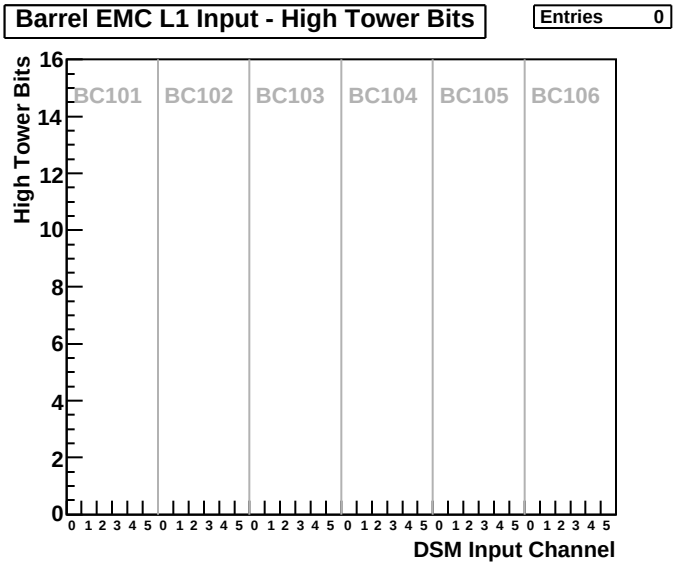
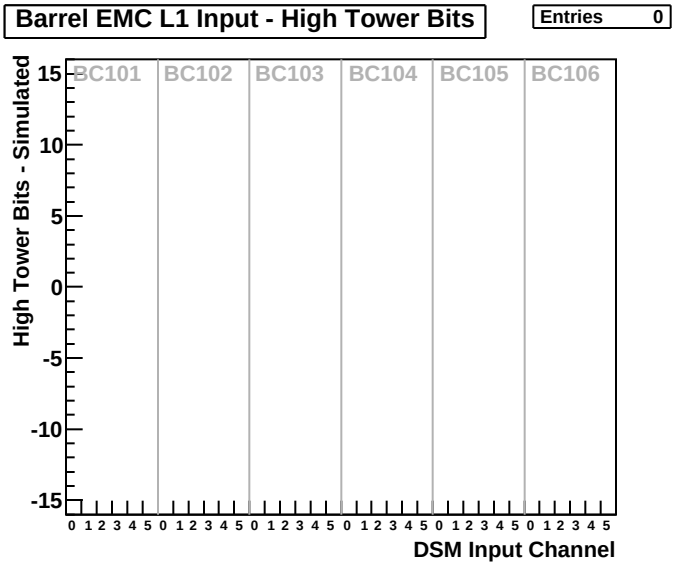

Barrel EMC L1 Input - Low Eta Sum
Entries 0
Low Eta Sum
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

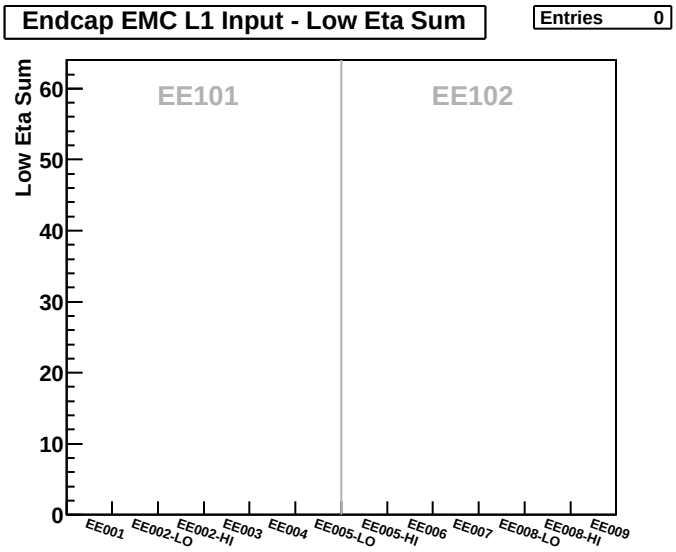

Barrel EMC L1 Input - Low Eta Sum
Entries 0
Low Eta Sum - Simulated
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

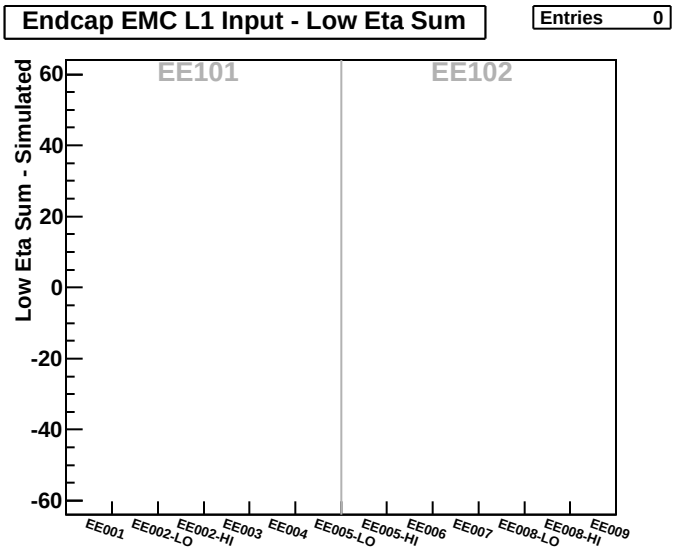

Barrel EMC L1 Input - High Eta Sum
Entries 0
High Eta Sum
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

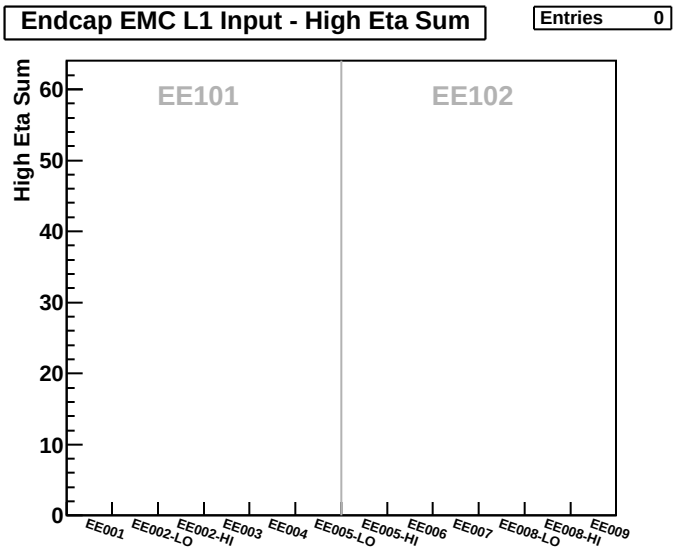

Barrel EMC L1 Input - High Eta Sum
Entries 0
High Eta Sum - Simulated
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

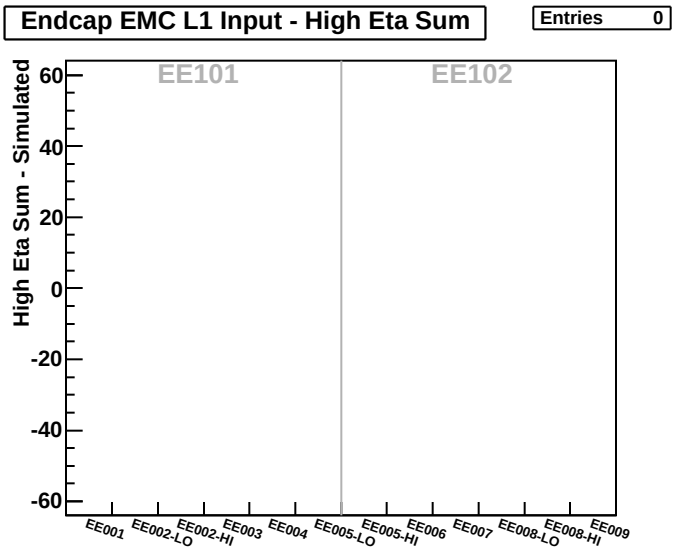

Barrel EMC L1 Input - High Tower Bits
Entries 0
High Tower Bits
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

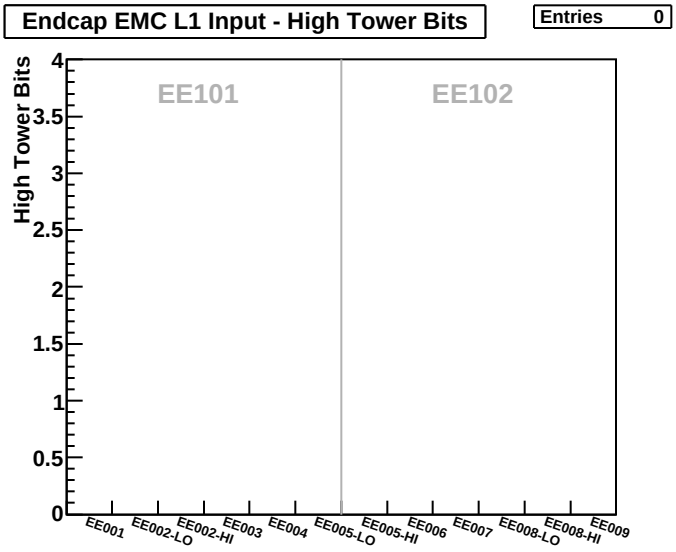

Barrel EMC L1 Input - High Tower Bits
Entries 0
High Tower Bits - Simulated
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

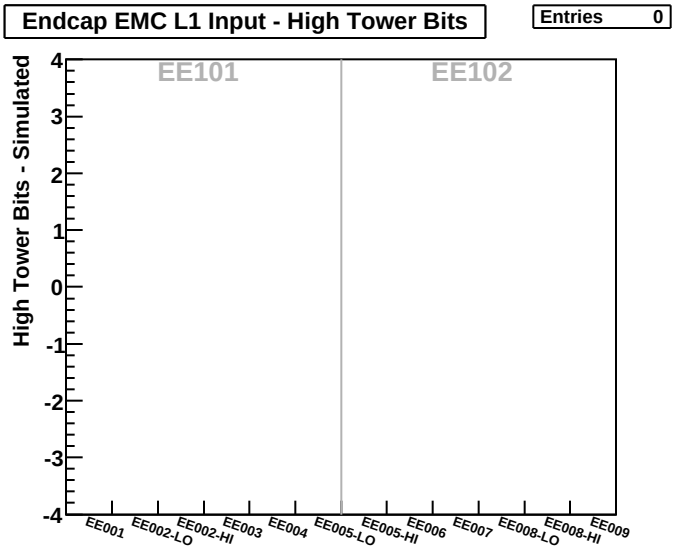

Endcap EMC L1 Input - Low Eta Sum
Entries 0
Low Eta Sum
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

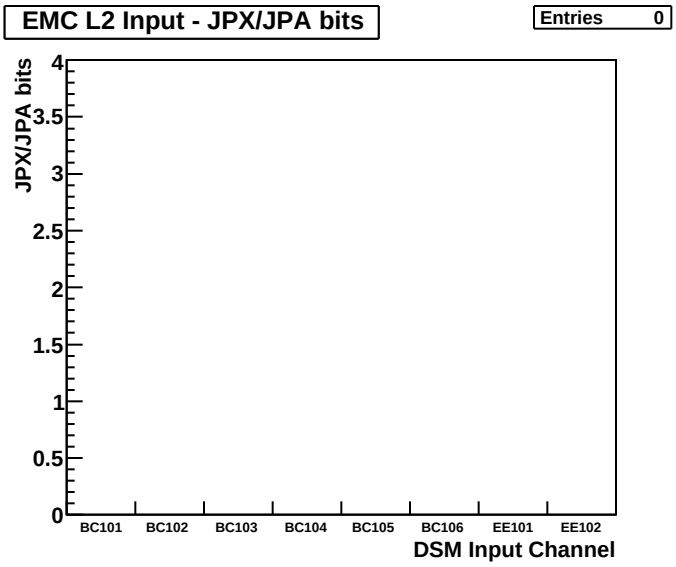

Endcap EMC L1 Input - Low Eta Sum
Entries 0
Low Eta Sum - Simulated
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

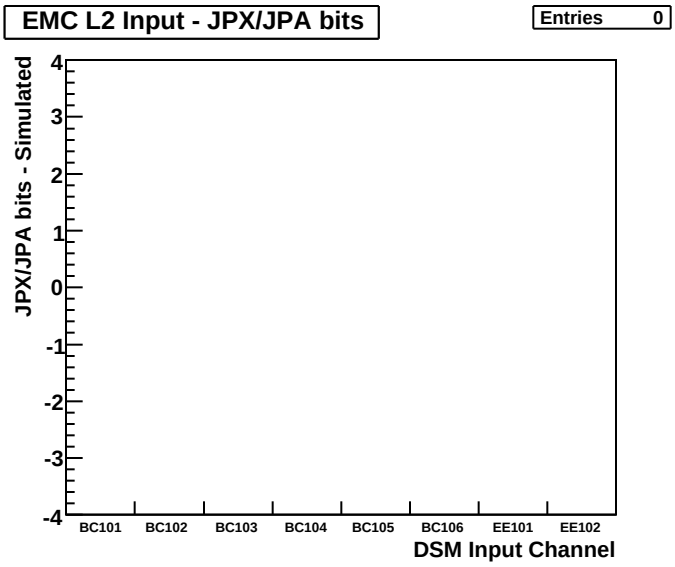

Endcap EMC L1 Input - High Eta Sum
Entries 0
High Eta Sum
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

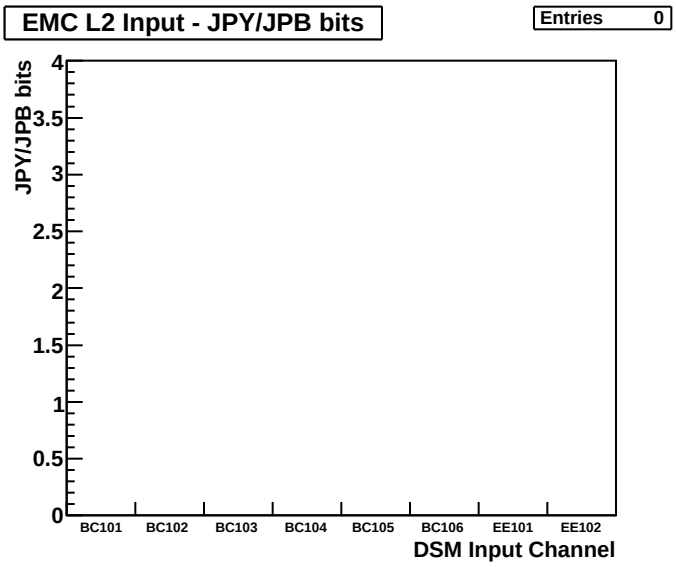

Endcap EMC L1 Input - High Eta Sum
Entries 0
High Eta Sum - Simulated
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

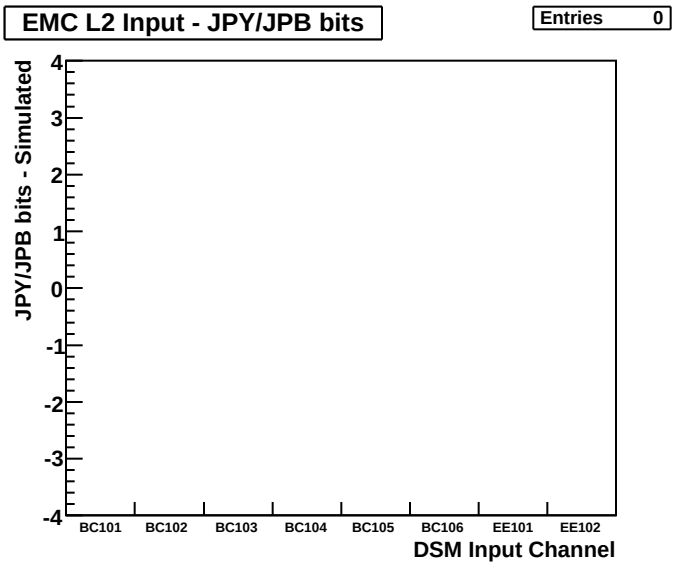

Endcap EMC L1 Input - High Tower Bits
Entries 0
High Tower Bits
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

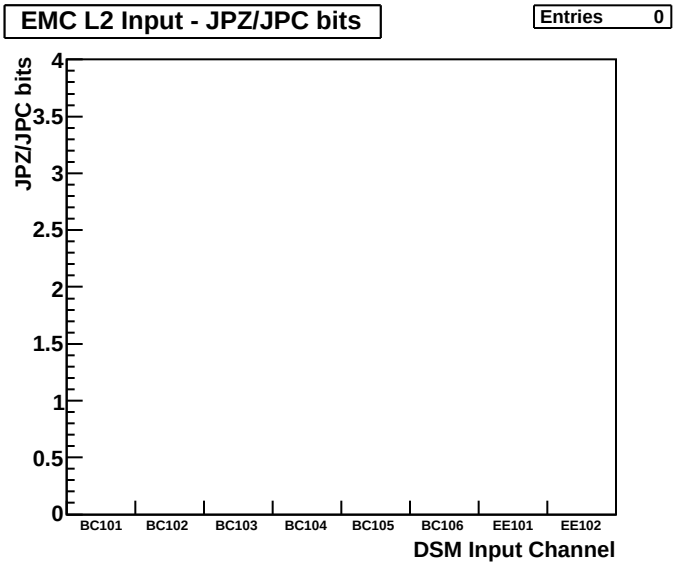

Endcap EMC L1 Input - High Tower Bits
Entries 0
High Tower Bits - Simulated
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

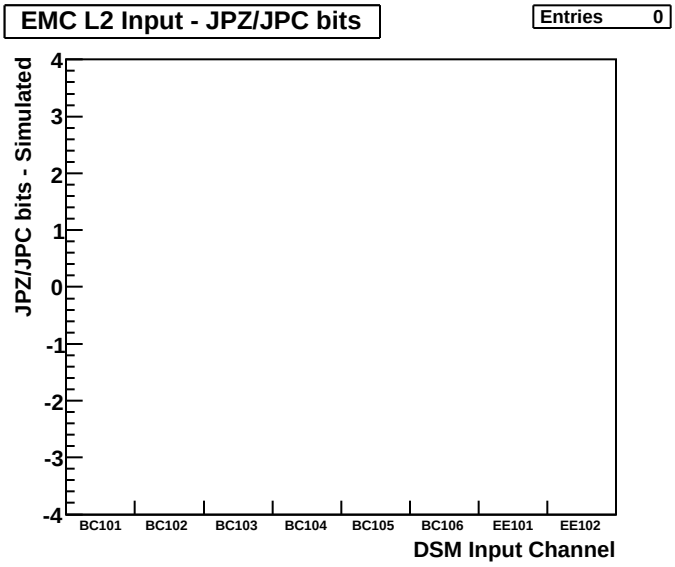

EMC L2 Input - JPX/JPA bits
Entries 0
JPX/JPA bits
4
3.5
3
2.5
2
1.5
1
0.5
0
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102
DSM Input Channel

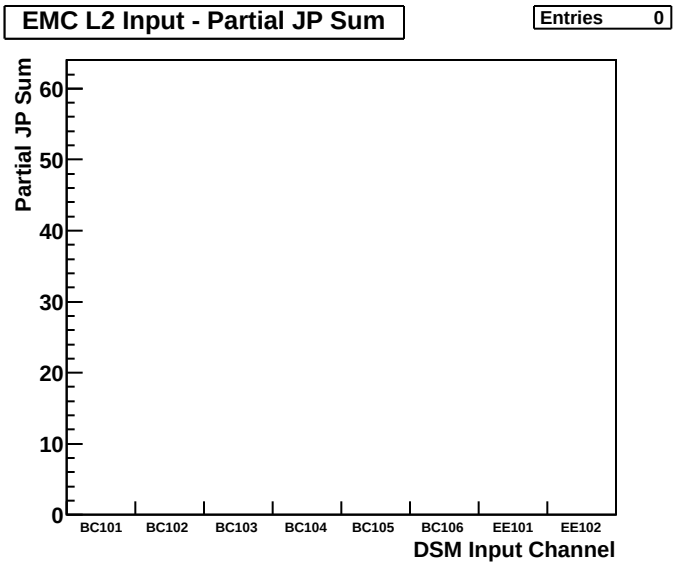

EMC L2 Input - JPX/JPA bits
Entries 0
JPX/JPA bits - Simulated
4
3
2
1
0
-1
-2
-3
-4
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102
DSM Input Channel

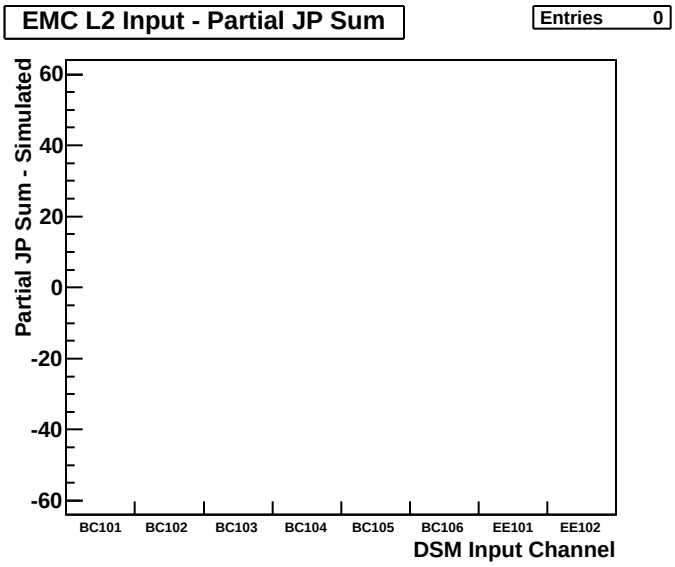

EMC L2 Input - JPY/JPB bits
Entries 0
JPY/JPB bits
4
3.5
3
2.5
2
1.5
1
0.5
0
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102
DSM Input Channel

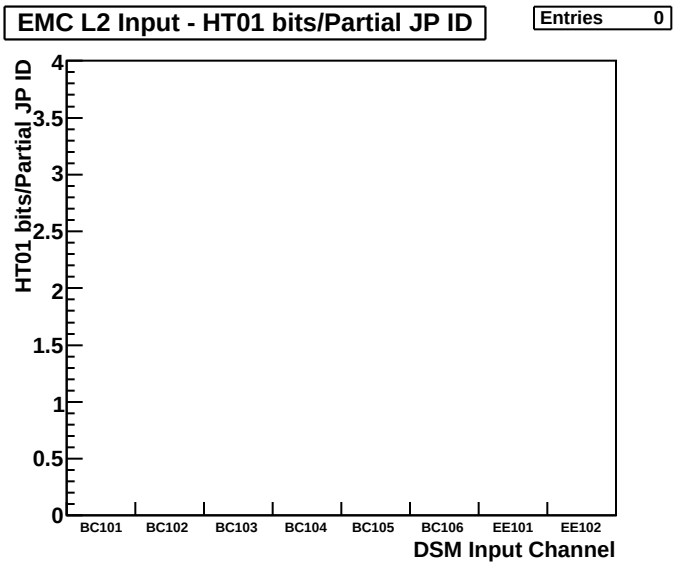

EMC L2 Input - JPY/JPB bits
Entries 0
JPY/JPB bits - Simulated
4
3
2
1
0
-1
-2
-3
-4
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102
DSM Input Channel

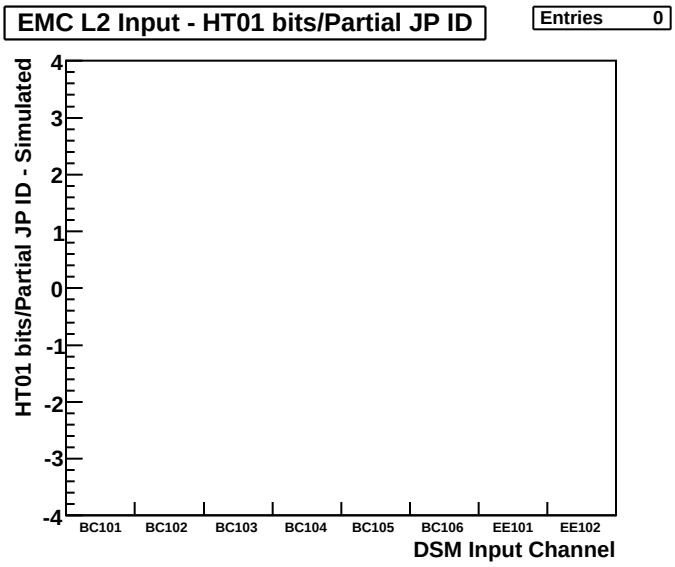

EMC L2 Input - JPZ/JPC bits
Entries 0
JPZ/JPC bits
4
3.5
3
2.5
2
1.5
1
0.5
0
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102
DSM Input Channel

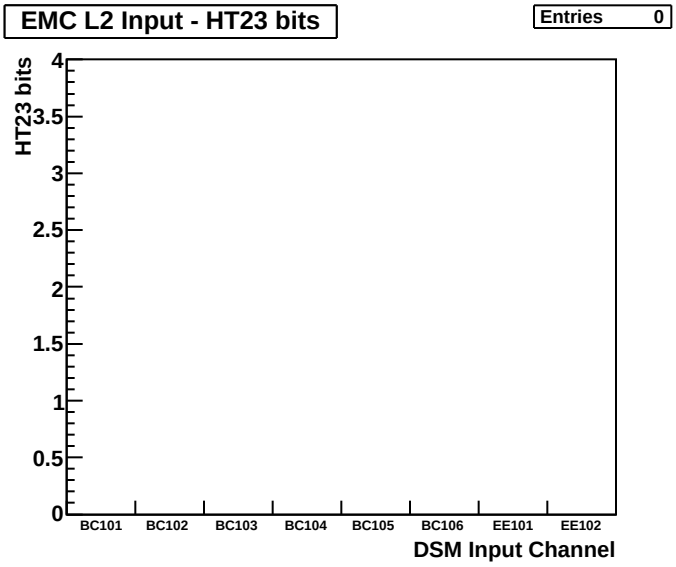

EMC L2 Input - JPZ/JPC bits
Entries 0
JPZ/JPC bits - Simulated
4
3
2
1
0
-1
-2
-3
-4
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102
DSM Input Channel

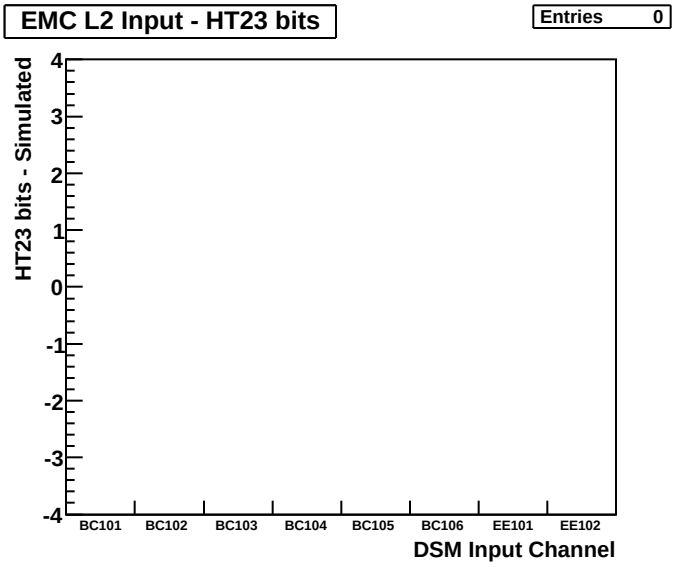

EMC L2 Input - Partial JP Sum
Entries 0
Partial JP Sum
60
50
40
30
20
10
0
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102
DSM Input Channel

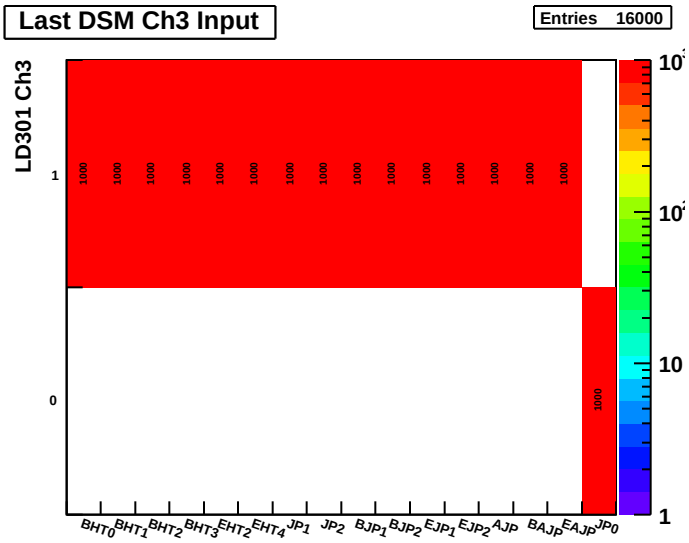

EMC L2 Input - Partial JP Sum
Entries 0
Partial JP Sum - Simulated
60
40
20
0
-20
-40
-60
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102
DSM Input Channel

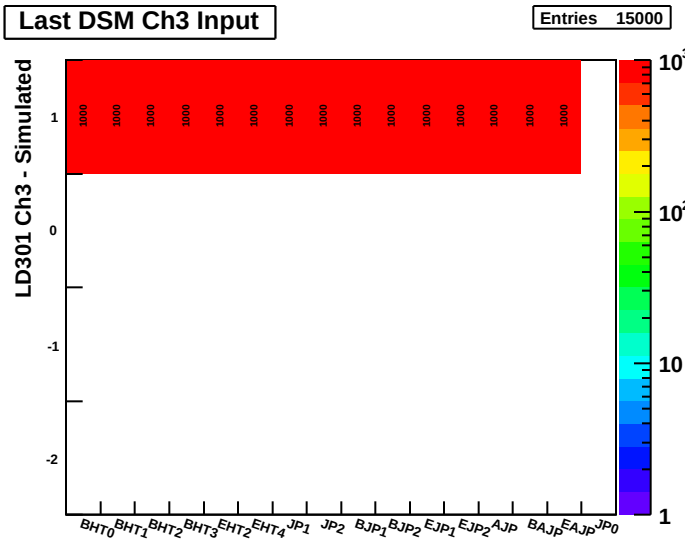

EMC L2 Input - HT01 bits/Partial JP ID
Entries 0
HT01 bits/Partial JP ID
4
3.5
3
2.5
2
1.5
1
0.5
0
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102
DSM Input Channel

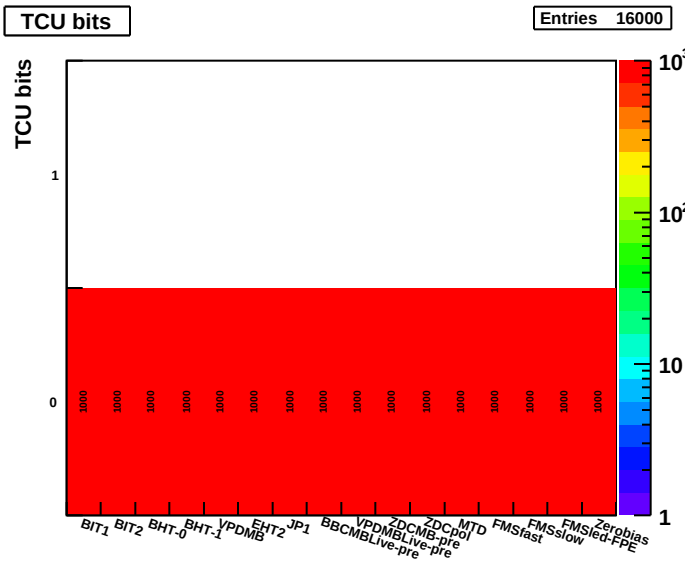

EMC L2 Input - HT01 bits/Partial JP ID
Entries 0
HT01 bits/Partial JP ID - Simulated
4
3
2
1
0
-1
-2
-3
-4
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102
DSM Input Channel

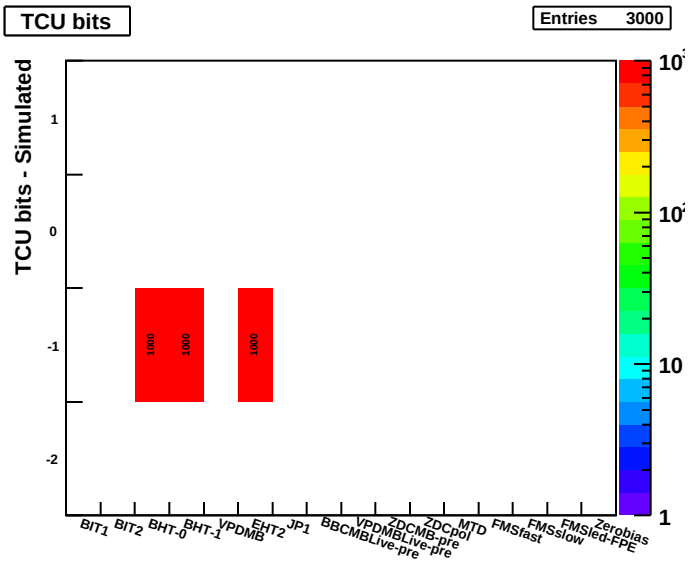

EMC L2 Input - HT23 bits
Entries 0
HT23 bits
4
3.5
3
2.5
2
1.5
1
0.5
0
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102
DSM Input Channel

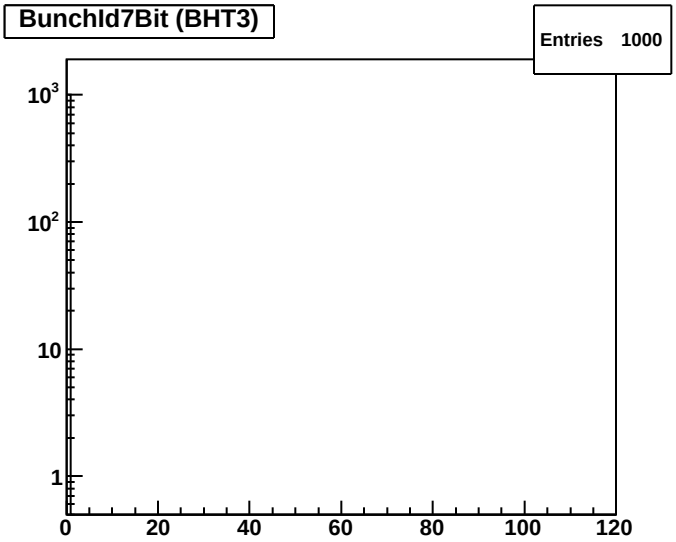

EMC L2 Input - HT23 bits
Entries 0
HT23 bits - Simulated
4
3
2
1
0
-1
-2
-3
-4
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102
DSM Input Channel

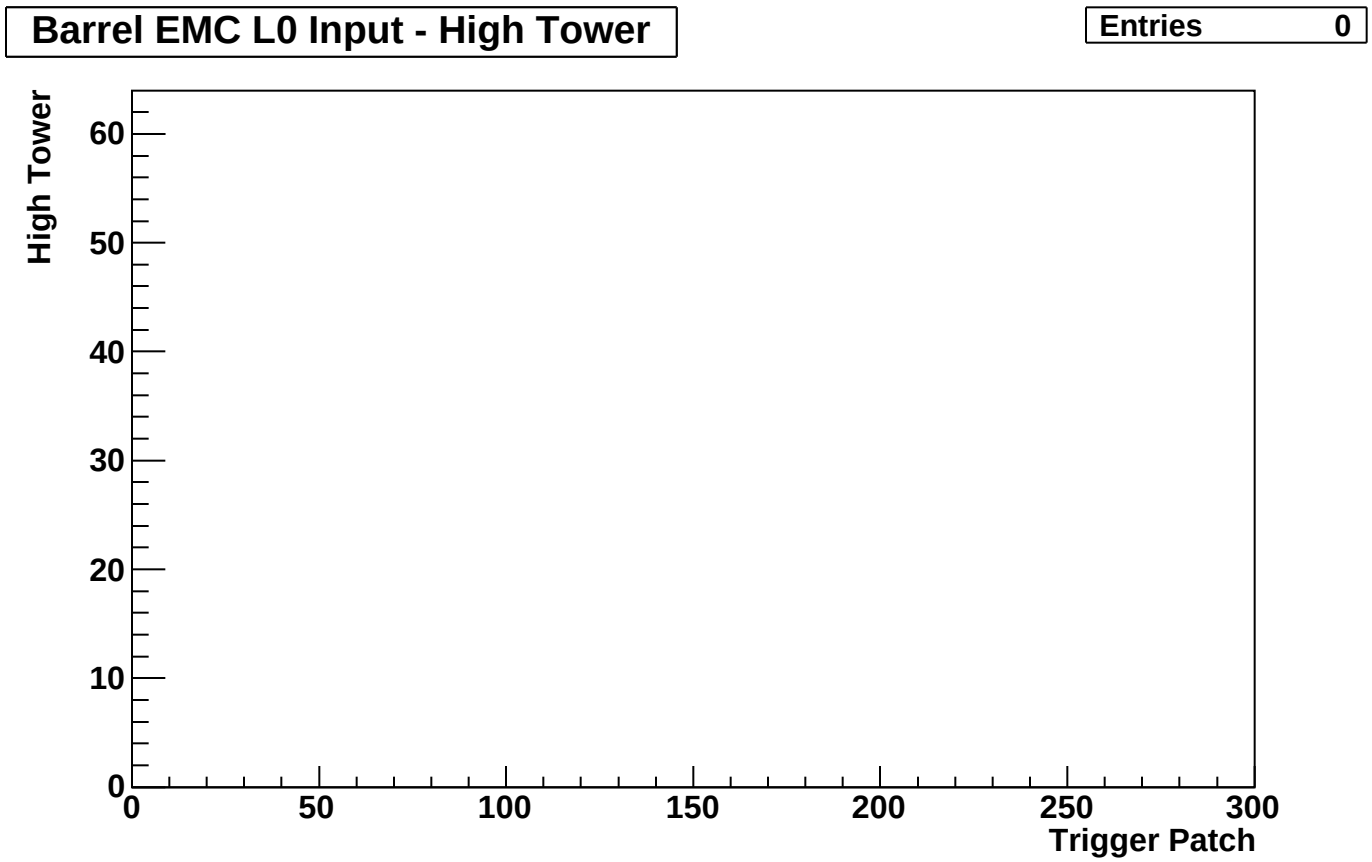

Last DSM Ch3 Input
Entries 16000
LD301 Ch3
BHT0 BHT1 BHT2 BHT3 EHT2 EHT4 JP1 JP2 BJP1 BJP2 EJP1 EJP2 AJP BAJP EAJP JP0

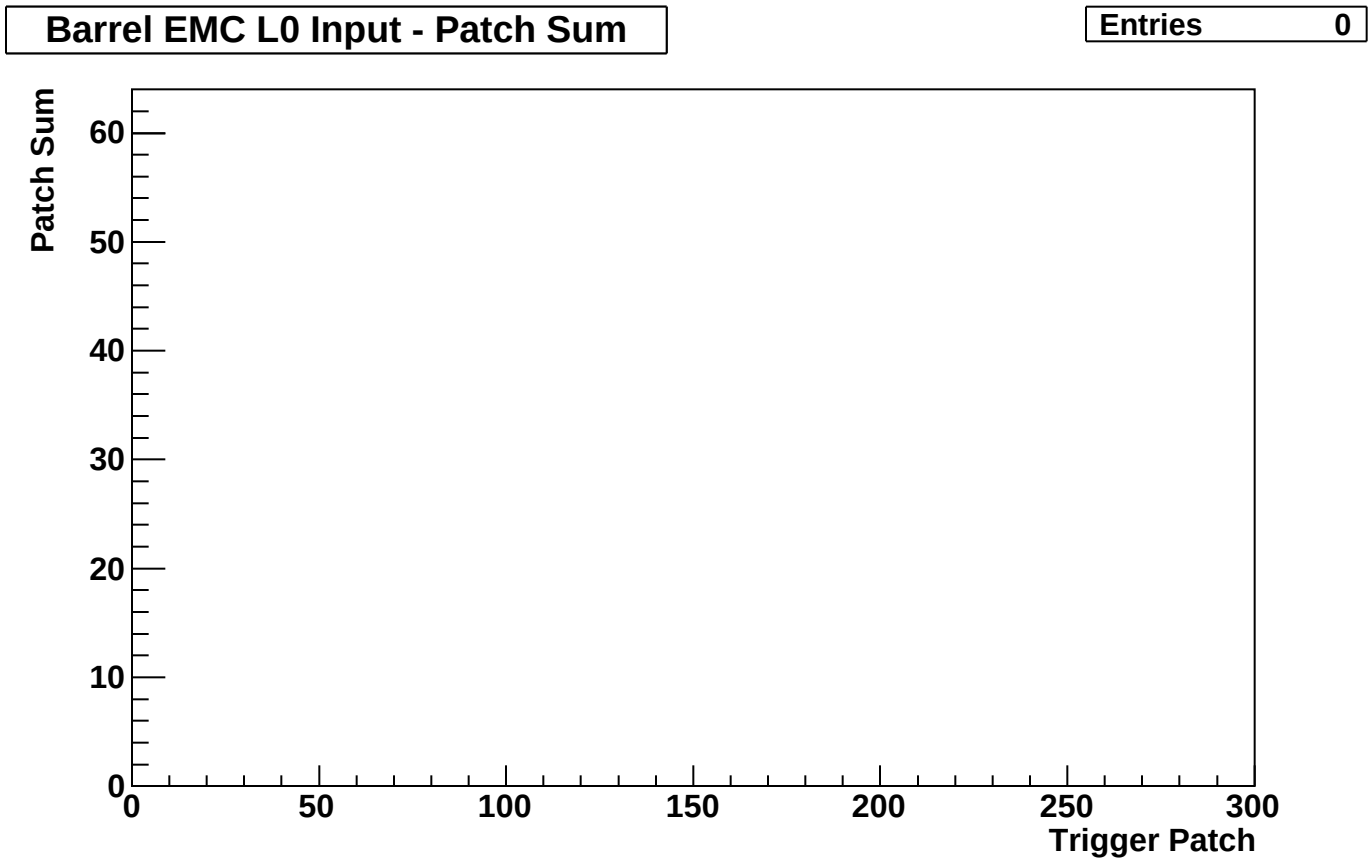

Last DSM Ch3 Input
Entries 15000
LD301 Ch3 - Simulated
BHT0 BHT1 BHT2 BHT3 EHT2 EHT4 JP1 JP2 BJP1 BJP2 EJP1 EJP2 AJP BAJP EAJP JP0

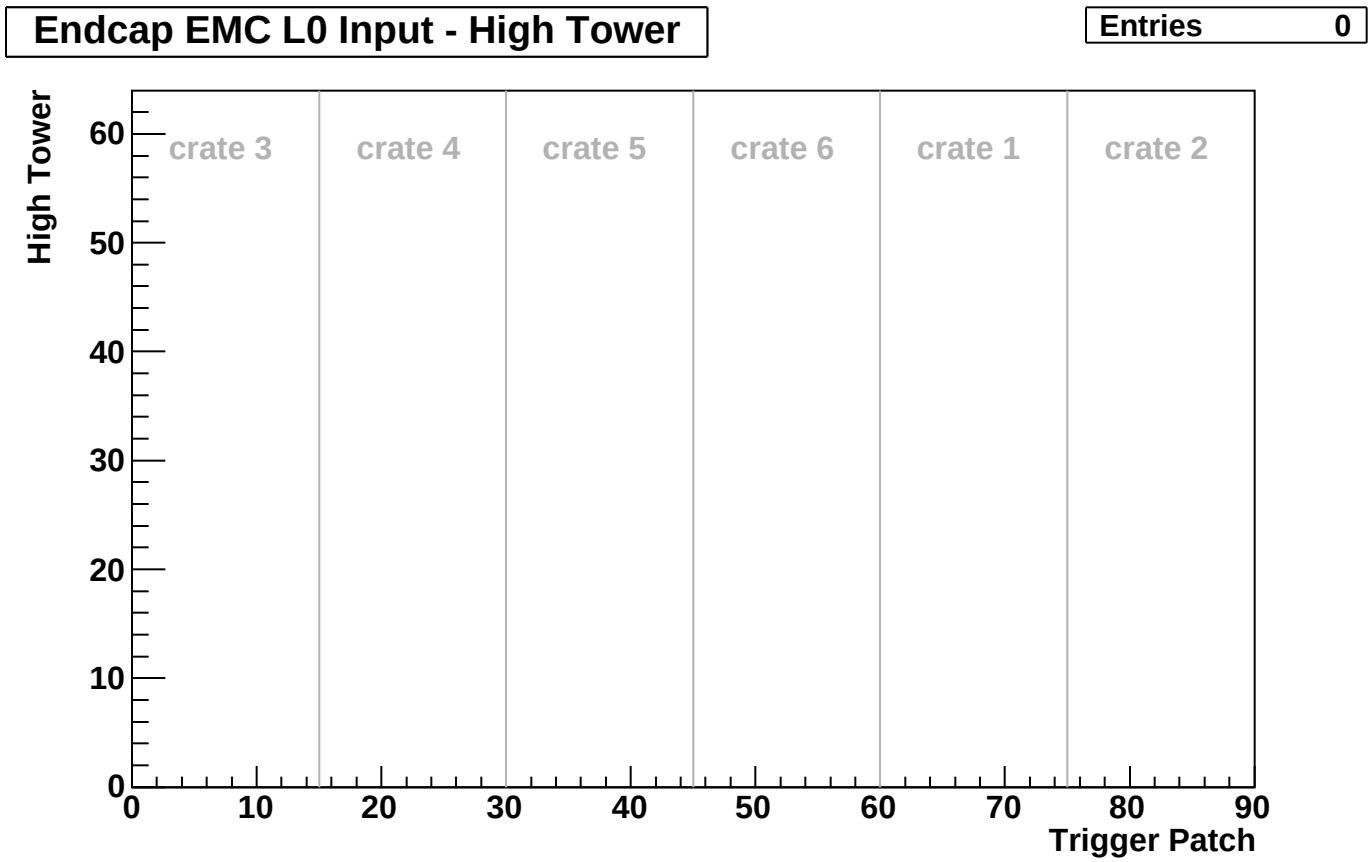

TCU bits
Entries 16000
TCU bits
BIT1 BIT2 BHT-0 BHT-1 VPDMB EHT2 JP1 BBCMBLive-pre VPDMBLive-pre ZDCMB-pre ZDCpol MTD FMSfast FMSslow FMSled-FPE Zerobias

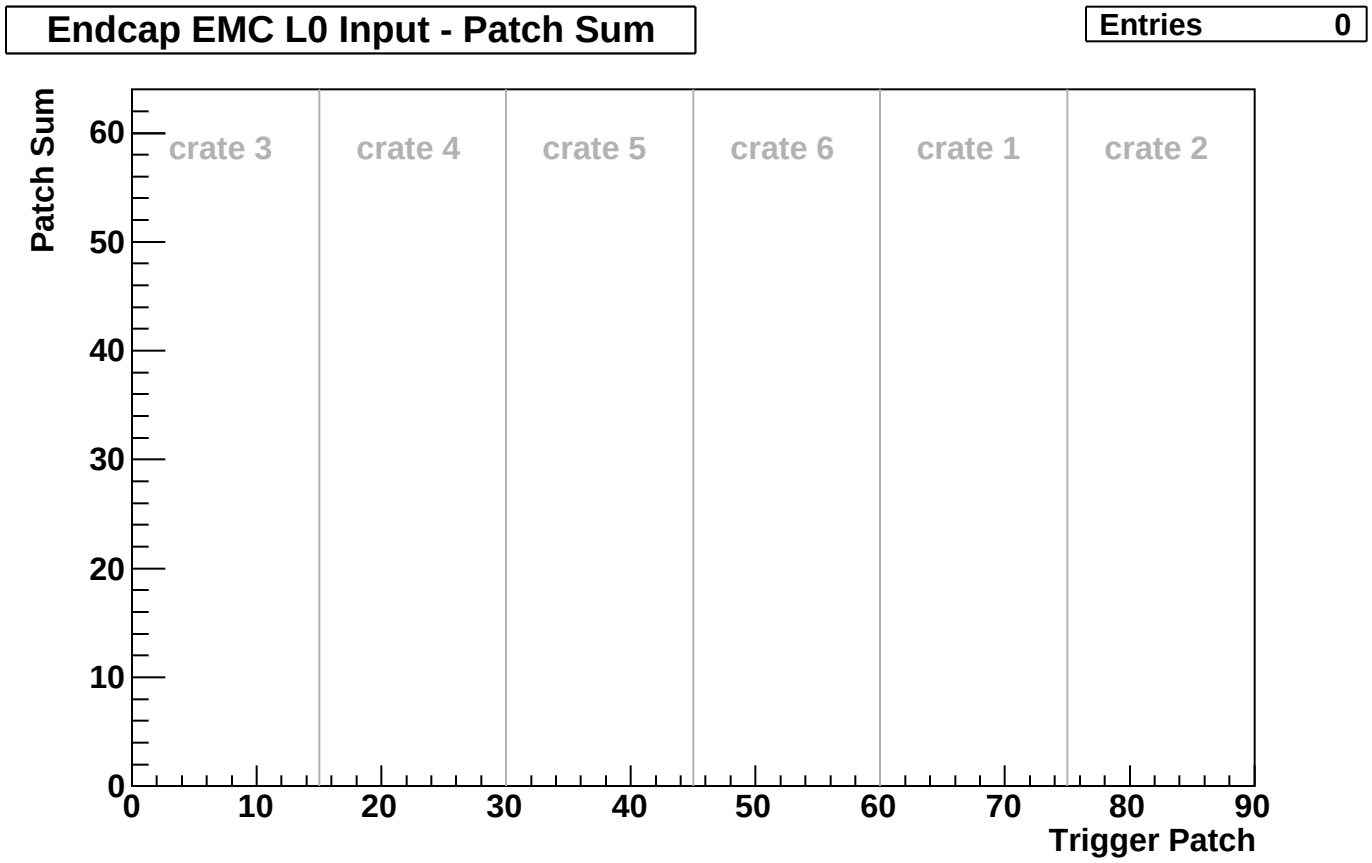

TCU bits
Entries 3000
TCU bits - Simulated
BIT1 BIT2 BHT-0 BHT-1 VPDMB EHT2 JP1 BBCMBLive-pre VPDMBLive-pre ZDCMB-pre ZDCpol MTD FMSfast FMSslow FMSled-FPE Zerobias

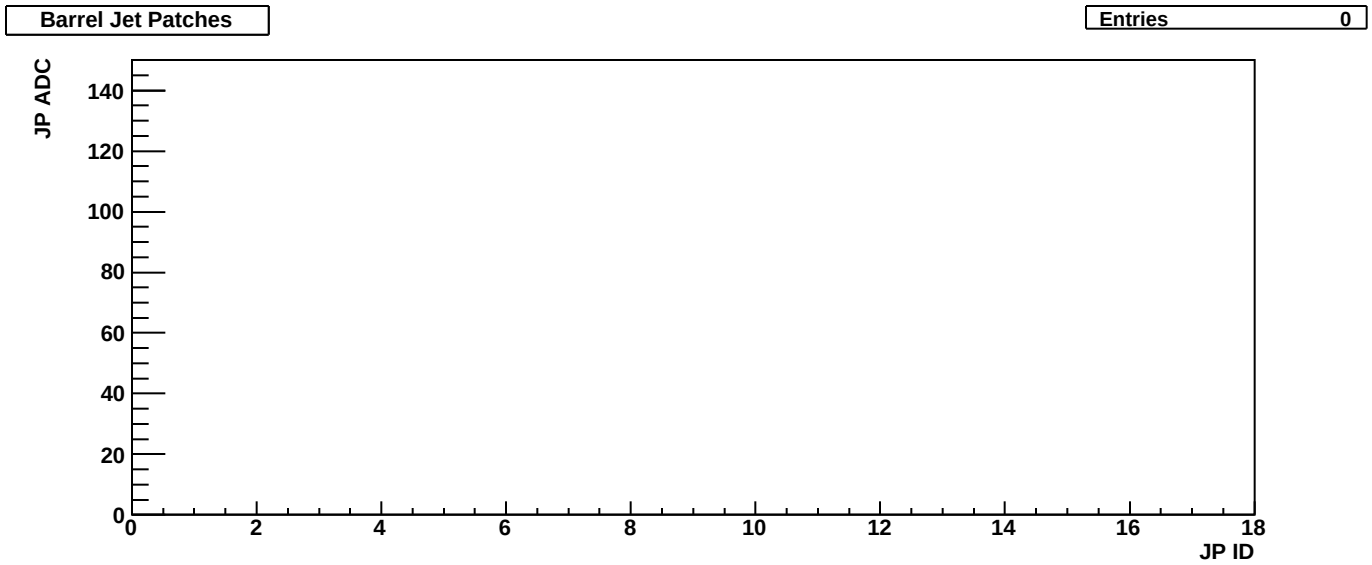

BunchId7Bit (BHT3)
Entries 1000

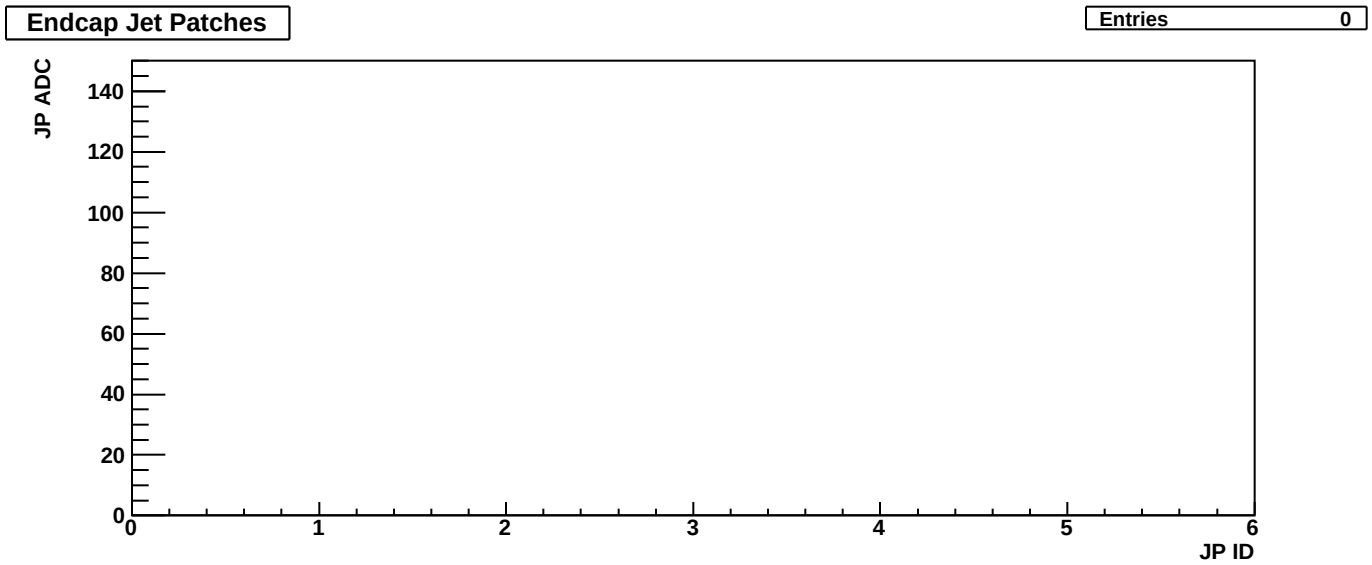

Barrel EMC L0 Input - High Tower
Entries 0
High Tower
0
10
20
30
40
50
60
0
50
100
150
200
250
300
Trigger Patch

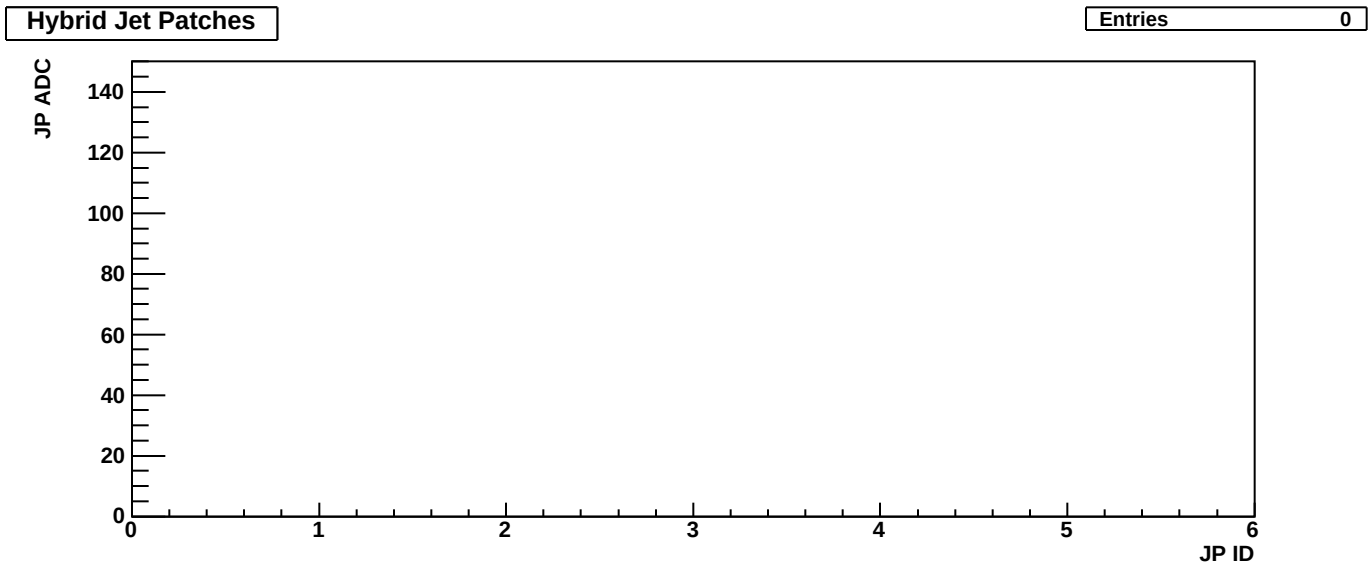

Barrel EMC L0 Input - Patch Sum
Entries 0
Patch Sum
0
10
20
30
40
50
60
0
50
100
150
200
250
300
Trigger Patch

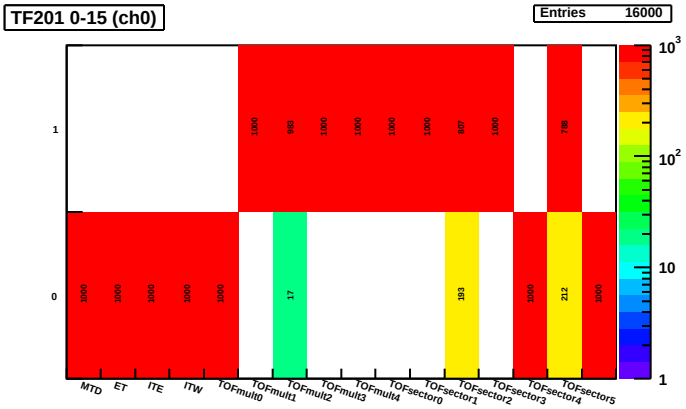

Endcap EMC L0 Input - High Tower
Entries 0
High Tower
crate 3
crate 4
crate 5
crate 6
crate 1
crate 2
0
10
20
30
40
50
60
70
80
90
Trigger Patch

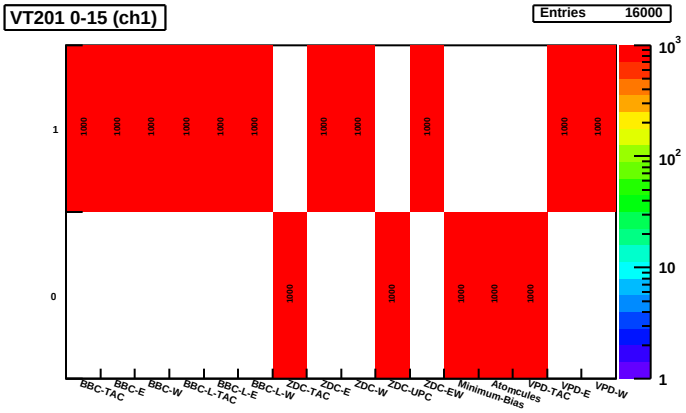

Endcap EMC L0 Input - Patch Sum
Entries 0
Patch Sum
crate 3
crate 4
crate 5
crate 6
crate 1
crate 2
0
10
20
30
40
50
60
70
80
90
Trigger Patch

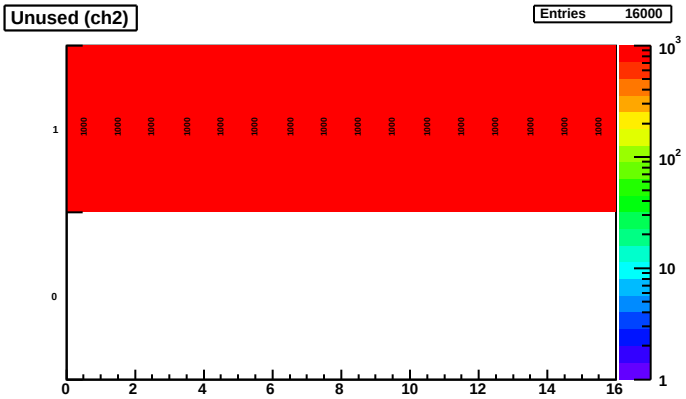

Barrel Jet Patches
Entries 0
JP ADC
0
20
40
60
80
100
120
140
0
2
4
6
8
10
12
14
16
18
JP ID

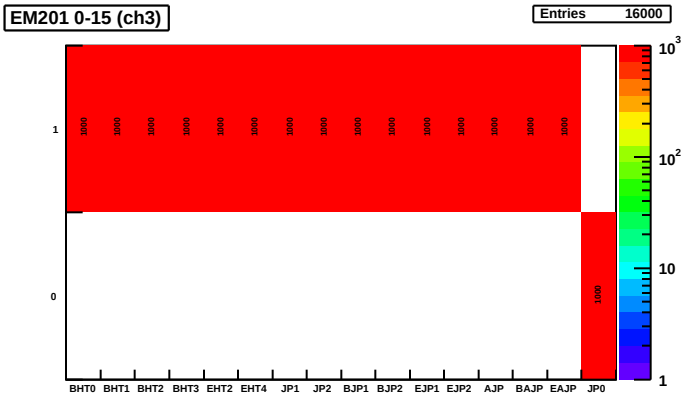

Endcap Jet Patches
Entries 0
JP ADC
0
20
40
60
80
100
120
140
0
1
2
3
4
5
6
JP ID

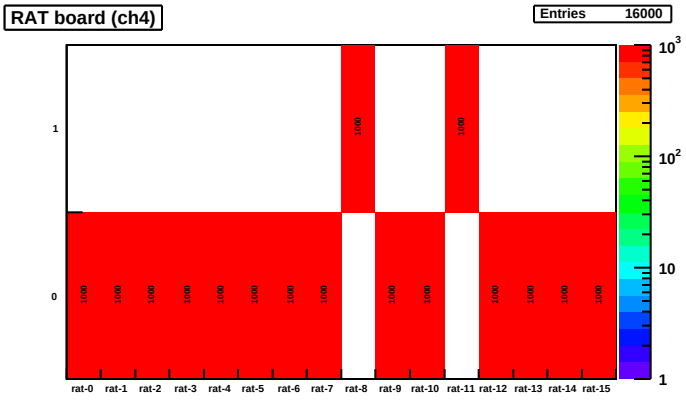

Hybrid Jet Patches
Entries 0
JP ADC
0
20
40
60
80
100
120
140
0
1
2
3
4
5
6
JP ID

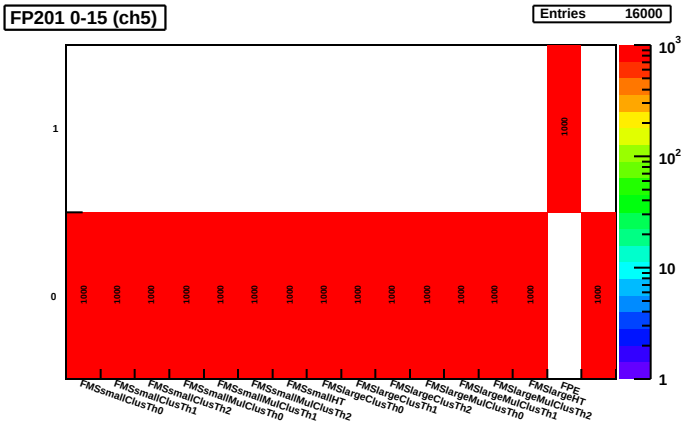

TF201 0-15 (ch0)
Entries 16000
MTD
ET
ITE
ITW
TOFmult0
TOFmult1
TOFmult2
TOFmult3
TOFmult4
TOFsector0
TOFsector1
TOFsector2
TOFsector3
TOFsector4
TOFsector5

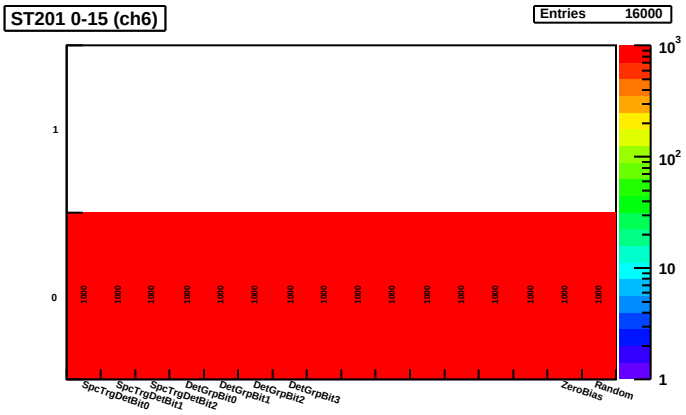

VT201 0-15 (ch1)
Entries 16000
BBC-TAC
BBC-E
BBC-W
BBC-L-TAC
BBC-L-E
BBC-L-W
ZDC-TAC
ZDC-E
ZDC-W
ZDC-UPC
ZDC-EW
Minimum-Bias
Atomcules
VPD-TAC
VPD-E
VPD-W

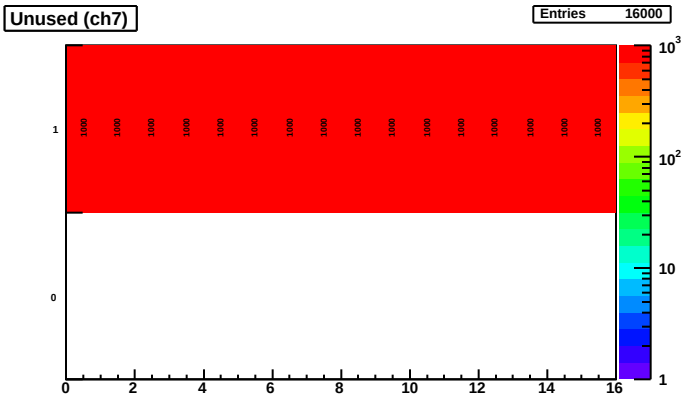

Unused (ch2)
Entries 16000

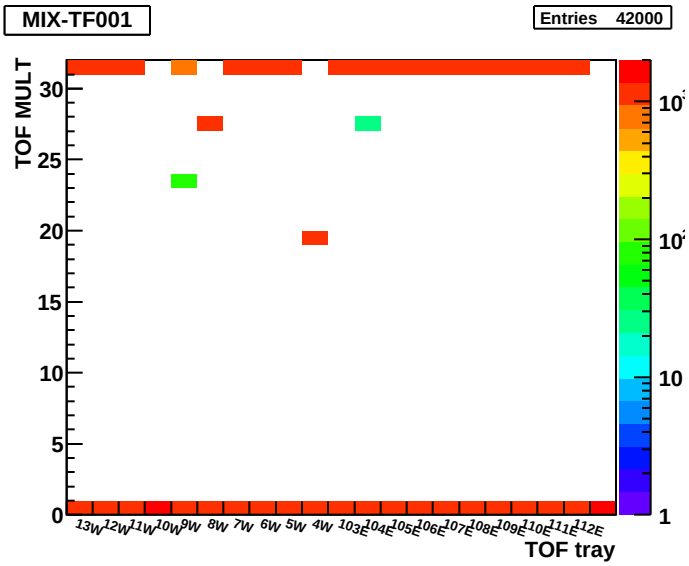

EM201 0-15 (ch3)
Entries 16000
BHT0
BHT1
BHT2
BHT3
EHT2
EHT4
JP1
JP2
BJP1
BJP2
EJP1
EJP2
AJP
BAJP
EAJP
JP0

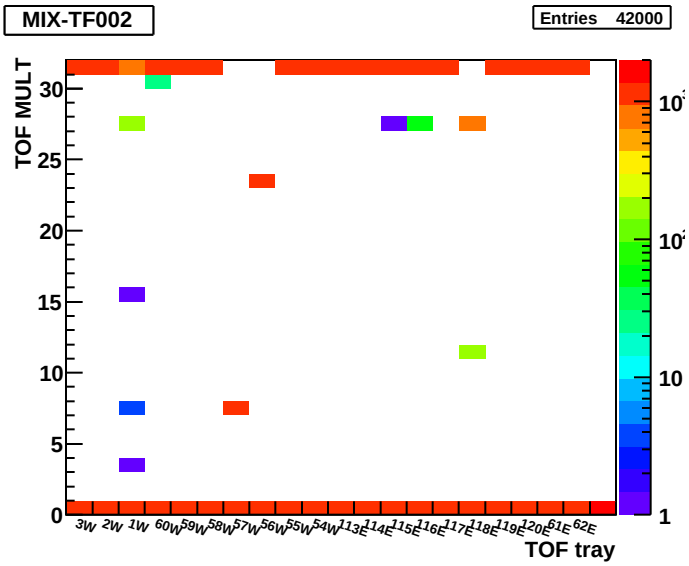

RAT board (ch4)
Entries 16000
rat-0
rat-1
rat-2
rat-3
rat-4
rat-5
rat-6
rat-7
rat-8
rat-9
rat-10
rat-11
rat-12
rat-13
rat-14
rat-15

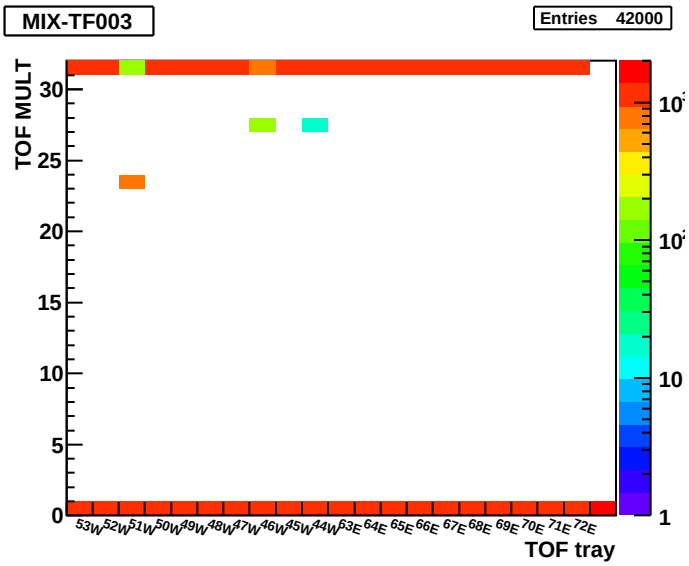

FP201 0-15 (ch5)
Entries 16000
FMSsmallClusTh0
FMSsmallClusTh1
FMSsmallClusTh2
FMSsmallMulClusTh0
FMSsmallMulClusTh1
FMSsmallHT
FMSlargeClusTh2
FMSlargeClusTh0
FMSlargeClusTh1
FMSlargeMulClusTh0
FMSlargeMulClusTh1
FMSlargeMulClusTh2
FMSlargeHT
FPE

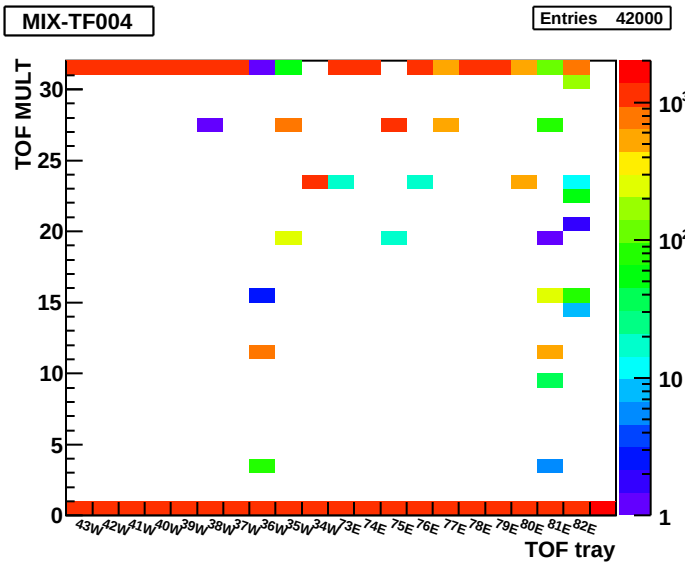

ST201 0-15 (ch6)
Entries 16000
SpcTrgDetBit0
SpcTrgDetBit1
SpcTrgDetBit2
DetCrpBit0
DetCrpBit1
DetCrpBit2
DetCrpBit3
ZeroBias
Random

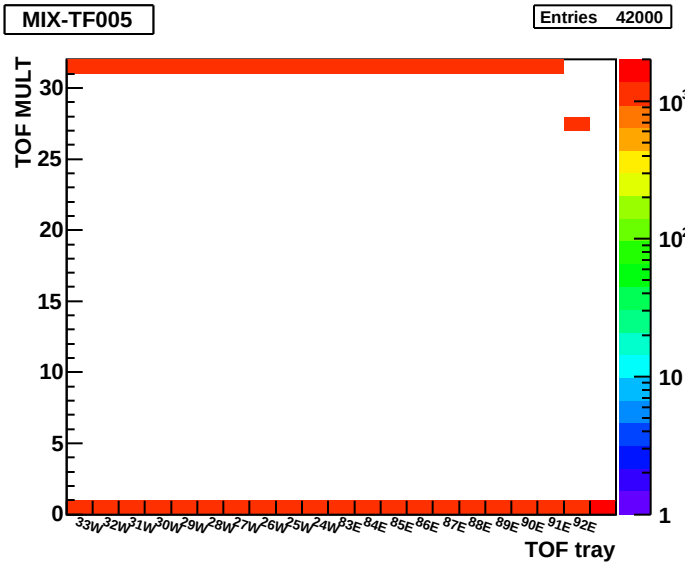

Unused (ch7)
Entries 16000

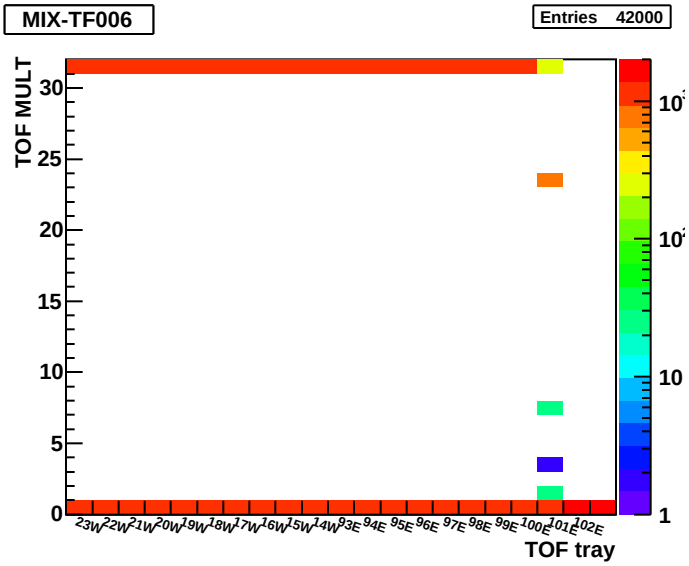

MIX-TF001
Entries 42000
TOF MULT
TOF tray

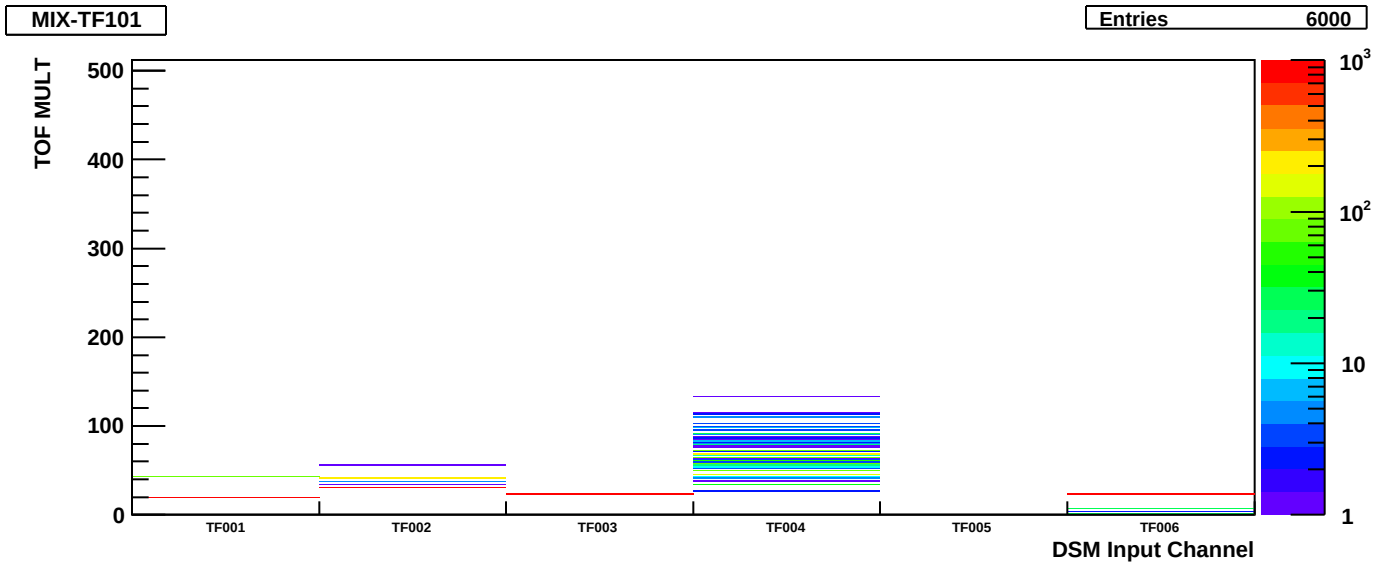

MIX-TF002
Entries 42000
TOF MULT
TOF tray

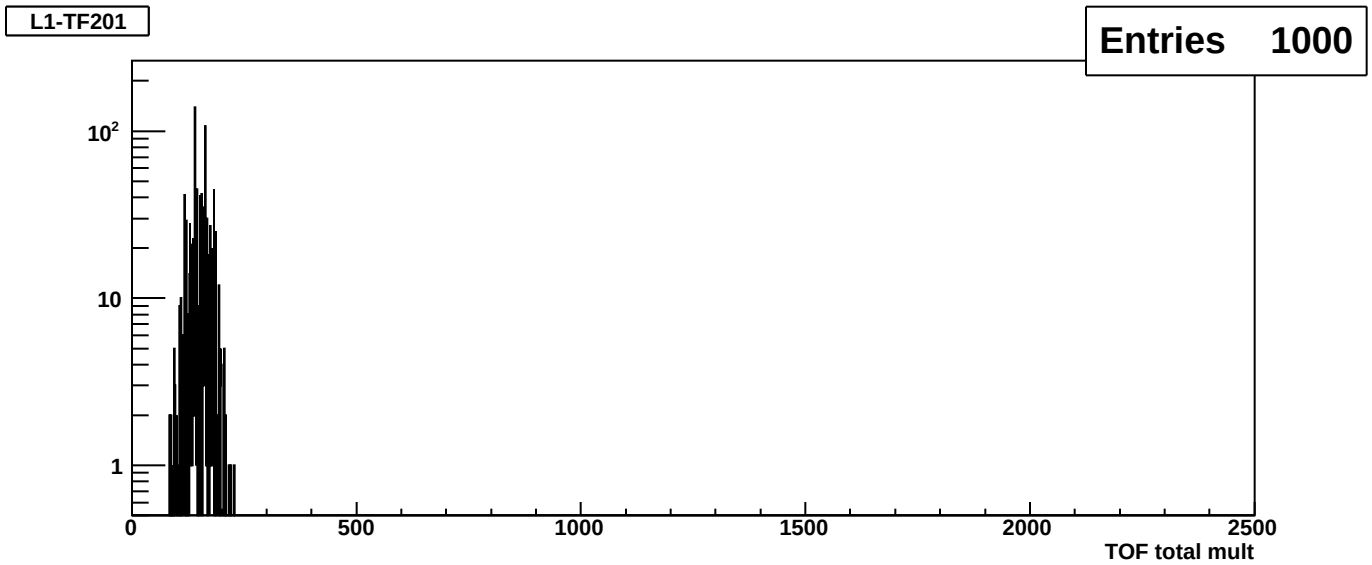

MIX-TF003
Entries 42000
TOF MULT
TOF tray

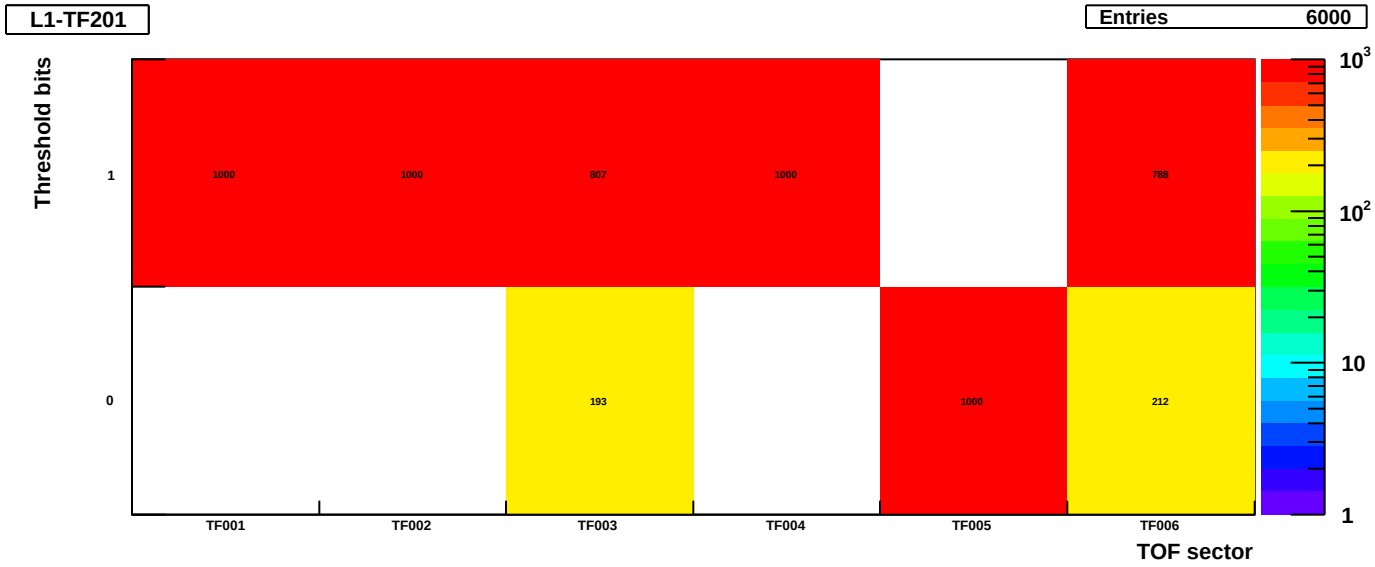

MIX-TF004
Entries 42000
TOF MULT
TOF tray

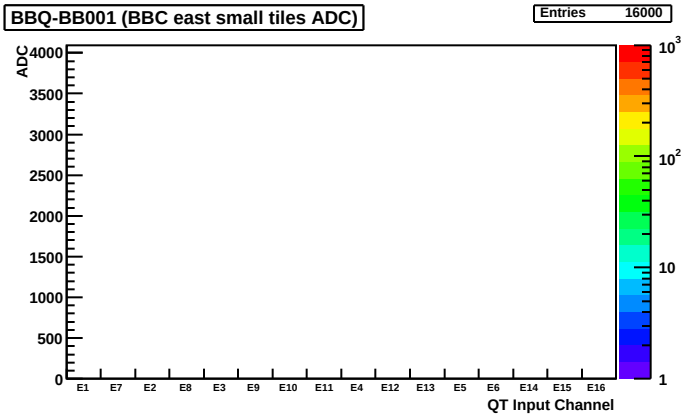

MIX-TF005
Entries 42000
TOF MULT
TOF tray

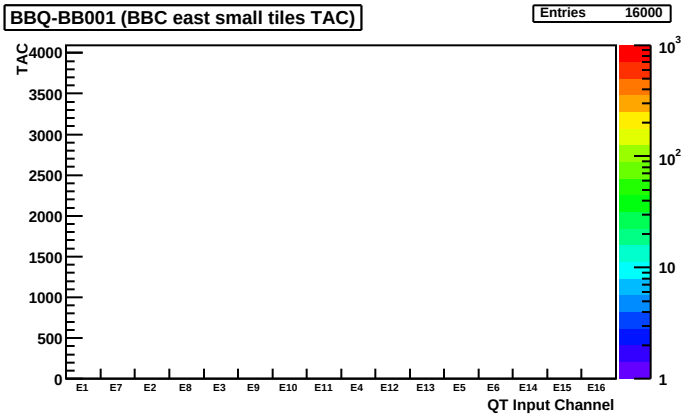

MIX-TF006
Entries 42000
TOF MULT
TOF tray

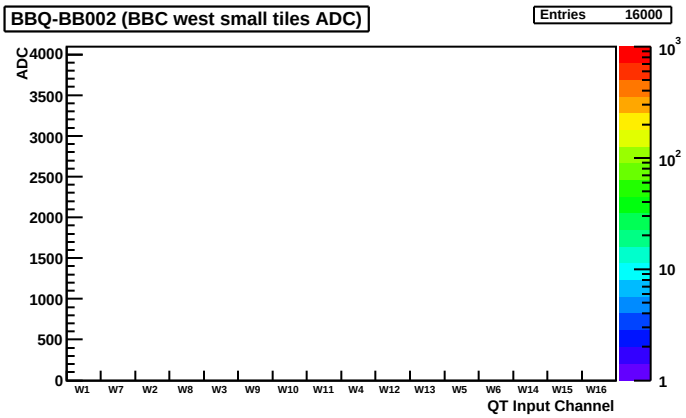

MIX-TF101
Entries 6000
TOF MULT
500
400
300
200
100
0
TF001
TF002
TF003
TF004
TF005
TF006
DSM Input Channel
10^3
10^2
10
1

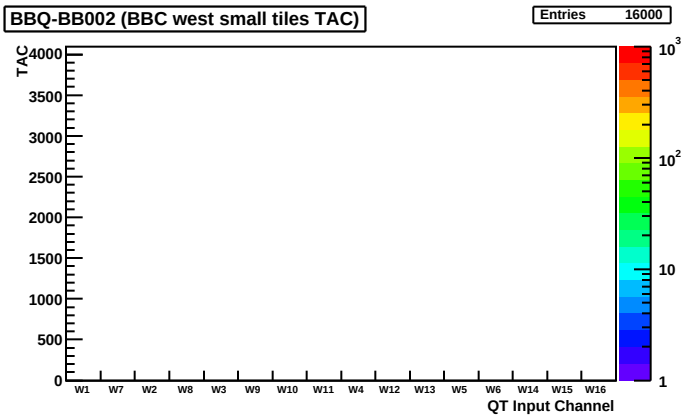

L1-TF201
Entries 1000
10^2
10
1
0
500
1000
1500
2000
2500
TOF total mult

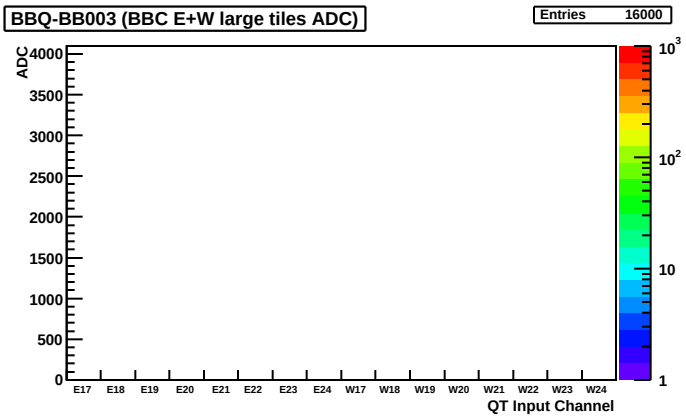

L1-TF201
Entries 6000
Threshold bits
1
0
1000
1000
807
1000
788
193
1000
212
TF001
TF002
TF003
TF004
TF005
TF006
TOF sector
10^3
10^2
10
1

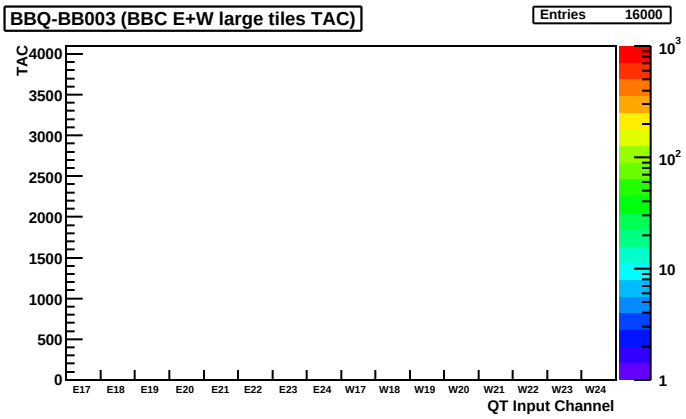

BBQ-BB001 (BBC east small tiles ADC)
Entries 16000
ADC
QT Input Channel

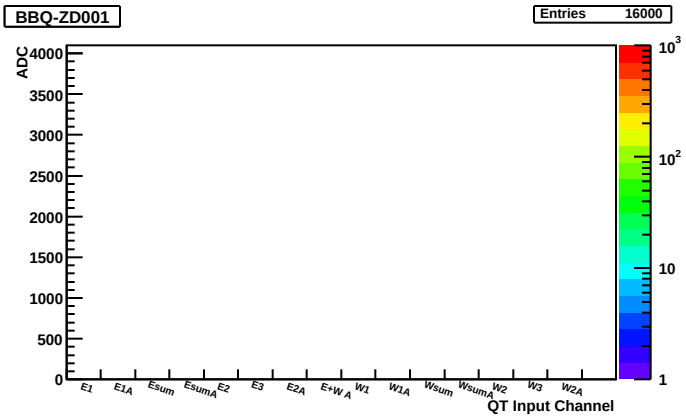

BBQ-BB001 (BBC east small tiles TAC)
Entries 16000
TAC
QT Input Channel

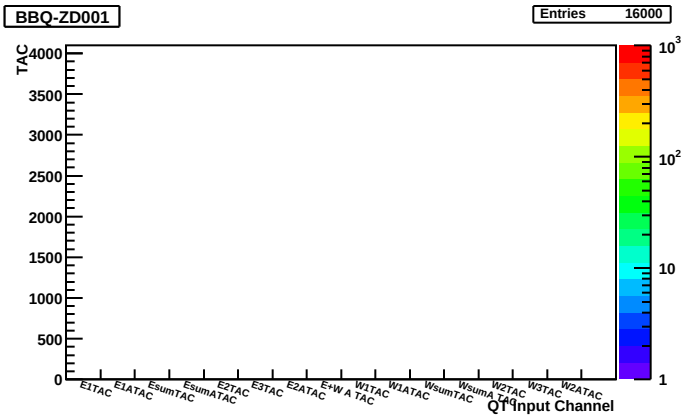

BBQ-BB002 (BBC west small tiles ADC)
Entries 16000
ADC
QT Input Channel

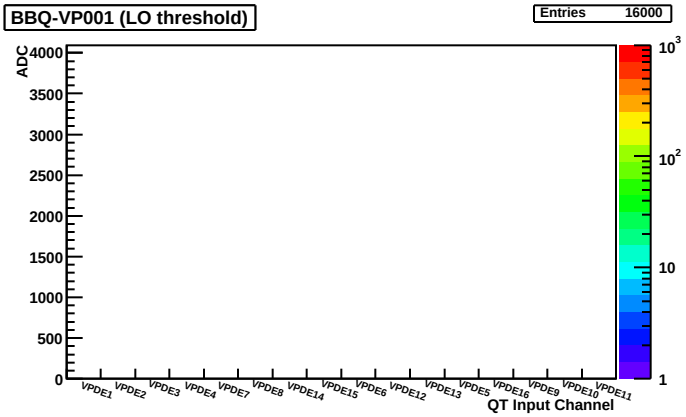

BBQ-BB002 (BBC west small tiles TAC)
Entries 16000
TAC
QT Input Channel

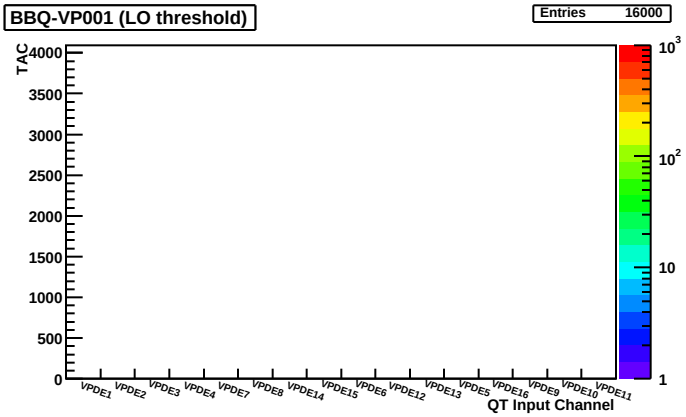

BBQ-BB003 (BBC E+W large tiles ADC)
Entries 16000
ADC
QT Input Channel

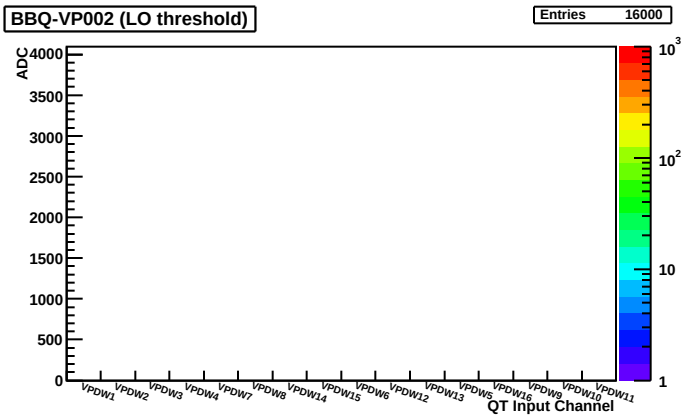

BBQ-BB003 (BBC E+W large tiles TAC)
Entries 16000
TAC
QT Input Channel

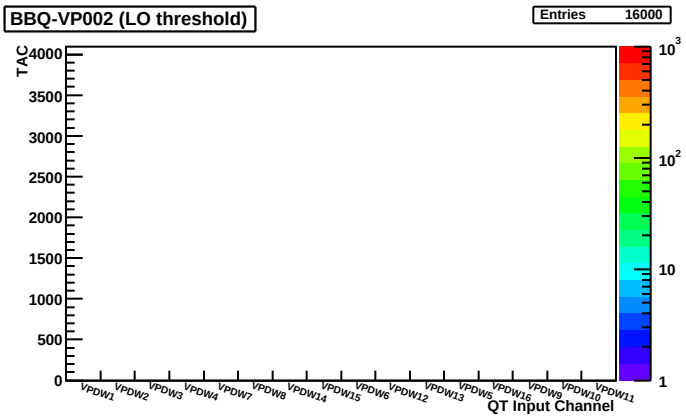

BBQ-ZD001
Entries 16000
ADC
QT Input Channel

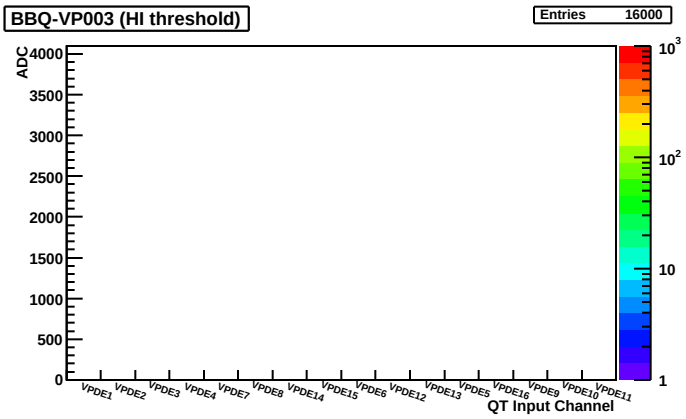

BBQ-ZD001
Entries 16000
TAC
QT Input Channel

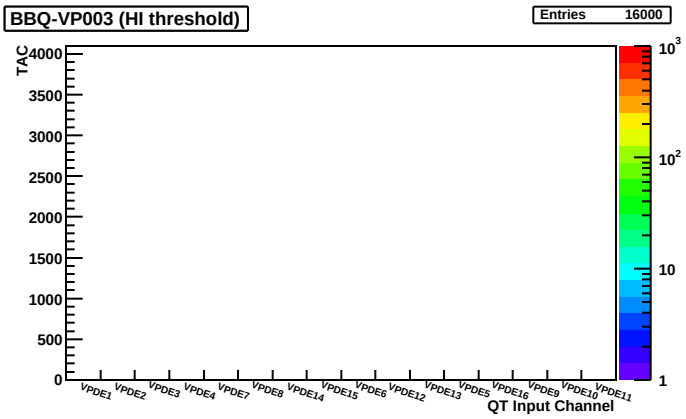

BBQ-VP001 (LO threshold)
Entries 16000
ADC
QT Input Channel

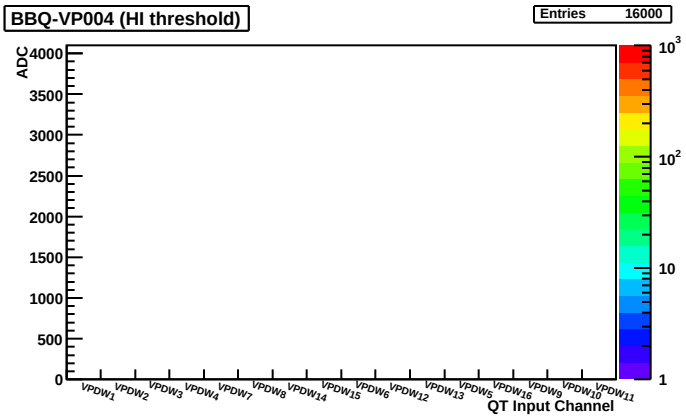

BBQ-VP001 (LO threshold)
Entries 16000
TAC
QT Input Channel

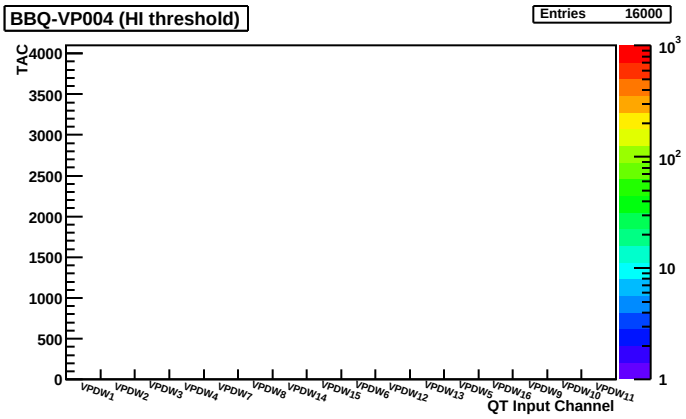

BBQ-VP002 (LO threshold)
Entries 16000
ADC
QT Input Channel

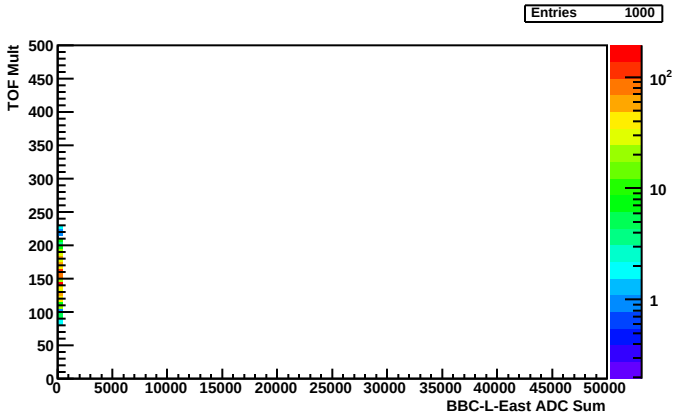

BBQ-VP002 (LO threshold)
Entries 16000
TAC
QT Input Channel

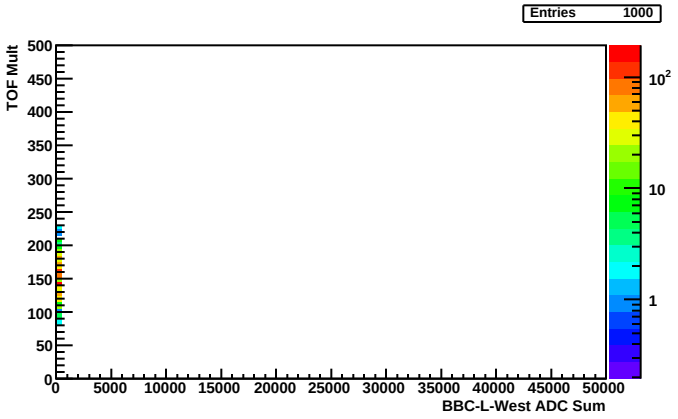

BBQ-VP003 (HI threshold)
Entries 16000
ADC
QT Input Channel

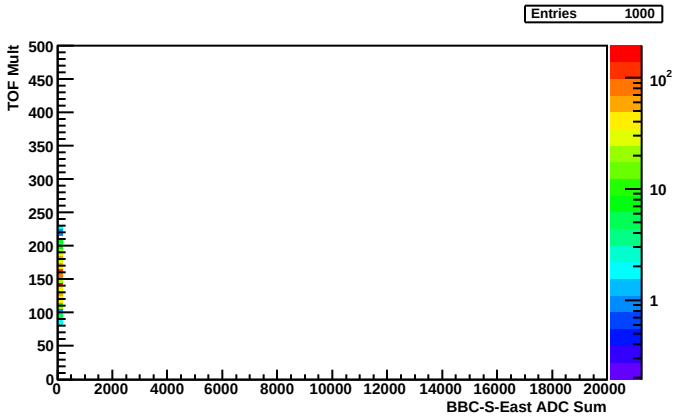

BBQ-VP003 (HI threshold)
Entries 16000
TAC
QT Input Channel

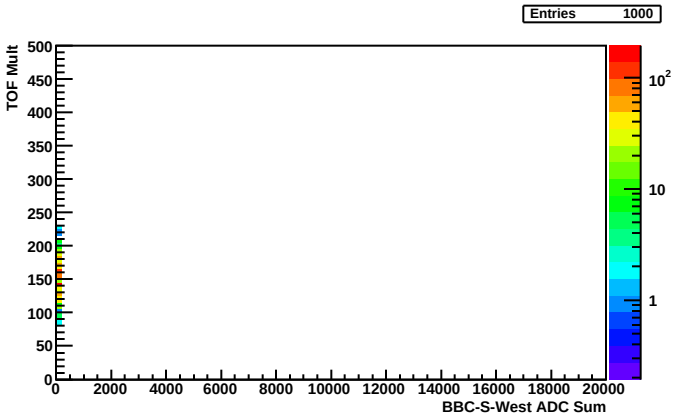

BBQ-VP004 (HI threshold)
Entries 16000
ADC
QT Input Channel

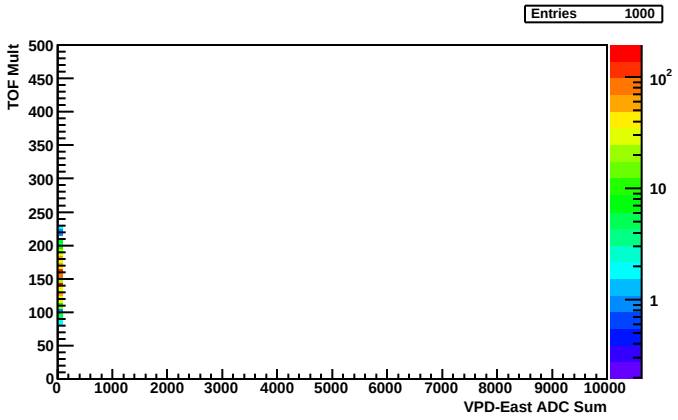

BBQ-VP004 (HI threshold)
Entries 16000
TAC
QT Input Channel

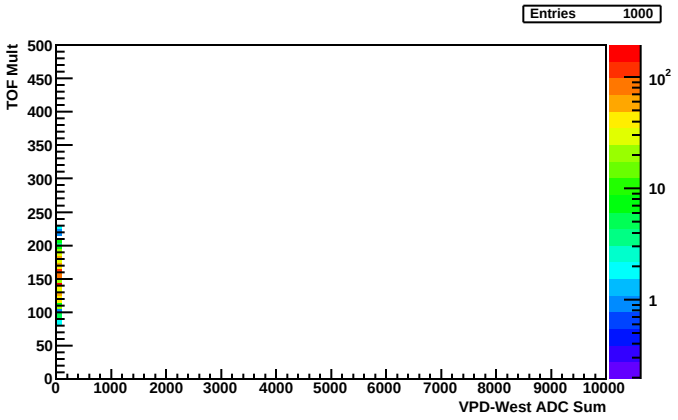

Entries 1000
TOF Mult
BBC-L-East ADC Sum

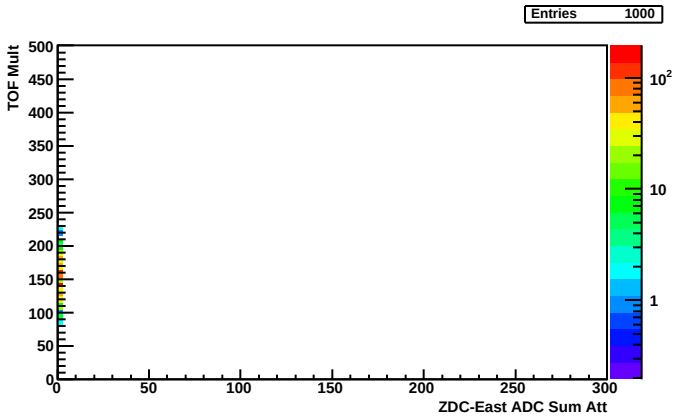

Entries 1000
TOF Mult
BBC-L-West ADC Sum

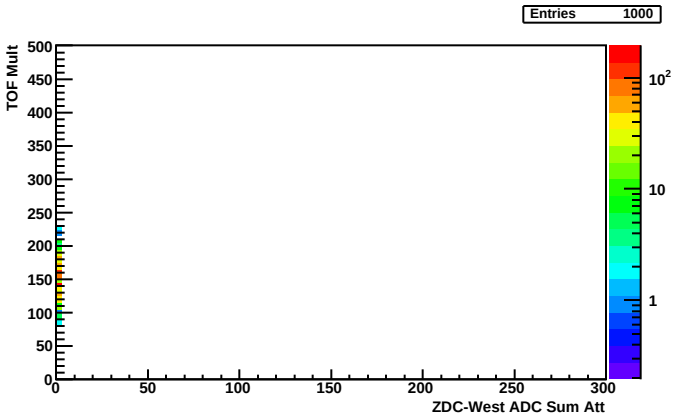

Entries 1000
TOF Mult
BBC-S-East ADC Sum

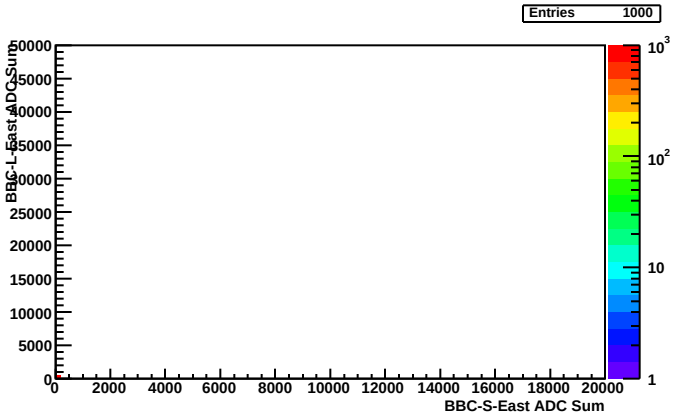

Entries 1000
TOF Mult
BBC-S-West ADC Sum

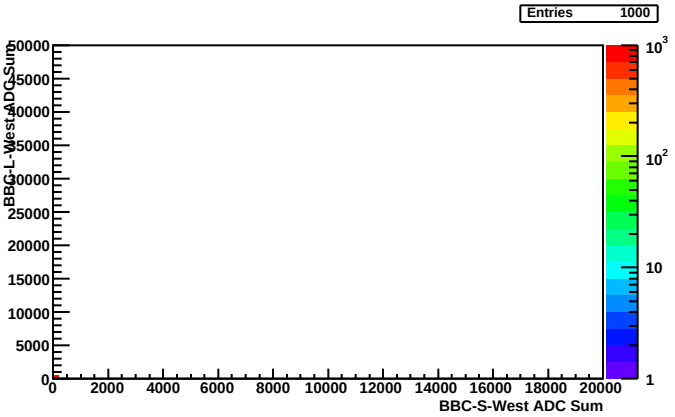

Entries 1000
TOF Mult
VPD-East ADC Sum

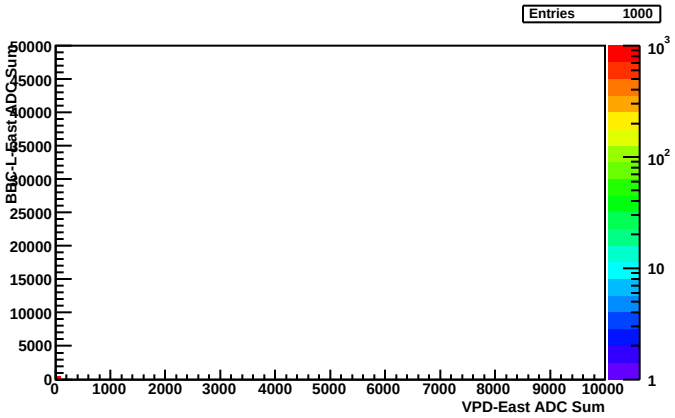

Entries 1000
TOF Mult
VPD-West ADC Sum

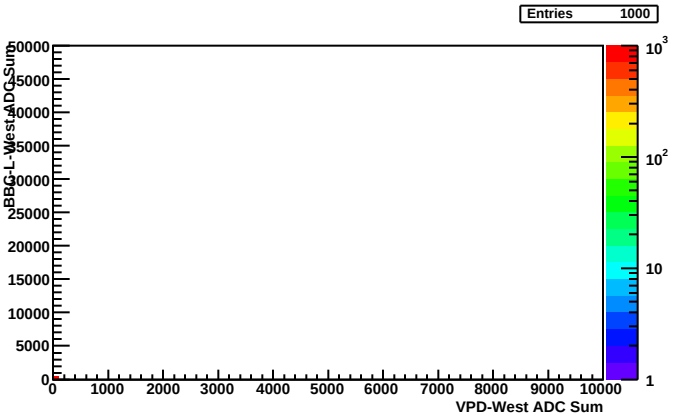

Entries 1000
TOF Mult
ZDC-East ADC Sum Att

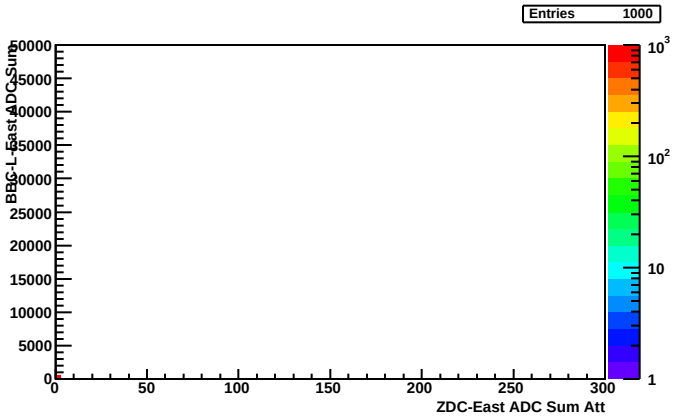

Entries 1000
TOF Mult
ZDC-West ADC Sum Att

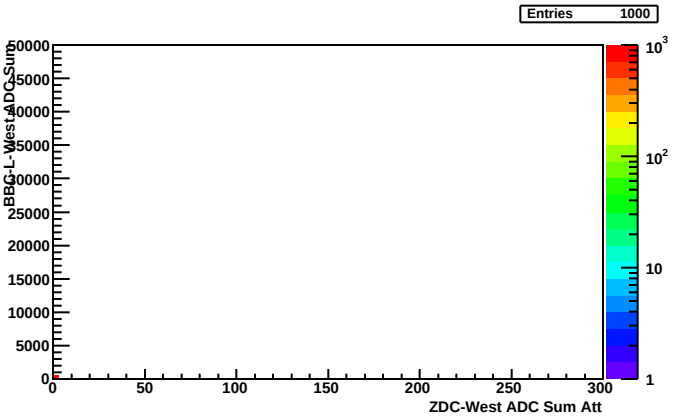

Entries 1000
BBC-L-East ADC Sum
BBC-S-East ADC Sum

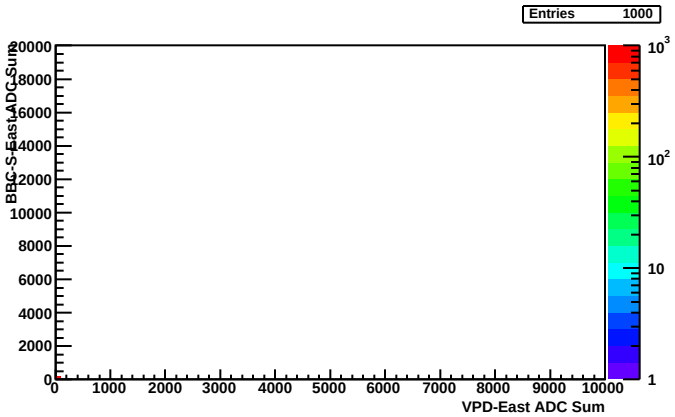

Entries 1000
BBC-L-West ADC Sum
BBC-S-West ADC Sum

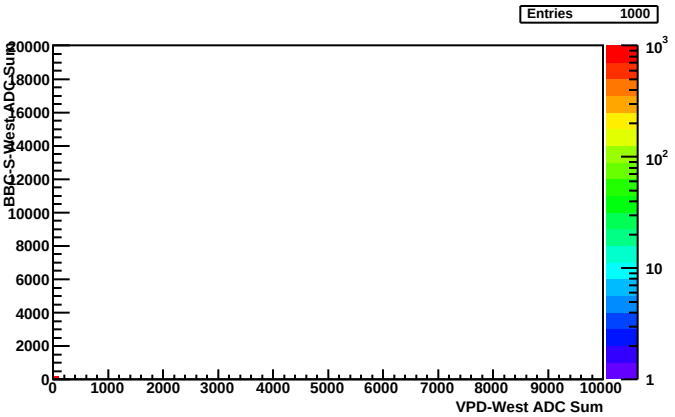

Entries 1000
BBC-L-East ADC Sum
VPD-East ADC Sum

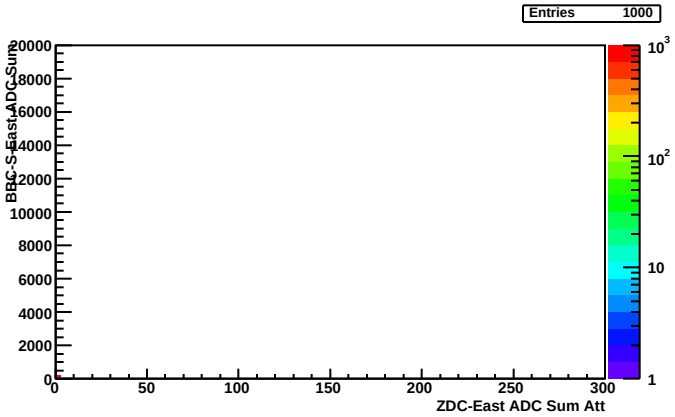

Entries 1000
BBC-L-West ADC Sum
VPD-West ADC Sum

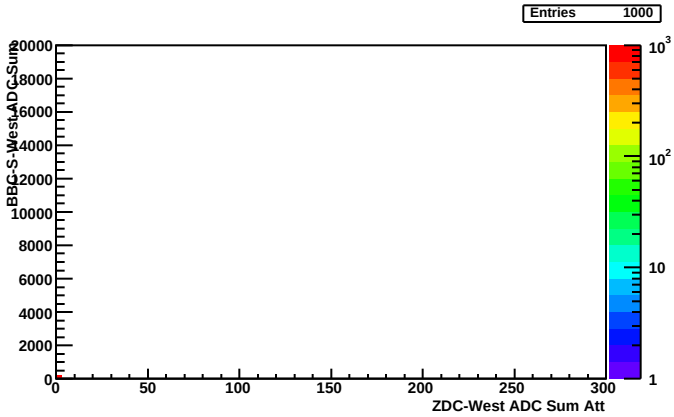

Entries 1000
BBC-L-East ADC Sum
ZDC-East ADC Sum Att

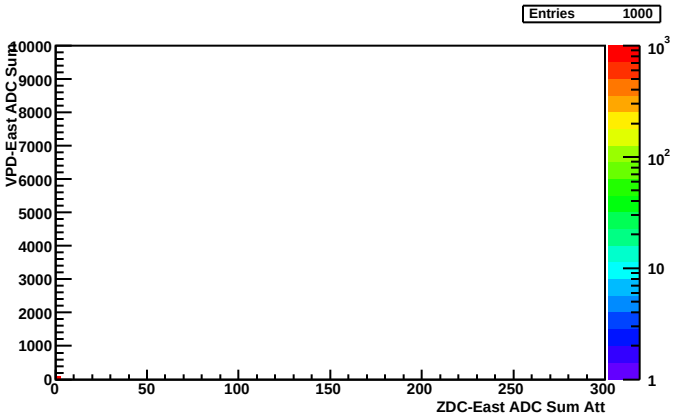

Entries 1000
BBC-L-West ADC Sum
ZDC-West ADC Sum Att

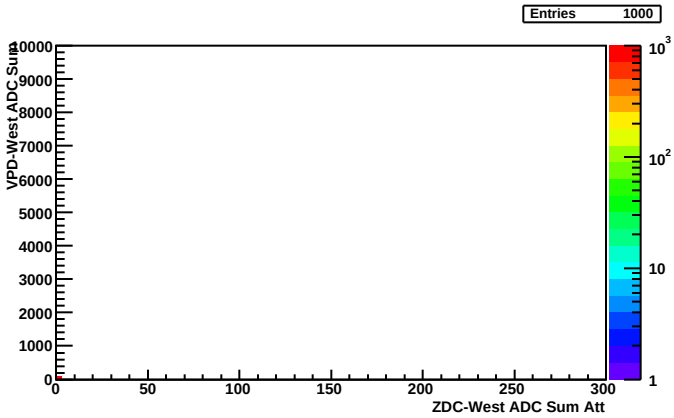

Entries 1000
BBC-S-East ADC Sum
VPD-East ADC Sum

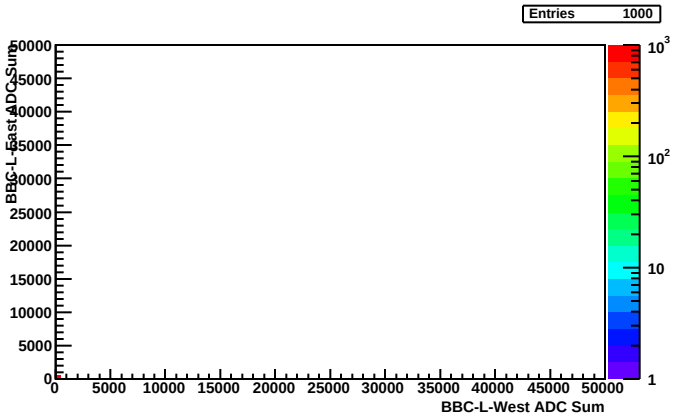

Entries 1000
BBC-S-West ADC Sum
VPD-West ADC Sum

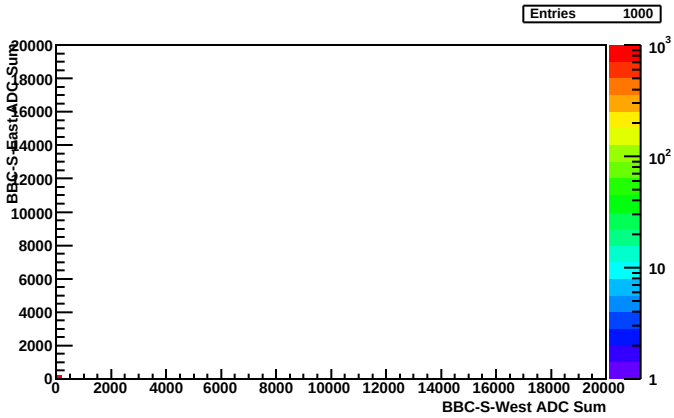

Entries 1000
BBC-S-East ADC Sum
ZDC-East ADC Sum Att

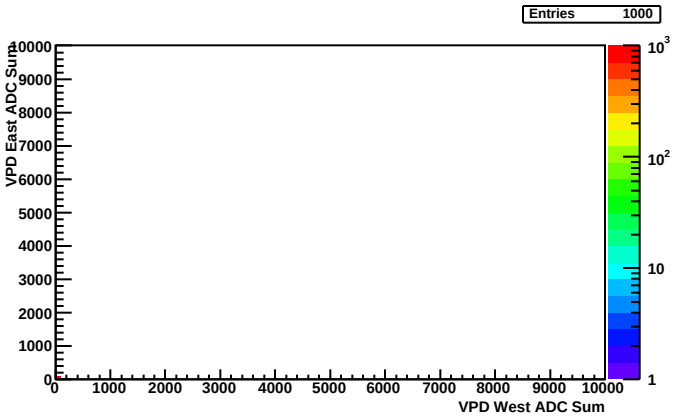

Entries 1000
BBC-S-West ADC Sum
ZDC-West ADC Sum Att

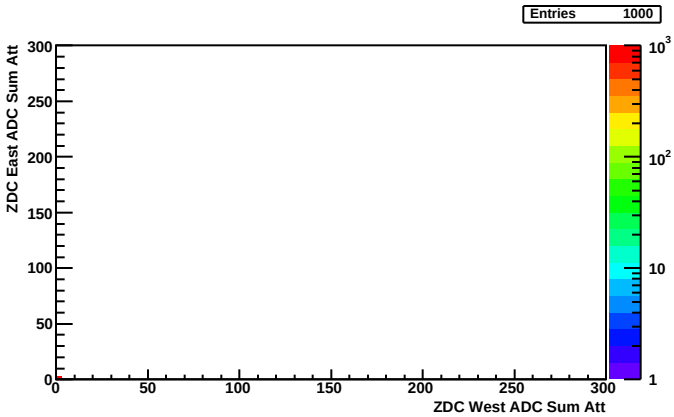

Entries 1000
VPD-East ADC Sum
ZDC-East ADC Sum Att

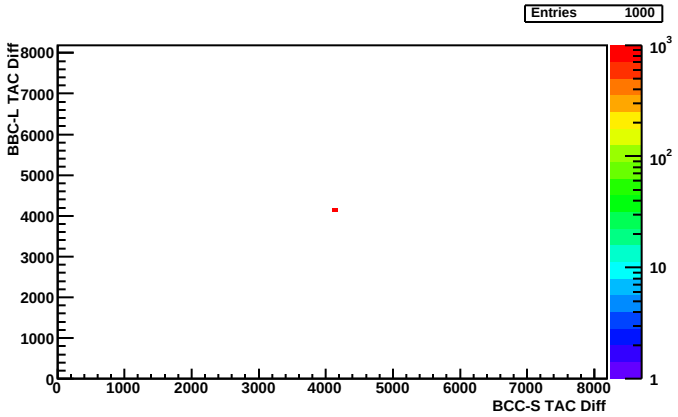

Entries 1000
VPD-West ADC Sum
ZDC-West ADC Sum Att

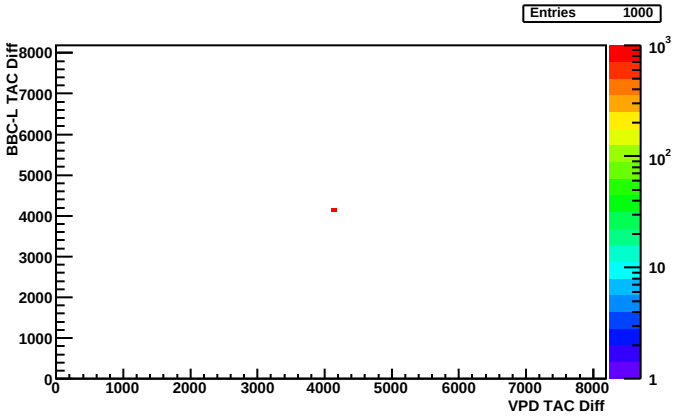

Entries 1000
BBC-L-East ADC Sum
BBC-L-West ADC Sum

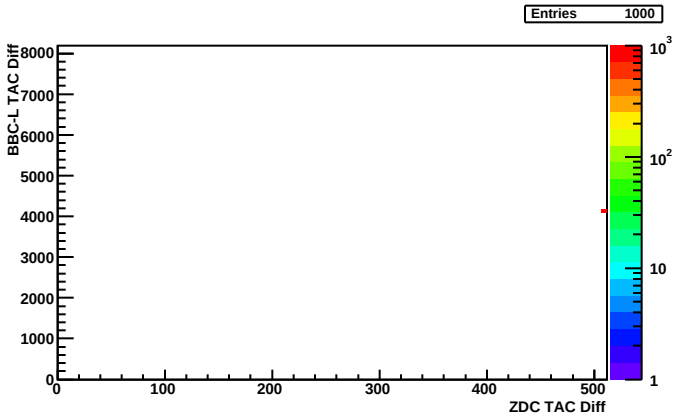

Entries 1000
BBC-S-East ADC Sum
BBC-S-West ADC Sum

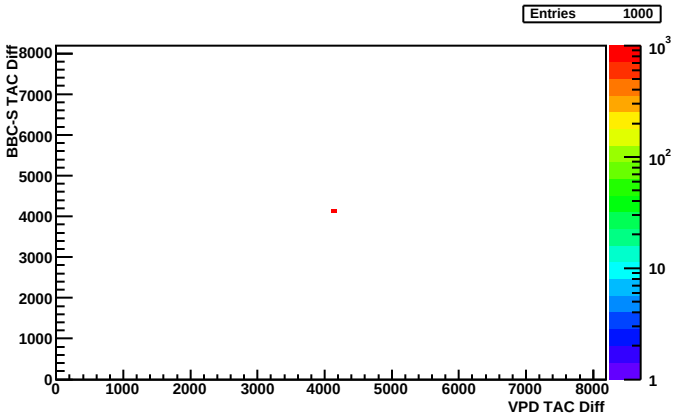

Entries 1000
VPD East ADC Sum
VPD West ADC Sum

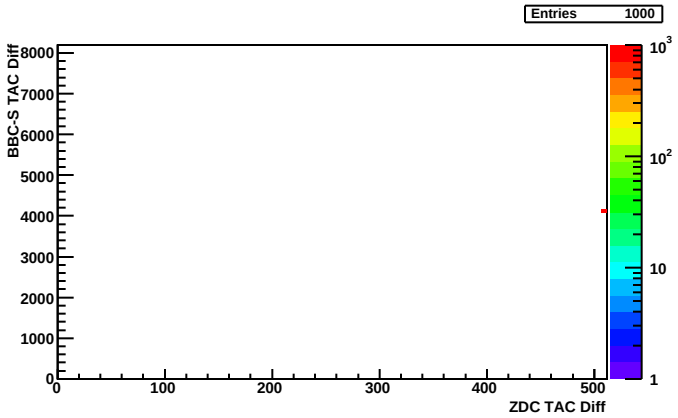

Entries 1000
ZDC East ADC Sum Att
ZDC West ADC Sum Att

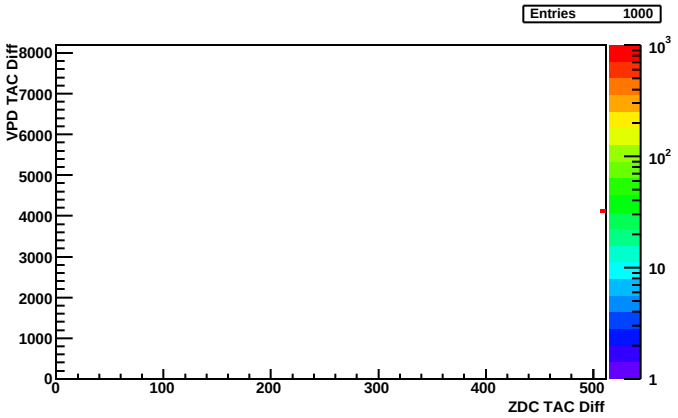

Entries 1000
BBC-L TAC Diff
BCC-S TAC Diff

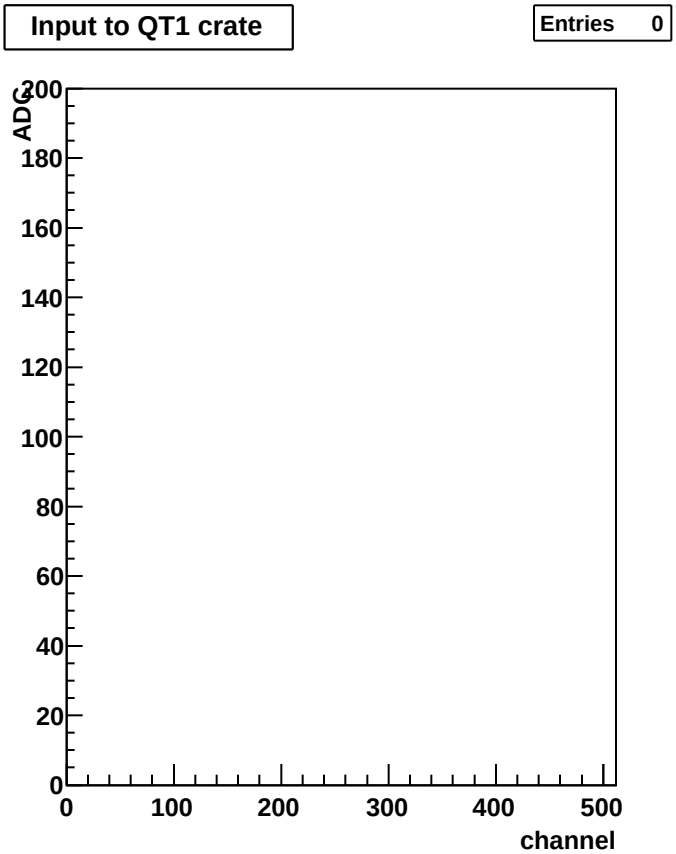

Entries 1000
BBC-L TAC Diff
VPD TAC Diff

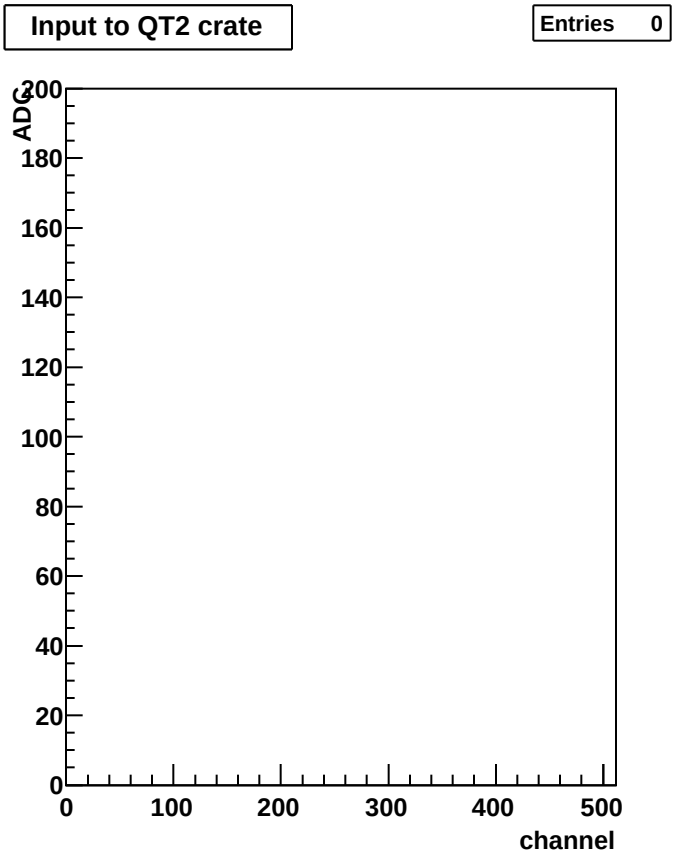

Entries 1000
BBC-L TAC Diff
ZDC TAC Diff

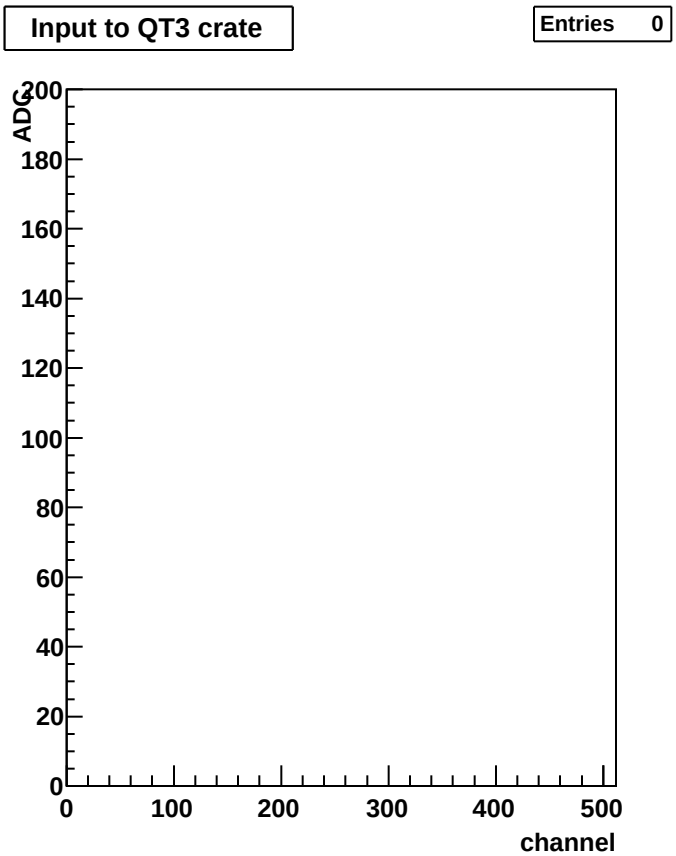

Entries 1000
BBC-S TAC Diff
VPD TAC Diff

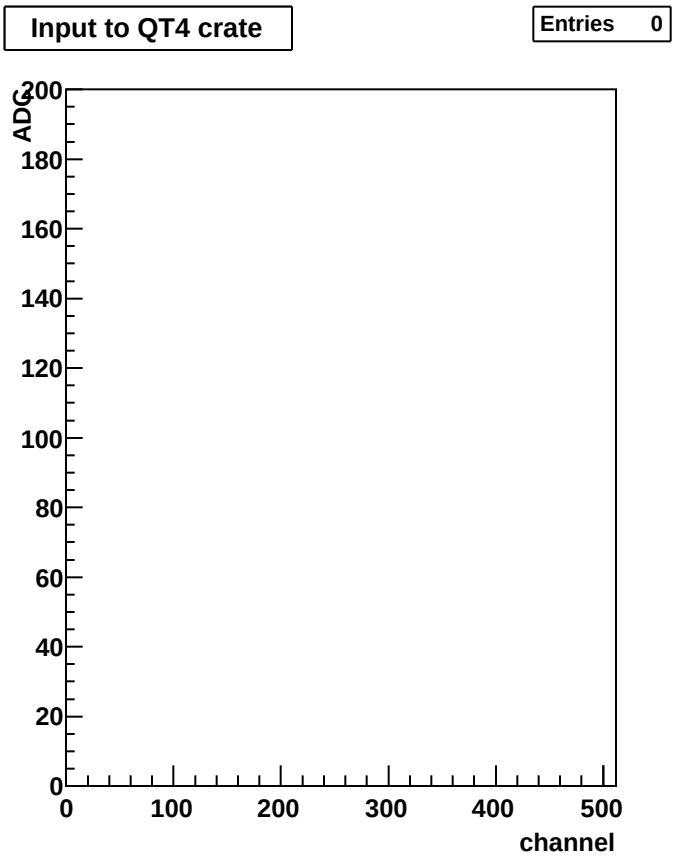

Entries 1000
BBC-S TAC Diff
ZDC TAC Diff

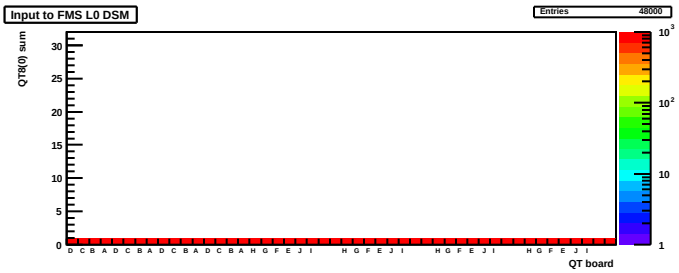

Entries 1000
VPD TAC Diff
ZDC TAC Diff

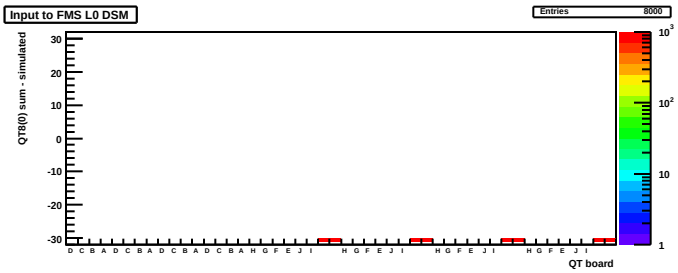

Input to QT1 crate
Entries 0
ADC
200
180
160
140
120
100
80
60
40
20
0
0
100
200
300
400
500
channel

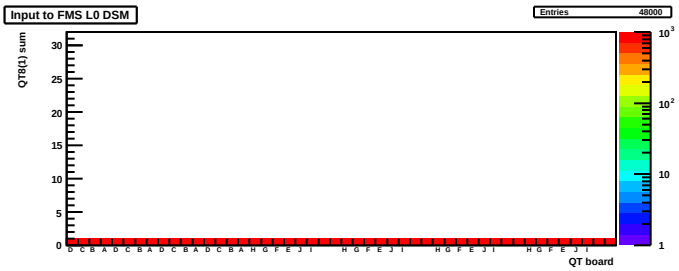

Input to QT2 crate
Entries 0
ADC
200
180
160
140
120
100
80
60
40
20
0
0
100
200
300
400
500
channel

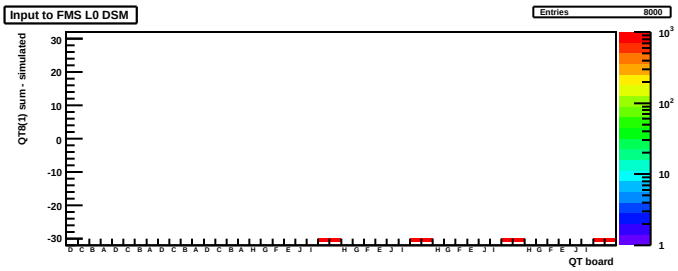

Input to QT3 crate
Entries 0
ADC
200
180
160
140
120
100
80
60
40
20
0
0
100
200
300
400
500
channel

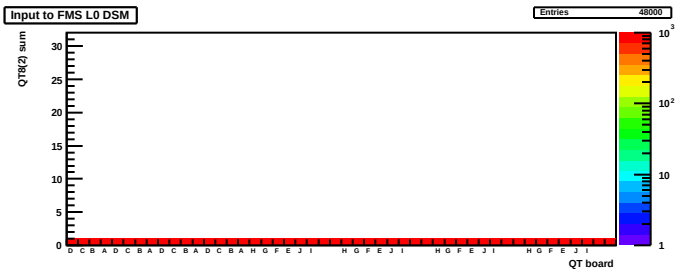

Input to QT4 crate
Entries 0
ADC
200
180
160
140
120
100
80
60
40
20
0
0
100
200
300
400
500
channel

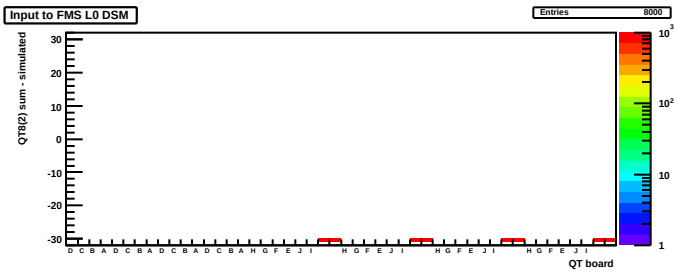

Input to FMS L0 DSM
Entries 48000
QT8(0) sum
QT board

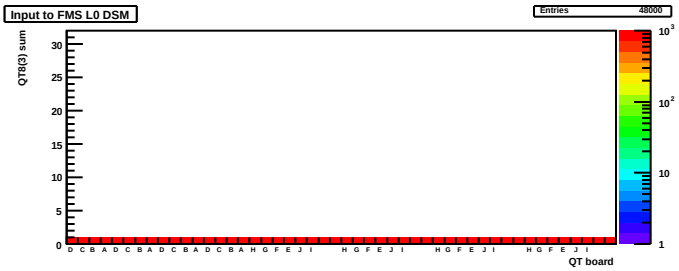

Input to FMS L0 DSM
Entries 8000
QT8(0) sum - simulated
QT board

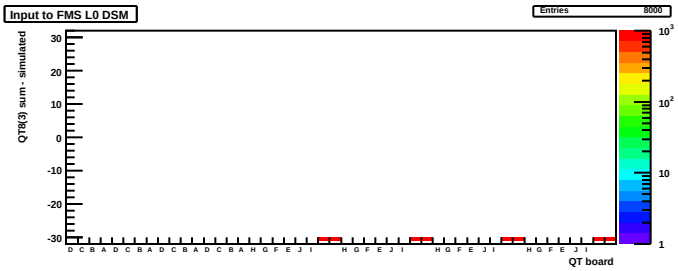

Input to FMS L0 DSM
Entries 48000
QT8(1) sum
QT board

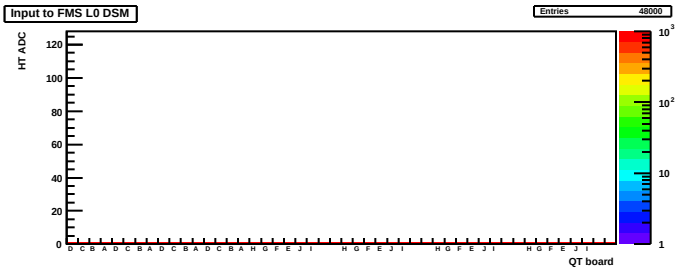

Input to FMS L0 DSM
Entries 8000
QT8(1) sum - simulated
QT board

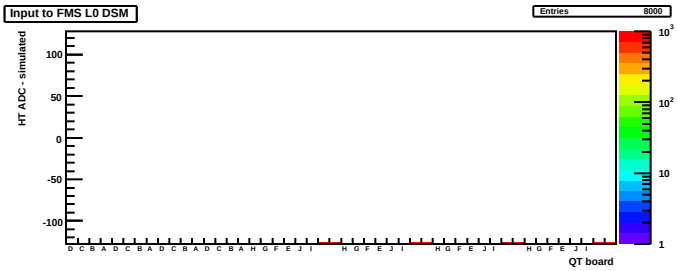

Input to FMS L0 DSM
Entries 48000
QT8(2) sum
QT board

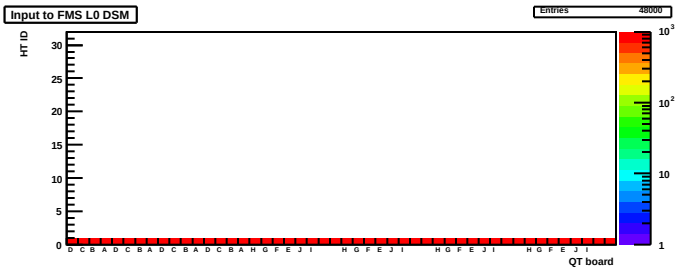

Input to FMS L0 DSM
Entries 8000
QT8(2) sum - simulated
QT board

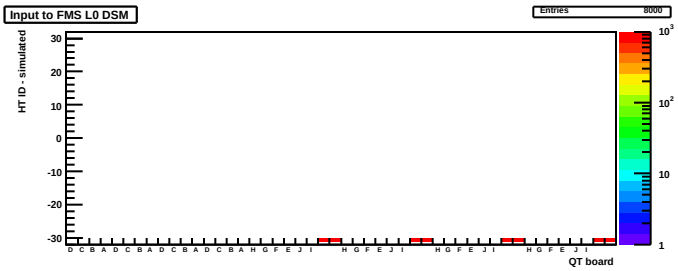

Input to FMS L0 DSM
Entries 48000
QT8(3) sum
QT board

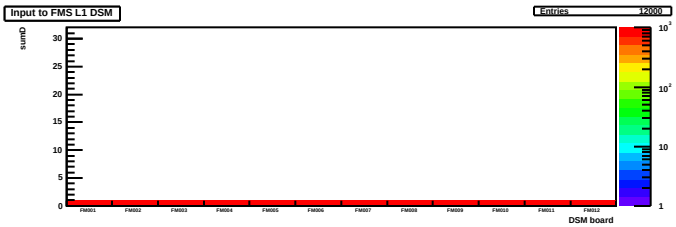

Input to FMS L0 DSM
Entries 8000
QT8(3) sum - simulated
QT board

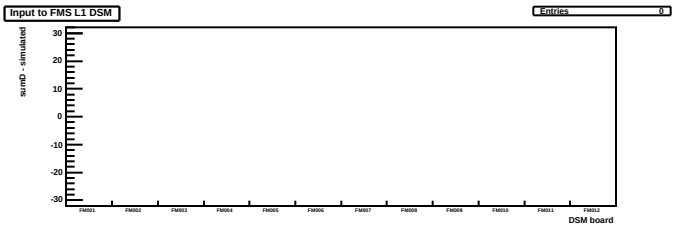

Input to FMS L0 DSM
Entries 48000
HT ADC
QT board

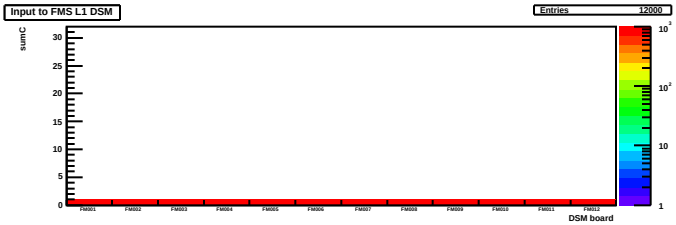

Input to FMS L0 DSM
Entries 8000
HT ADC - simulated
QT board

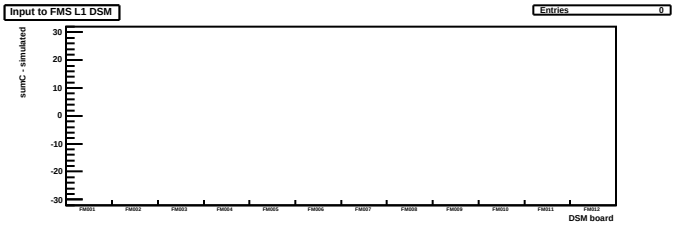

Input to FMS L0 DSM
Entries 48000
HT ID
QT board

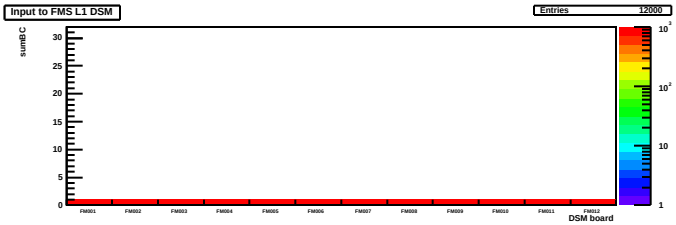

Input to FMS L0 DSM
Entries 8000
HT ID - simulated
QT board

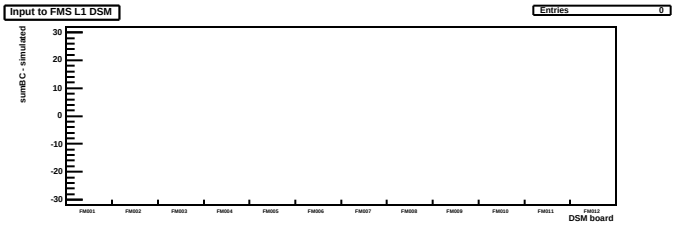

Input to FMS L1 DSM
Entries 12000
sumD
DSM board

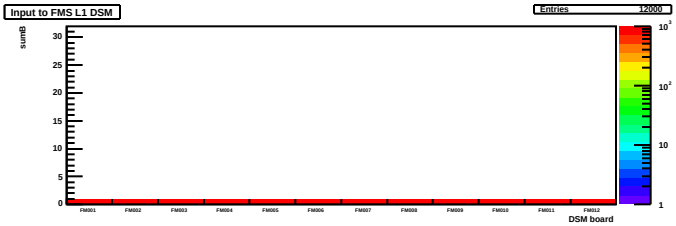

Input to FMS L1 DSM
Entries 0
sumD - simulated
DSM board

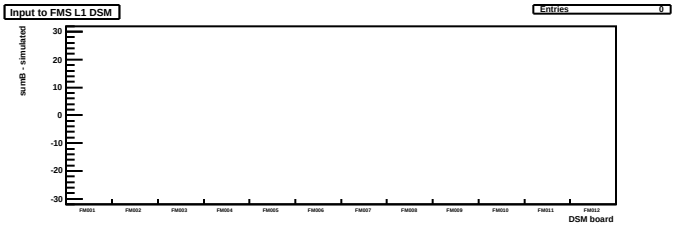

Input to FMS L1 DSM
Entries 12000
sumC
DSM board

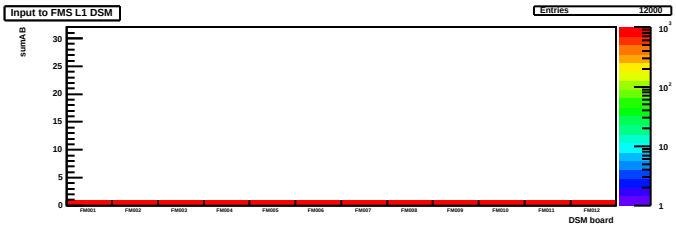

Input to FMS L1 DSM
Entries 0
sumC - simulated
DSM board

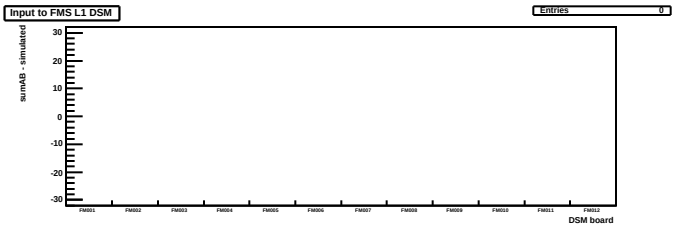

Input to FMS L1 DSM
Entries 12000
sumBC
DSM board

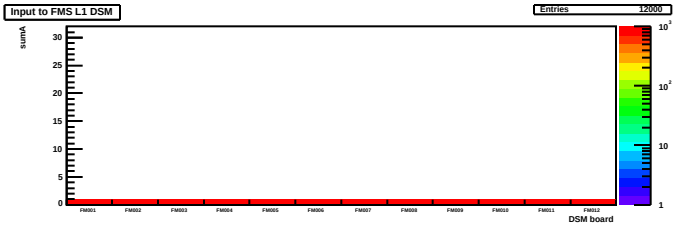

Input to FMS L1 DSM
Entries 0
sumBC - simulated
DSM board

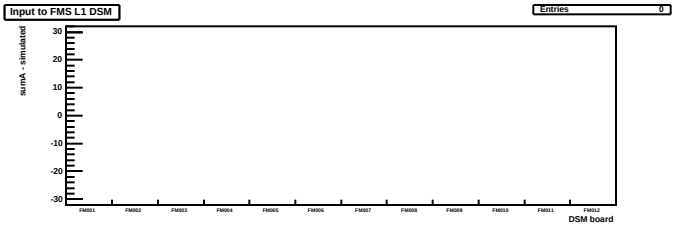

Input to FMS L1 DSM
Entries 12000
sumB
DSM board

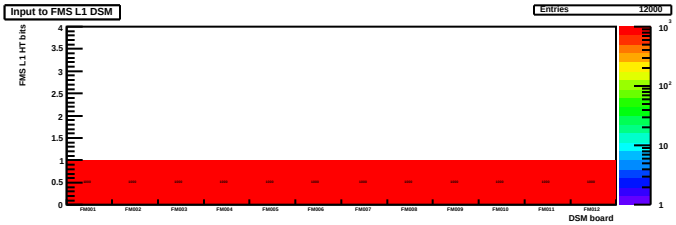

Input to FMS L1 DSM
Entries 0
sumB - simulated
DSM board

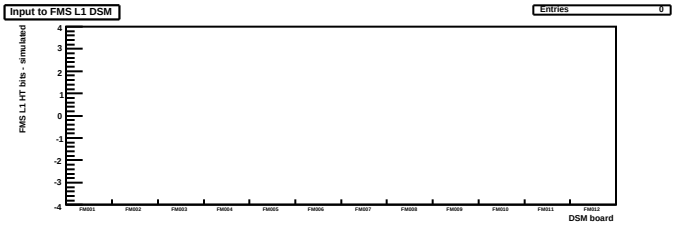

Input to FMS L1 DSM
Entries 12000
sumAB
DSM board

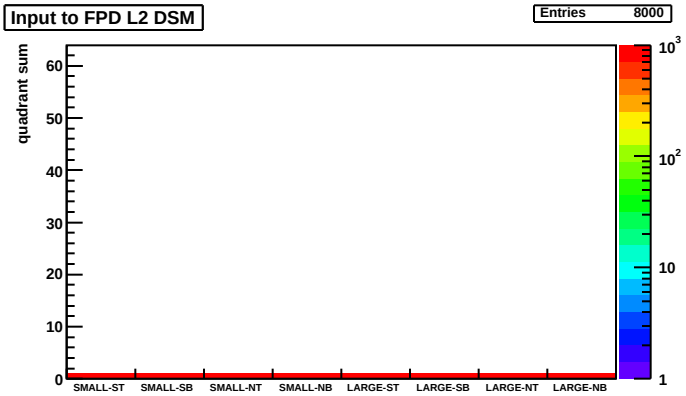

Input to FMS L1 DSM
Entries 0
sumAB - simulated
DSM board

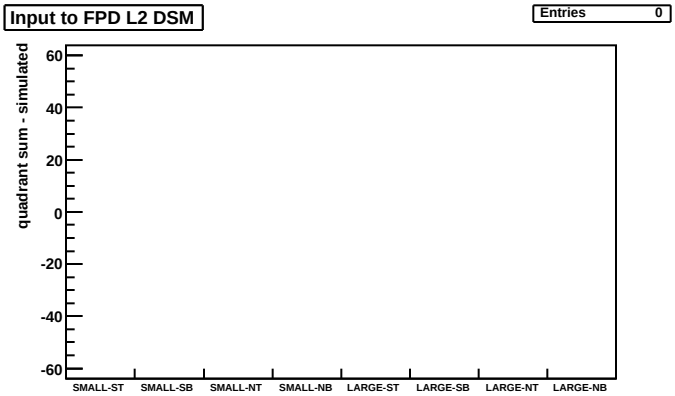

Input to FMS L1 DSM
Entries 12000
sumA
DSM board

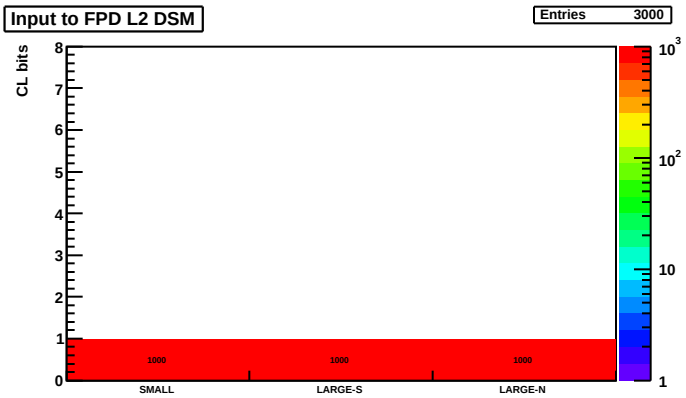

Input to FMS L1 DSM
Entries 0
sumA - simulated
DSM board

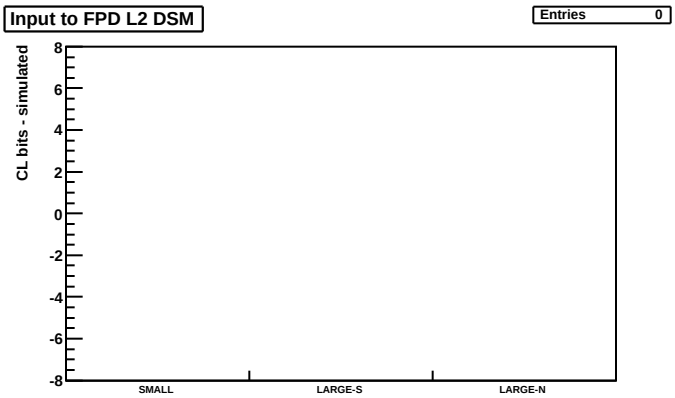

Input to FMS L1 DSM
Entries 12000
FMS L1 HT bits
DSM board

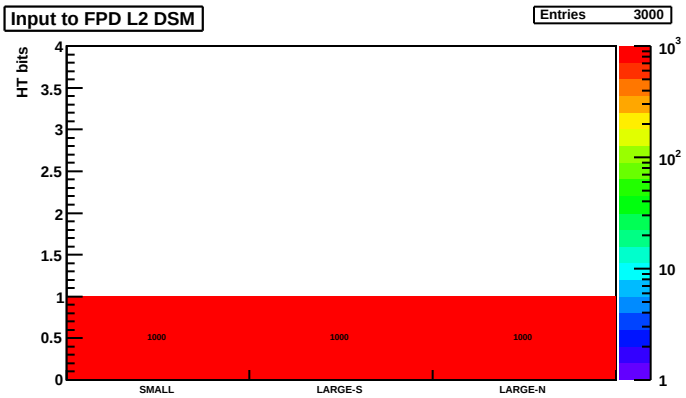

Input to FMS L1 DSM
Entries 0
FMS L1 HT bits - simulated
DSM board

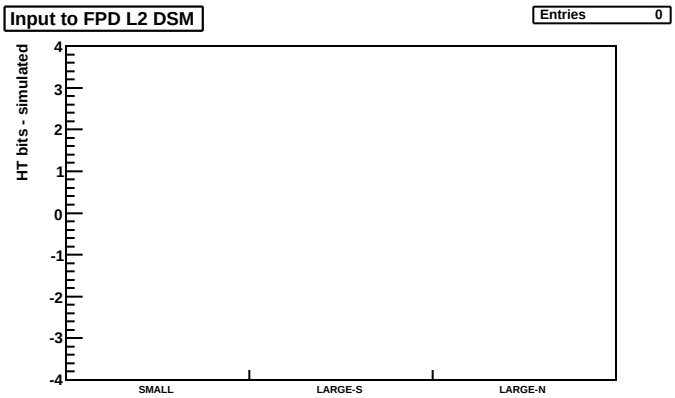

Input to FPD L2 DSM
Entries 8000
quadrant sum
SMALL-ST SMALL-SB SMALL-NT SMALL-NB LARGE-ST LARGE-SB LARGE-NT LARGE-NB

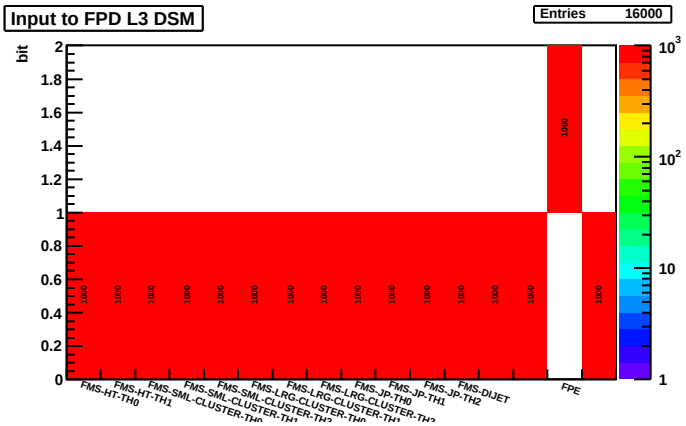

Input to FPD L2 DSM
Entries 0
quadrant sum - simulated
SMALL-ST SMALL-SB SMALL-NT SMALL-NB LARGE-ST LARGE-SB LARGE-NT LARGE-NB

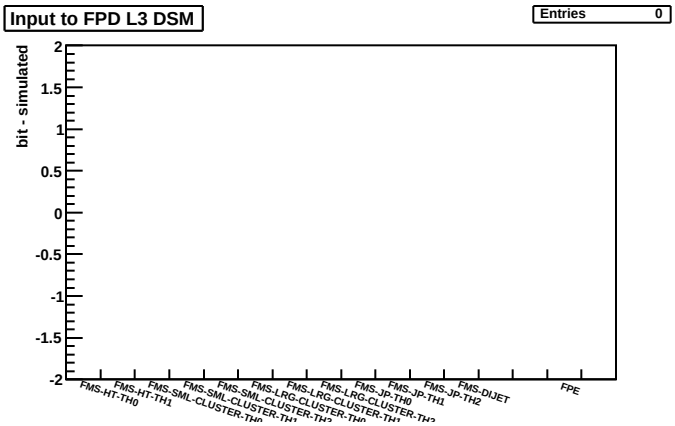

Input to FPD L2 DSM
Entries 3000
CL bits
1000 1000 1000
SMALL LARGE-S LARGE-N

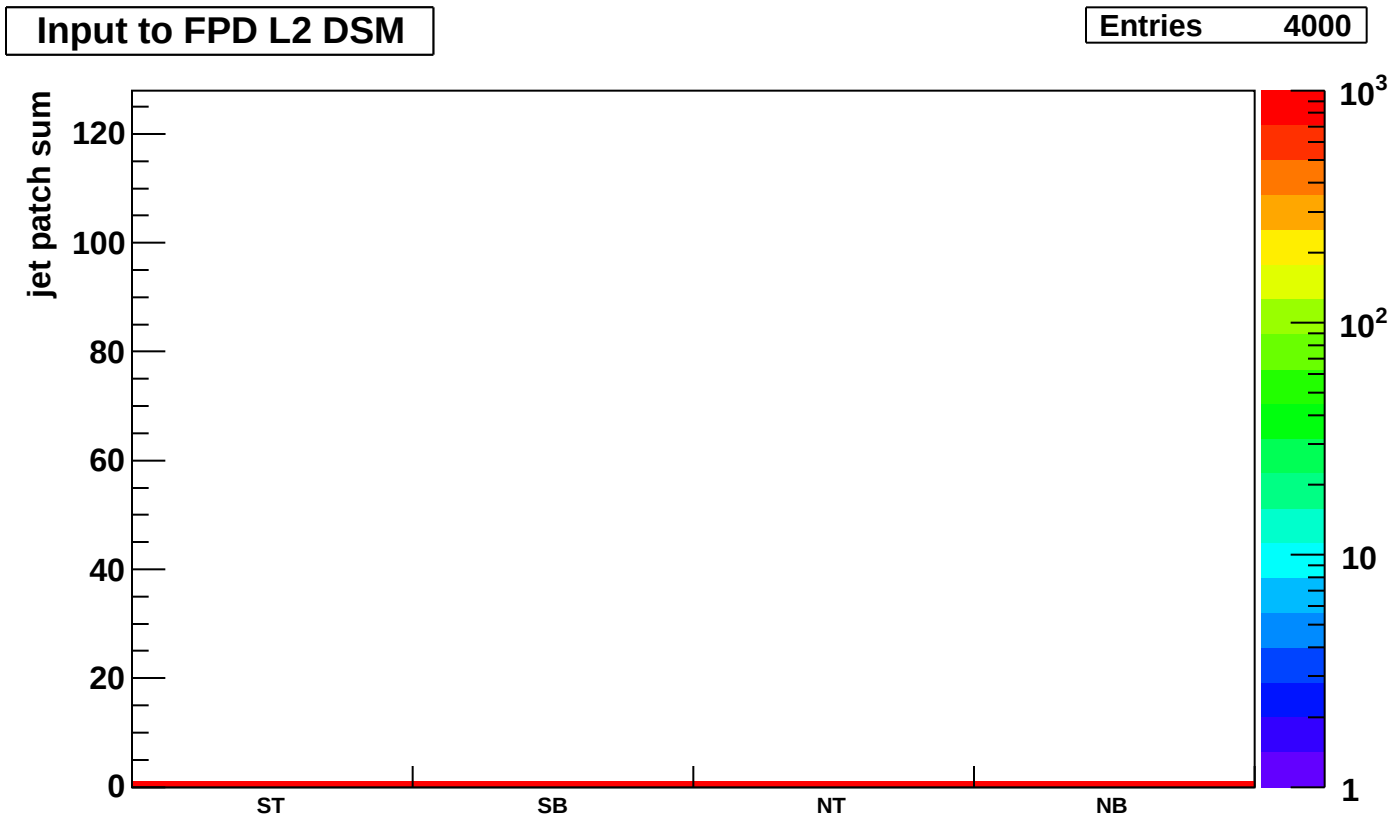

Input to FPD L2 DSM
Entries 0
CL bits - simulated
SMALL LARGE-S LARGE-N

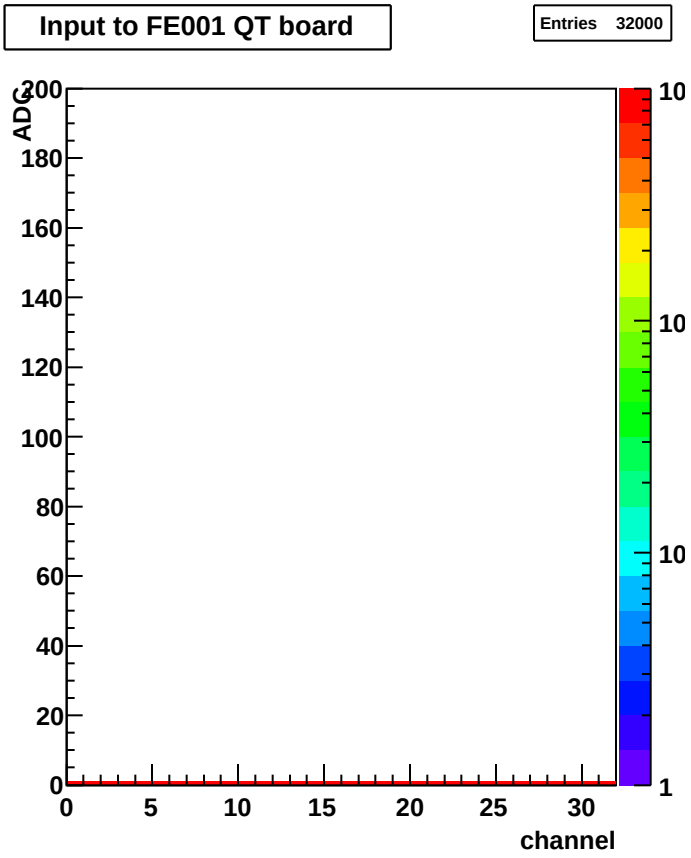

Input to FPD L2 DSM
Entries 3000
HT bits
1000 1000 1000
SMALL LARGE-S LARGE-N

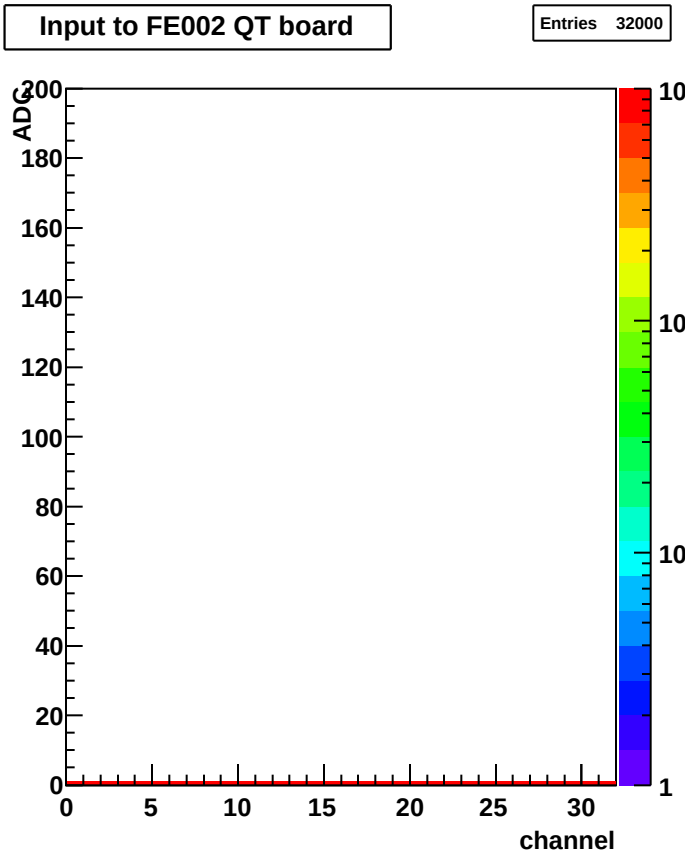

Input to FPD L2 DSM
Entries 0
HT bits - simulated
SMALL LARGE-S LARGE-N

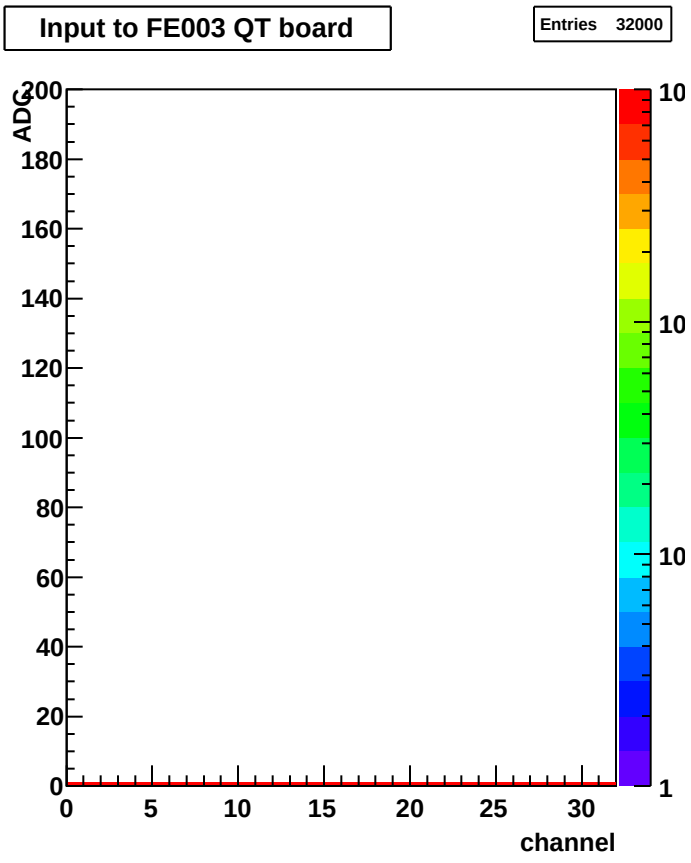

Input to FPD L3 DSM
Entries 16000
bit
FMS-HT-TH0 FMS-HT-TH1 FMS-SML-CLUSTER-TH0 FMS-SML-CLUSTER-TH1 FMS-SML-CLUSTER-TH2 FMS-LRG-CLUSTER-TH0 FMS-LRG-CLUSTER-TH1 FMS-LRG-CLUSTER-TH2 FMS-JP-TH0 FMS-JP-TH1 FMS-JP-TH2 FMS-DIJET FPE

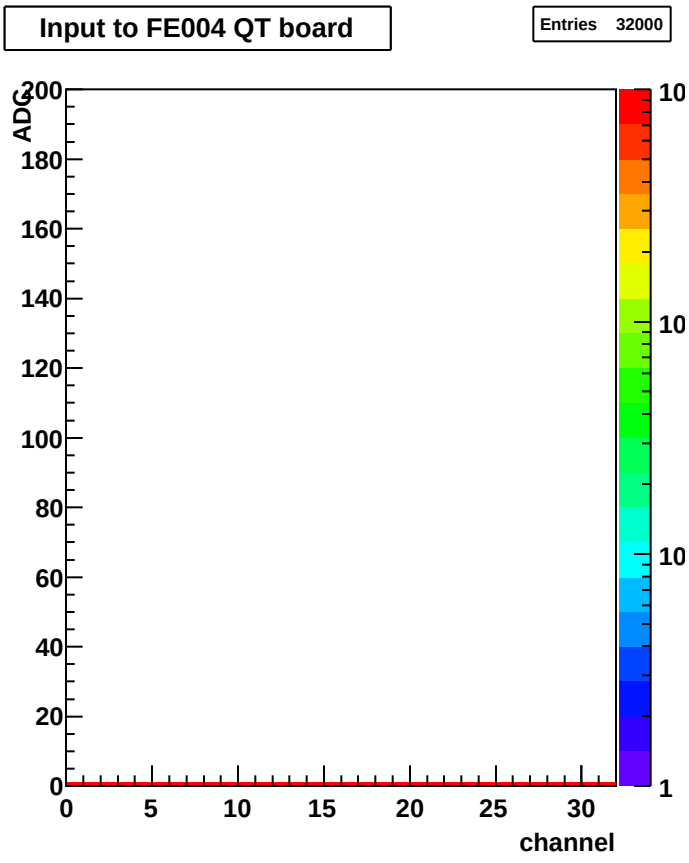

Input to FPD L3 DSM
Entries 0
bit - simulated
FMS-HT-TH0 FMS-HT-TH1 FMS-SML-CLUSTER-TH0 FMS-SML-CLUSTER-TH1 FMS-SML-CLUSTER-TH2 FMS-LRG-CLUSTER-TH0 FMS-LRG-CLUSTER-TH1 FMS-LRG-CLUSTER-TH2 FMS-JP-TH0 FMS-JP-TH1 FMS-JP-TH2 FMS-DIJET FPE

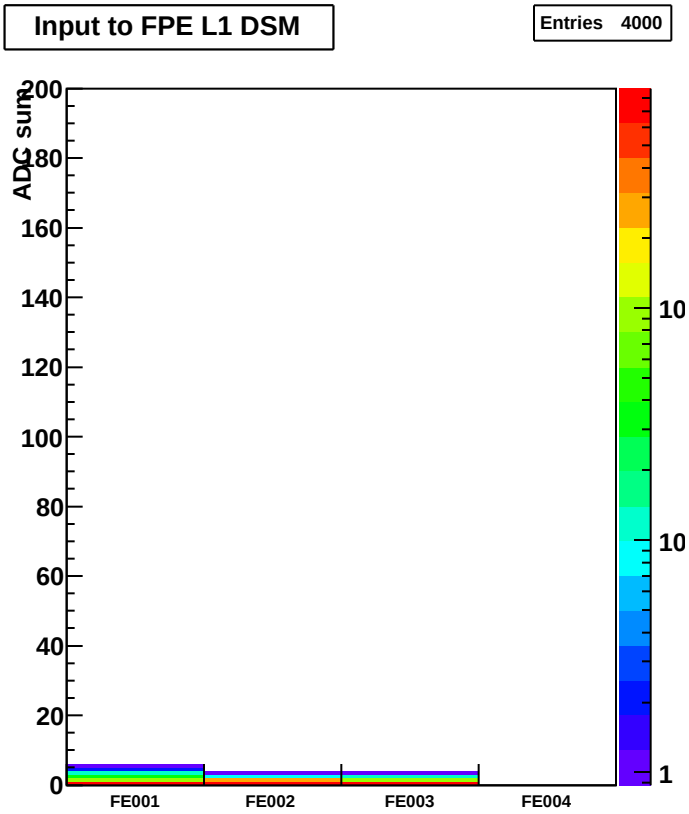

Input to FPD L2 DSM
Entries 4000
jet patch sum
120
100
80
60
40
20
0
ST
SB
NT
NB
10^3
10^2
10
1

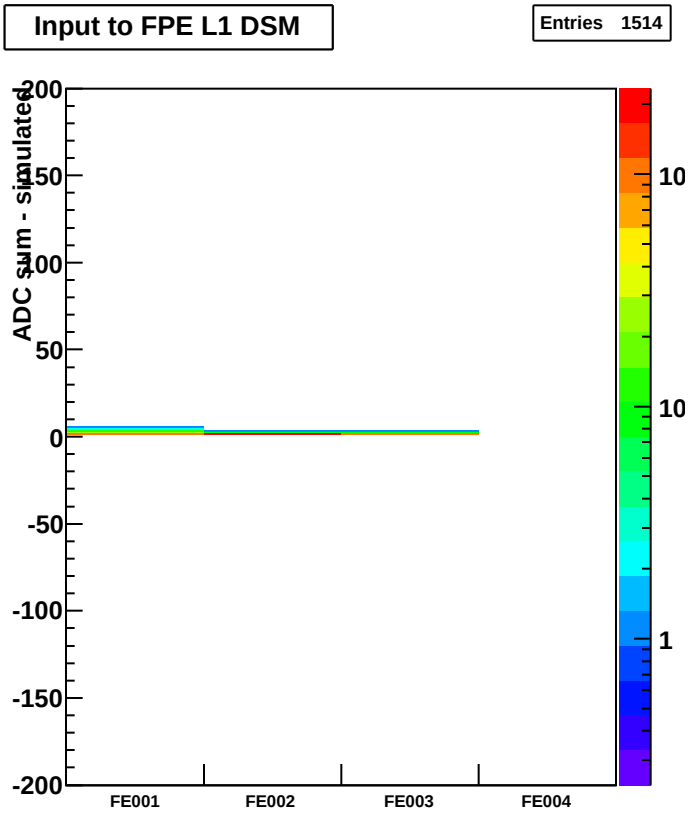

Input to FE001 QT board
Entries 32000
ADC
channel

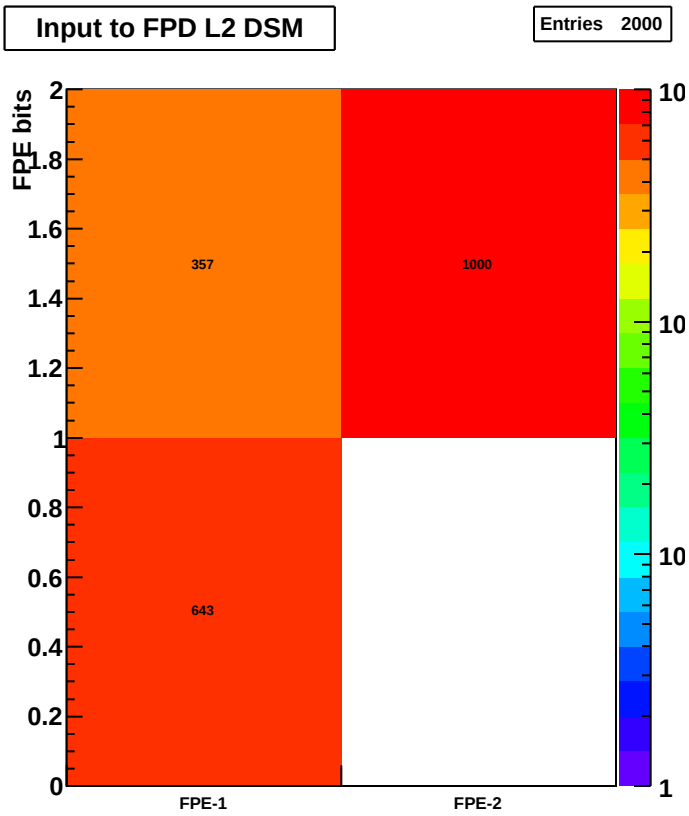

Input to FE002 QT board
Entries 32000
ADC
channel

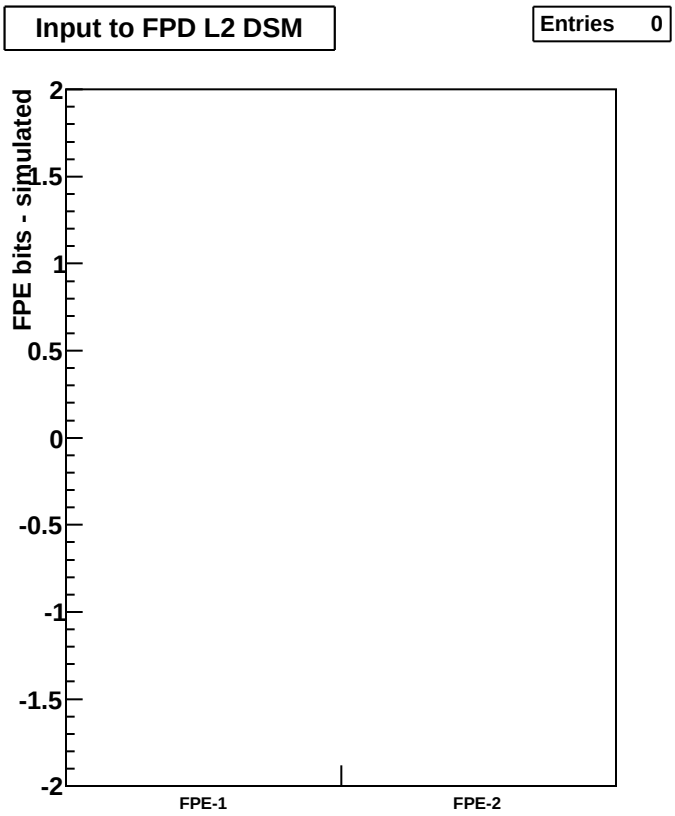

Input to FE003 QT board
Entries 32000
ADC
channel


Input to FE004 QT board
Entries 32000
ADC
channel


Input to FPE L1 DSM
Entries 4000
ADC sum
200
180
160
140
120
100
80
60
40
20
0
FE001
FE002
FE003
FE004
10
10
1


Input to FPE L1 DSM
Entries 1514
ADC sum - simulated
200
150
100
50
0
-50
-100
-150
-200
FE001
FE002
FE003
FE004
10
10
1


Input to FPD L2 DSM
Entries 2000
FPE bits
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
357
1000
643
FPE-1
FPE-2
10
10
10
1


Input to FPD L2 DSM
Entries 0
FPE bits - simulated
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
FPE-1
FPE-2